Medium Power Amplifier
71 - 86 GHz

Features
- 4 Stage Driver Amplifier for E Band
- 18 dB Gain
- 10 dB Input and Output Match
- 24 dBm Saturated Output Power
- 27 dBm OIP3
- Variable Gain with Adjustable Bias
- Integrated Detector
- Bare die
- RoHS* Compliant
- HBM ESD rating of 200 V
- Size: 3780 x 1500 x 50 µm

Description
The MAAM-011167 is a bare die power amplifier that operates from 71 - 86 GHz. The amplifier provides 18 dB small signal gain. The input and output are matched to 50 Ω with bond wires to external board.

It is designed for use as a driver stage in transmit chains and is ideally suited for E band point to point radios.

Each device is 100% RF tested to ensure performance compliance. The part is fabricated using an efficient pHEMT process.

Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAAM-011167-DIE</td>
<td>Die in Vacuum release gel pack</td>
</tr>
</tbody>
</table>

Pad Configuration

<table>
<thead>
<tr>
<th>Pad No.</th>
<th>Function</th>
<th>Pad No.</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>V_D1</td>
<td>9</td>
<td>V_REF</td>
</tr>
<tr>
<td>2</td>
<td>V_D2</td>
<td>10</td>
<td>GND_DET</td>
</tr>
<tr>
<td>3</td>
<td>V_D3</td>
<td>11</td>
<td>V_G4</td>
</tr>
<tr>
<td>4</td>
<td>V_D4</td>
<td>12</td>
<td>V_G3</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>13</td>
<td>V_G2</td>
</tr>
<tr>
<td>6</td>
<td>RF_OUT</td>
<td>14</td>
<td>V_G1</td>
</tr>
<tr>
<td>7</td>
<td>GND</td>
<td>15</td>
<td>GND</td>
</tr>
<tr>
<td>8</td>
<td>V_DET</td>
<td>16</td>
<td>RF_IN</td>
</tr>
<tr>
<td></td>
<td></td>
<td>17</td>
<td>GND</td>
</tr>
</tbody>
</table>

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Electrical Specifications\(^1,2\): Freq. = 71 - 86 GHz, \(V_D = 4\) V, \(I_D = 360\) mA, \(T_A = 25^\circ\)C

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Units</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>dB</td>
<td>16</td>
<td>18</td>
<td>-</td>
</tr>
<tr>
<td>Input Return Loss</td>
<td>dB</td>
<td>-</td>
<td>10</td>
<td>-</td>
</tr>
<tr>
<td>Output Return Loss</td>
<td>dB</td>
<td>-</td>
<td>10</td>
<td>-</td>
</tr>
<tr>
<td>(P_{1dB})</td>
<td>dB</td>
<td>-</td>
<td>21</td>
<td>-</td>
</tr>
<tr>
<td>(P_{OUT}) with (P_{IN}) = 10 dBm</td>
<td>dBm</td>
<td>20</td>
<td>24</td>
<td>-</td>
</tr>
<tr>
<td>(P_{SAT}) (P3dB)</td>
<td>dBm</td>
<td>-</td>
<td>24</td>
<td>-</td>
</tr>
<tr>
<td>OIP3 (worst tone)</td>
<td>dBm</td>
<td>-</td>
<td>27</td>
<td>-</td>
</tr>
<tr>
<td>IIP3 (worst tone) for Gain = 20 turned-down to -5 dB</td>
<td>dBm</td>
<td>-</td>
<td>10</td>
<td>-</td>
</tr>
</tbody>
</table>

1. Minimum limits are the on-wafer minimum test limits.
2. Quiescent DC Bias: \(I_{c1}= 30\) mA, \(I_{c2}= 60\) mA, \(I_{c3}= 120\) mA, \(I_{c4}= 150\) mA. Total DC Power = 1.44 W.

Absolute Maximum Ratings\(^3,4,5\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Absolute Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain Voltage</td>
<td>4.3 V</td>
</tr>
<tr>
<td>Drain Current</td>
<td>460 mA</td>
</tr>
<tr>
<td>Gate Bias Voltage ((V_G))</td>
<td>(-1.5 V &lt; V_G &lt; +0.3) V</td>
</tr>
<tr>
<td>Input Power</td>
<td>13 dBm</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-55°C to +150°C</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>150°C</td>
</tr>
<tr>
<td>Thermal Resistance</td>
<td>16.15°C/W</td>
</tr>
</tbody>
</table>

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these class 0 static sensitive devices.
Typical Performance Curves

**Gain @ VD = 4 V, I_{DQ} = 360 mA**

**Reverse Isolation @ VD = 4 V, I_{DQ} = 360 mA**

**Input Return Loss @ VD = 4 V, I_{DQ} = 360 mA**

**Output Return Loss @ VD = 4 V, I_{DQ} = 360 mA**
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Typical Performance Curves

**Gain, @ VD = 4 V, Frequency = 80 GHz**

**Reverse Isolation @ VD = 4 V, Frequency = 80 GHz**

**Input Return Loss @ VD = 4 V, Frequency = 80 GHz**

**Output Return Loss @ VD = 4 V, Frequency = 80 GHz**

**Detector Delta Voltage @ VD = 4 V**
Typical Performance Curves

**P1dB vs. Frequency @ VD = 4 V, IDQ = 360 mA**

![Graph showing P1dB vs. Frequency at 4 V, IDQ = 360 mA](image)

**P3dB vs. Frequency @ VD = 4 V, IDQ = 360 mA**

![Graph showing P3dB vs. Frequency at 4 V, IDQ = 360 mA](image)

**Output IP3 vs. Frequency @ VD = 4 V, IDQ = 250 mA**

![Graph showing Output IP3 vs. Frequency at 4 V, IDQ = 250 mA](image)

**Output IP3 vs. Frequency @ VD = 4 V, IDQ = 360 mA**

![Graph showing Output IP3 vs. Frequency at 4 V, IDQ = 360 mA](image)

**P_{OUT}, P_{IN} = 10 dBm @ VD = 4 V, IDQ = 250 mA**

![Graph showing P_{OUT}, P_{IN} = 10 dBm at 4 V, IDQ = 250 mA](image)

**P_{OUT}, P_{IN} = 10 dBm @ VD = 4 V, IDQ = 360 mA**

![Graph showing P_{OUT}, P_{IN} = 10 dBm at 4 V, IDQ = 360 mA](image)
Typical Performance Curves

**Lower Tone Gain vs. Total Current @ VD = 4 V**

![Graph showing Gain vs. Total Drain Current for 71 GHz, 76 GHz, 81 GHz, and 86 GHz](#)

**Upper Tone Gain vs. Total Current @ VD = 4 V**

![Graph showing Gain vs. Total Drain Current for 71 GHz, 76 GHz, 81 GHz, and 86 GHz](#)

**Lower Tone Input IP3 vs. Total Current @ VD = 4 V**

![Graph showing Input IP3 vs. Total Drain Current for 71 GHz, 76 GHz, 81 GHz, and 86 GHz](#)

**Upper Tone Input IP3 vs. Total Current @ VD = 4 V**

![Graph showing Input IP3 vs. Total Drain Current for 71 GHz, 76 GHz, 81 GHz, and 86 GHz](#)

**Lower Tone Output IP3 vs. Total Current @ VD = 4 V**

![Graph showing Output IP3 vs. Total Drain Current for 71 GHz, 76 GHz, 81 GHz, and 86 GHz](#)

**Upper Tone Output IP3 vs. Total Current @ VD = 4 V**

![Graph showing Output IP3 vs. Total Drain Current for 71 GHz, 76 GHz, 81 GHz, and 86 GHz](#)
Calibration Plane
All data was measured on die with 200 µm pitch probes. The calibration plane is at the middle of the through, 178.5 µm from the middle of the RF pad.

App Note [1] Biasing -
All gates should be pinched-off \( (V_G < -1 \text{ V}) \) before applying drain voltage \( (V_D = 4 \text{ V}) \). Then the gate voltages can be increased until the desired quiescent drain current is reached in each stage. The recommended quiescent bias is \( V_D = 4 \text{ V}, I_D1 = 30 \text{ mA}, I_D2 = 60 \text{ mA}, I_D3 = 120 \text{ mA} \) and \( I_D4 = 150 \text{ mA} \). The performance in this datasheet has been measured with the gate bias set to the voltage that gives the stated value of the quiescent current. It is also possible to regulate the drain current dynamically, to limit the DC power dissipation under RF drive. To turn off the device, the turn on bias sequence should be followed in reverse.

App Note [2] Bias Arrangement -
Each DC pin \( (V_G1,2,3,4 \text{ and } V_D1,2,3,4) \) needs to have bypass capacitance \( (120 \text{ pF and 10 nF}) \) mounted as close to the MMIC as possible.

App Note [3] Wire Bonding -
The loop height of the RF bonds should be minimized. Where the die is mounted above the PCB, it is recommended to use Reverse Ball-Stitch-on-Ball bonds (BSOB). If the die is mounted inside a cavity on the board, Forward Loop bonding may result in a lower loop height.

V-shape RF bond with two wires \( (\text{diameter} = 25 \text{ µm}) \) is recommended for optimum RF performance.

RF bond wire length to be minimized to reduce the inductance effect. Simulations suggest no more than 300 µm. Substrate RF pad can be optimized to improve the Microstrip to MMIC bond transition as shown in the example below.
App Note [4] Detector biasing schematic -
As shown in the schematic below, the power detector is biased by matched 120 kΩ resistors to a 5 V bias. The difference voltage between V\text{DET} and V\text{REF} pins can be obtained using the op-amp differencing circuit shown below.

![Schematic Diagram]

### Layout Dimensions

- **Die Thickness**: 50µm
- **RF Pads**: 60 x 120µm²
- **DC Pads**: 100 x 100µm²
Assembly Diagram