GaN Low Noise Amplifier
8 - 12 GHz

MAAL-FR1250
Rev. V1

Features

- Gain: 24 dB
- Noise: 1.4 dB
- Output P1dB: 19.5 dBm @ 10 GHz
- Output Saturated Power: 21 dBm @ 10 GHz
- Power Consumption: 1.2 W
- Voltage: +8 V
- Lead-Free 5 mm QFN - 24 Leads

Applications

- Satellite Communication
- Radar

Description

The MAAL-FR1250 is a 3-stage low noise amplifier (LNA) designed to operate from 8 - 12 GHz with 1.4 dB of noise figure and 24 dB of gain at 10 GHz. This LNA is matched to 50 Ω at both input and output ports.

The MAAL-FR1250 has a single positive voltage bias which includes a DC current regulation. This device is ideally suited to satellite communication and radar applications.

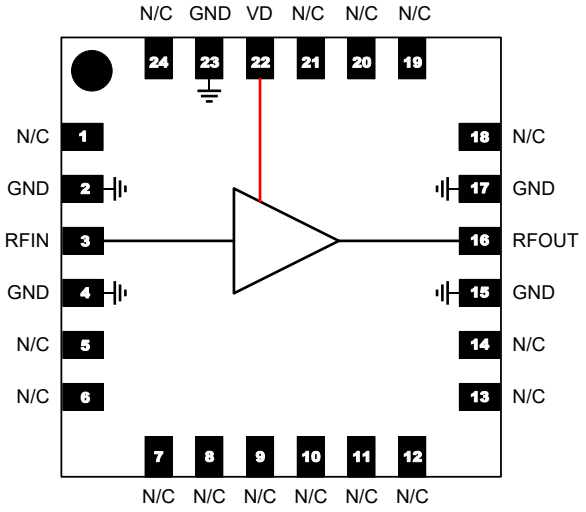
The MAAL-FR1250 is manufactured using a high performance 100 nm gate length GaN on Si HEMT power technology. The MMIC uses gold bonding pads and backside metallization and is protected with silicon nitride passivation to obtain the highest level of reliability.

Ordering Information[1,2]

Part Number	Package
MAAL-FR1250	Bulk
MAAL-FR1250-TR0500	500 part reel
MAAL-FR1250-001SMB	Sample Board

1. Reference Application Note M513 for reel size information.
2. MAAL-FR1250 also exists in die form: MAAL-011250-DIE.

Functional Schematic



Pin Configuration[3]

Pin #	Function
1,5,6,7,8,9,10,11,12,13,14,18,19,20, 21,24	No Connection
2,4,15,17,23	Ground
3	RFIN
22	VD
16	RFOUT
-	Paddle[4]

3. MACOM recommends connecting unused package pins to ground.
4. The exposed pad centered on the package bottom must be connected to RF and DC ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications: Freq. = 8 - 12 GHz, T_A = +25°C, V_D = +8 V, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	—	dB	19	24	—
Input Return Loss	—	dB	—	-10	—
Output Return Loss	—	dB	—	-10	—
Noise Figure	—	dB	—	1.4	2.2
Drain Current	—	mA	—	150	—
Output P1dB	@ 10 GHz	dBm	—	19.5	—
Output Saturated Power	@ 10 GHz	dBm	—	21	—
Output IP3	Tone Spacing ∆f = 1 MHz @ 10 GHz	dBm	—	32	—

Absolute Maximum Ratings[5,6]

Parameter	Absolute Maximum
Input RF port (1 minute at CW)	33 dBm
Operating Voltage	20 V
Junction Temperature[7,8]	+200°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-40°C to +150°C

5. Exceeding any one or combination of these limits may cause permanent damage to this device.
6. MACOM does not recommend sustained operation near these survivability limits.
7. Operating at nominal conditions with $T_J \leq$ +200°C will ensure MTTF > 1 x 10^9 hours.
8. Junction Temperature (T_J) = T_C + Θjc * (V * I)
   Typical thermal resistance (Θjc) = 31.6 °C/W.
   a) For T_C = +25°C,
   T_J = 62.9 °C @ 8 V, 150 mA
   b) For T_C = +85°C,
   T_J = 129.9 °C @ 8 V, 145 mA

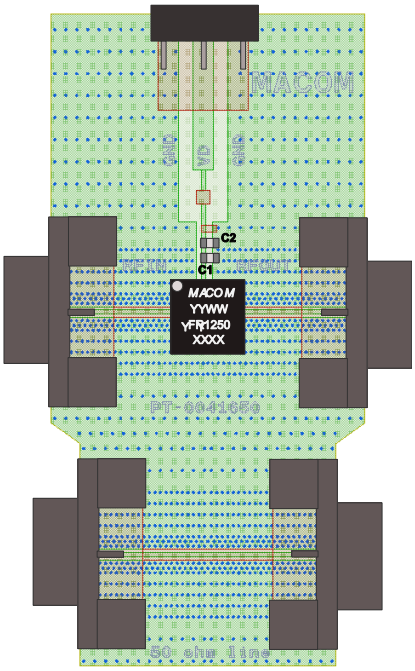
Handling Procedures

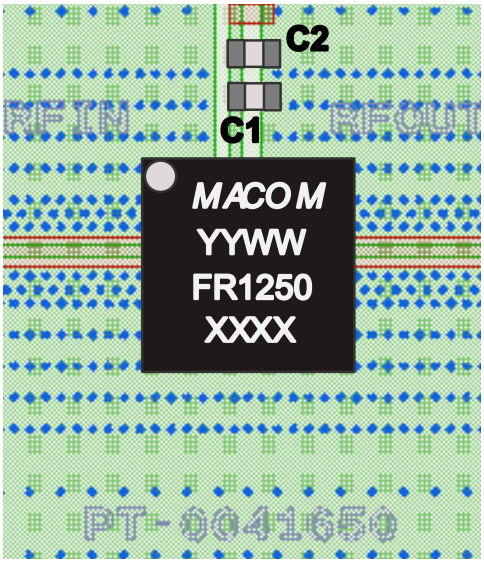
Please observe the following precautions to avoid damage:

Static Sensitivity

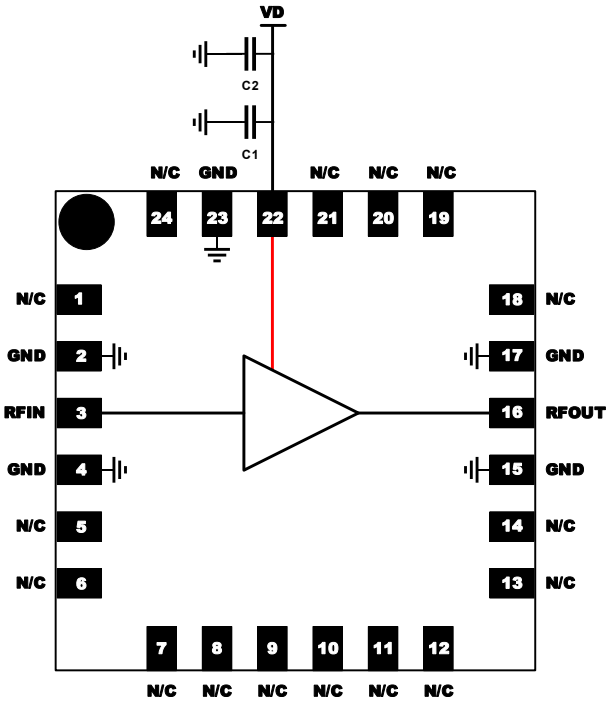
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

PCB Layout





Application Schematic

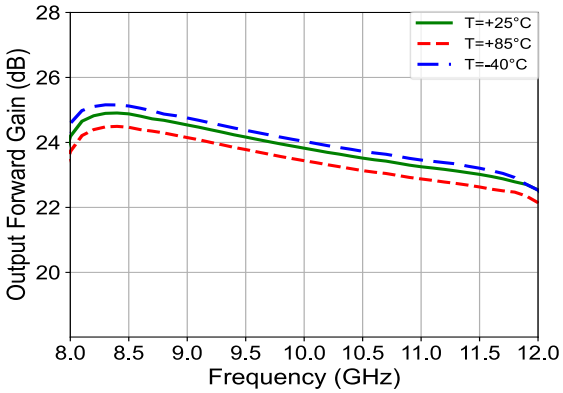


Parts List

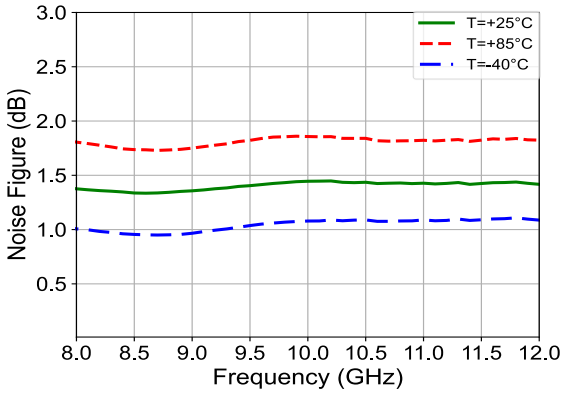
Part	Value	Case Style	Manufacturer	Manufacturer's Part number
C1	10 nF	0402	KYOCERA AVX	0402YC103JAT2A
C2	1 µF	0402	KYOCERA AVX	0402YD105KAT4A

Typical Performance Curves: @ PCB level with De-Embedding
V_D = 8 V, I_D = 150 mA

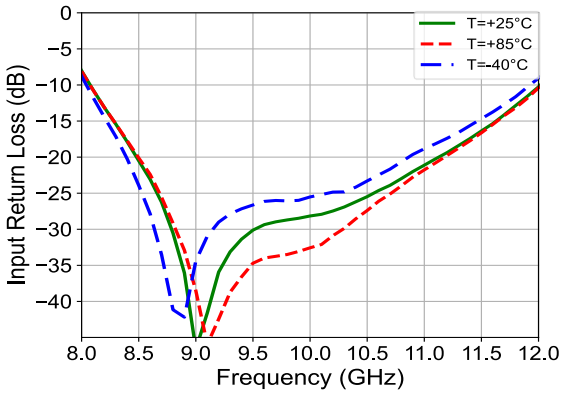
Gain vs. Frequency over Temperature



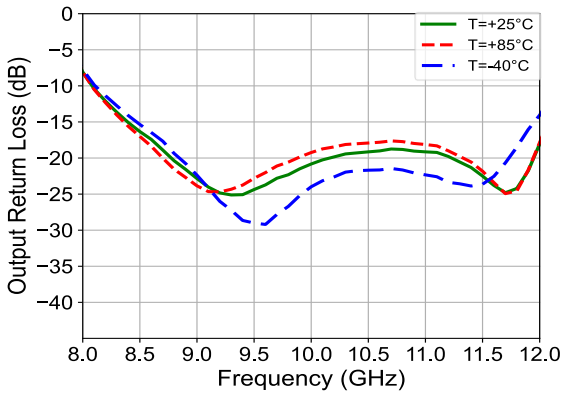
Noise Figure vs. Frequency over Temperature



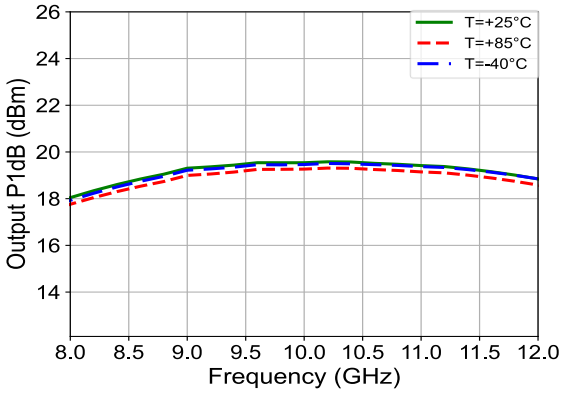
Input Return Loss vs. Frequency over Temperature



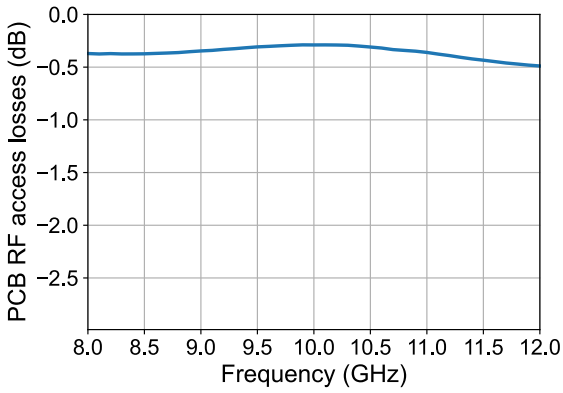
Output Return Loss vs. Frequency over Temperature



Output P1dB vs. Frequency over Temperature

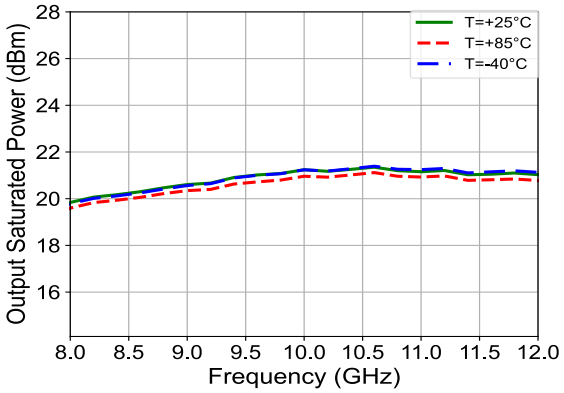


PCB RF Access Loss vs. Frequency

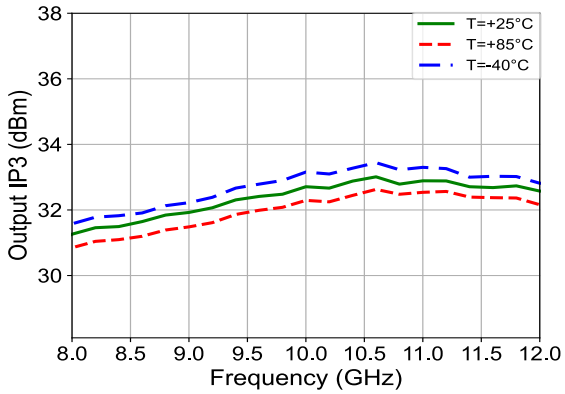


Typical Performance Curves: @ PCB level with De-Embedding
VD = +8 V, I_D = 150mA

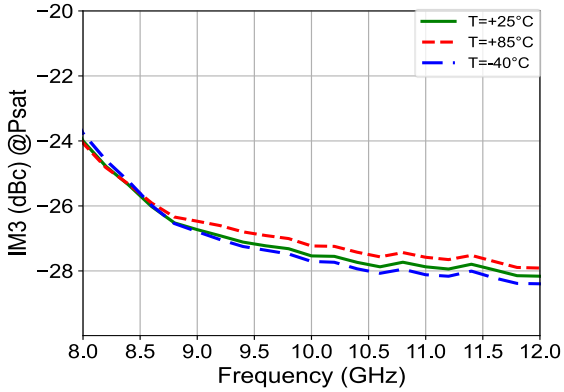
Saturated Power vs. Frequency over Temperature



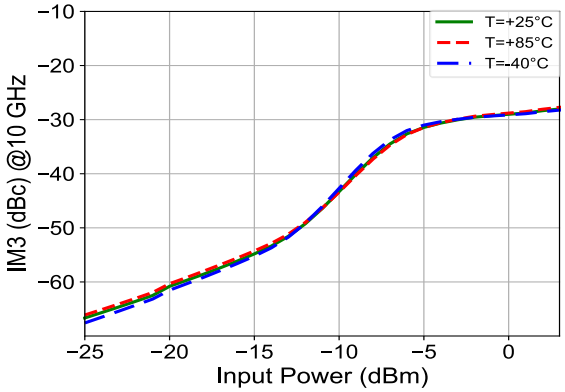
Output IP3 vs. Frequency over Temperature



Three Order Intermodulation vs. Frequency over Temperature



Three Order Intermodulation vs. Input Power over Temperature

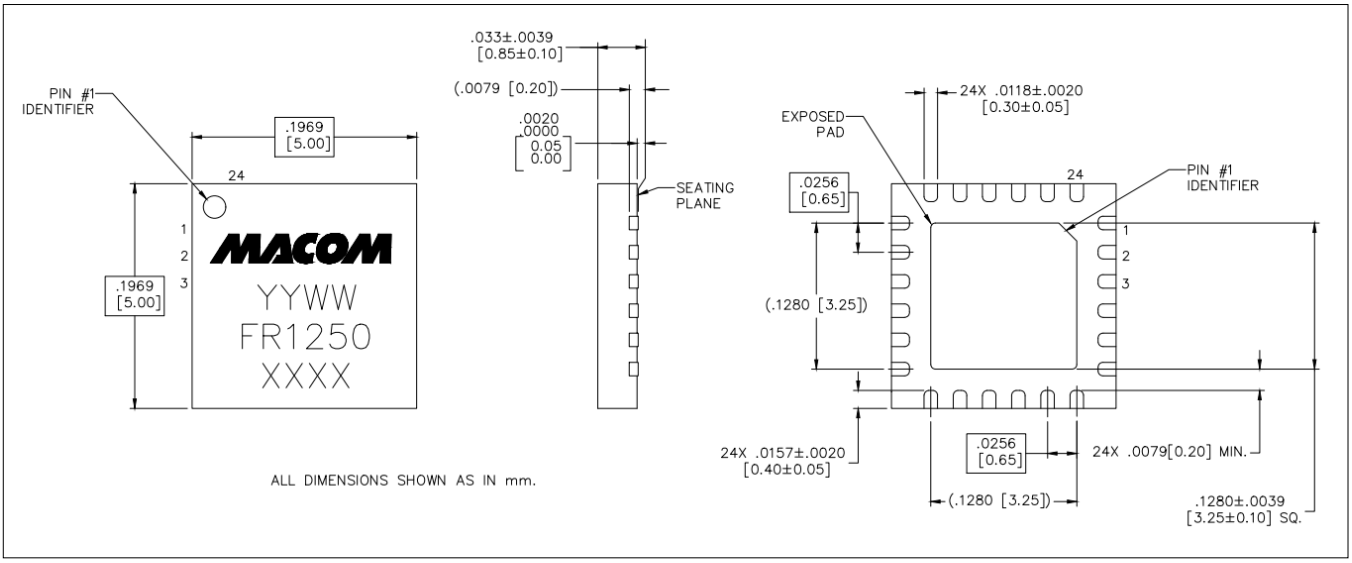


Biasing Procedure

Biasing UP
Set I_D limit to 200 mA.
Ensure voltages are at 0 before turning on DC supply.
Set V_D to +8 V.
Ensure I_D ≈ 150 mA.

Biasing Down
Set V_D to 0 V.
Turn off DC supply.

Lead-Free 5 mm 24-Lead PQFN†



† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 1 requirements.
Plating is 100% matte tin over copper.

Revision History

Rev	Date	Change description
V1	27/08/25	Initial Release