Low Noise Amplifier
5 - 6 GHz

MAAL-FR0004
Rev. V1

Features

- Gain: 28 dB
- Output P1dB: 14.7 dBm
- Noise Figure: 1.25 dB
- Reverse isolation: 50 dB
- Input return Loss: -17 dB
- Output return Loss: -15 dB
- Lead-Free 4 mm 24-Lead PQFN
- RoHS* Compliant

Applications

- C-Band Active antennas
- General Purpose

Description

The MAAL-FR0004 is a high gain, low noise figure MMIC amplifier operating from 5 to 6 GHz designed for use with the integrated core chip, attenuator/ phase shifter chip set or as general purpose low noise amplifier in band C and packaged in a 4 mm 24-lead Plastic QFN.

MAAL-FR0004 uses a simple external matching circuit to provide excellent input matching between 5 and 6 GHz.

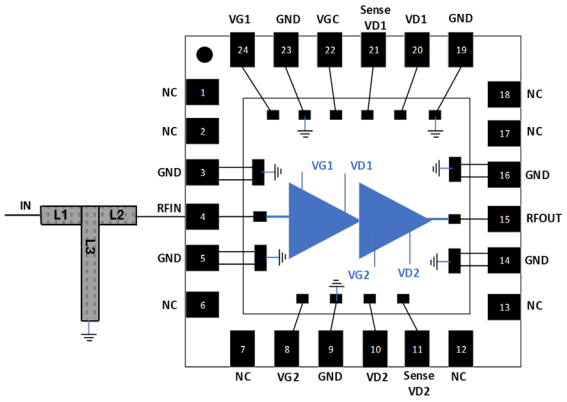
The MMIC is manufactured with a 0.18 µm PHEMT GaAs MMIC technology.

Ordering Information[1,2]

Part Number	Package
MAAL-FR0004-TR0500	500 Part Reel
MAAL-FR0004-001SMB	Sample Board

1. Reference Application Note M513 for reel size information.
2. MAAL-FR0004 also exists in die form: CGY2178UH/C1.

Functional Schematic



Pin Configuration[3,4]

Pin #	Function	Description
1,2,6,7,12, 13,17,18	NC	Not Connected
3,5,9,14, 16,19,23	GND	Ground
4	RFIN	RF Package Input
8	VG2	Gate Supply 2
10	VD2	Drain Supply 2
11	Sense VD2	Possibility to Sense VD2
15	RFOUT	RF Output
20	VD1	Drain Supply 1
21	Sense VD1	Possibility to Sense VD1
22	VGC	Cascode Bias Stage 1
24	VG1	Gate Supply 1
Paddle	GND[4]	Ground Paddle

3. MACOM recommends connecting unused package pins to ground.
4. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

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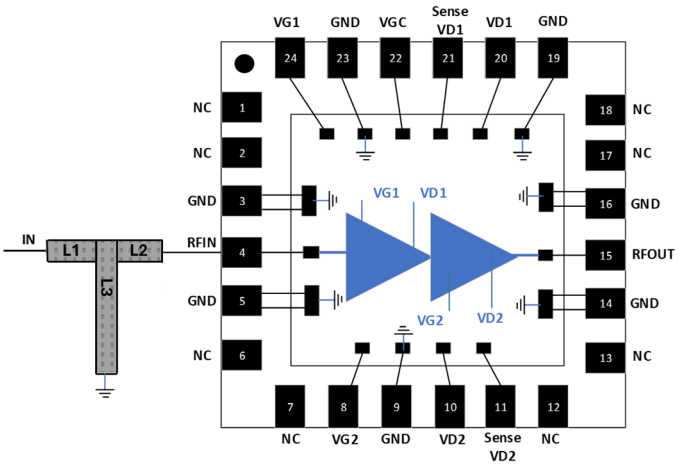
Pin Configuration and Functional Descriptions



Pin #	Pin Name	Description
1,2,6,7,12,13,17,18	NC	These pins are not connected internally. It is recommended these are grounded on the application PCB.
3,5,9,14,16,19,23	GND	Pins connected to GND
4	RFIN	RF Signal Input. This pad is matched to 50 Ω using an external T-matching circuit and is AC coupled.
8	VG2	Gate bias 2. For bypassing 100 nF capacitors are recommended.
10,11	VD2, Sense VD2	Drain bias 2. For bypassing 100 nF capacitors are recommended. Sense VD2 is connected internally to VD2, the purpose is to offer the possibility to sense VD2.
15	RFOUT	RF Signal Output. This pad is matched to 50 Ω and is AC coupled.
20, 21	VD1, Sense VD1	Drain bias 1. For bypassing 100 nF capacitors are recommended. Sense VD1 is connected internally to VD1, the purpose is to offer the possibility to sense VD1.
22	VGC	To bias the cascode of 1st stage, it should be connected to VD1 on the board.
24	VG1	Gate bias 1. For bypassing 100 nF capacitors are recommended.
Paddle	GND	RF, DC and thermal ground

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Electrical Specifications: Measured on Reference Board, Freq. = 5 - 6 GHz, Z_0 = 50 Ω, VD1 = VD2 = 3 V, T_A = 25°C, Quiescent Bias Currents (ID_1 = 10 mA ID_2 = 30 mA)

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	5.0 GHz 5.5 GHz 6.0 GHz	dB	28 26 24	30 28 26	—
Noise Figure	5.5 GHz	dB	—	1.25	1.6
Reverse Isolation	5.5 GHz	dB	—	45	—
Output P1dB	5.5 GHz @ P_{IN} = -12.3 dBm	dBm	—	14.7	—
Input Return Loss	5.5 GHz	dB	—	-17	—
Output Return Loss	5.5 GHz	dB	—	-15	—

Absolute Maximum Ratings[5,6]

Parameter	Absolute Maximum
Input Power	5 dBm
Gate Voltage	-6 to 0 V
Drain Voltage	0 to +6 V
Drain current	40 mA (stage 1) 60 mA (stage 2)
Gate current	10 mA
Junction Temperature[7,8]	+150 °C
Operating Temperature	-40 °C to + 85 °C
Storage Temperature	-55 °C to + 150 °C

5. Exceeding any one or combination of these limits may cause permanent damage to this device.
6. MACOM does not recommend sustained operation near these survivability limits.
7. Operating at nominal conditions with $T_J \leq +200°C$ will ensure MTTF > 1 x 10^9 hours.
8. Junction Temperature (T_J) = T_C + Θjc * (V * I)
   a) For T_C = +25°C,
   Typical thermal resistance (Θjc) = 116.06 °C/W.
   T_J = 35.4 °C @ 3 V, 30 mA
   b) For T_C = +85°C,
   Typical thermal resistance (Θjc) = 139.11 °C/W.
   T_J = 97.5 °C @ 3 V, 30 mA

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Operating the MAAL-FR0004

Turn-on

1. Apply VG1 = VG2 = -1.5 V
2. Increase VD1 = VD2 to 3 V.
3. Set ID1 = 10 mA and ID2 = 30 mA by adjusting VG1 and VG2 more positive.
4. Apply RFIN signal.

Turn-off

1. Remove RFIN signal.
2. Decrease VG1 and VG2 to -1.5 V
3. Decrease VDD to 0 V.

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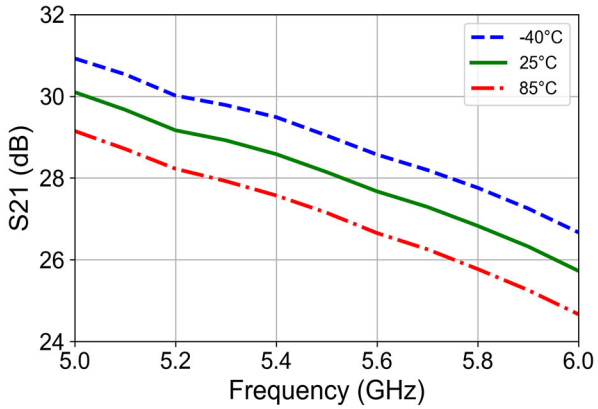
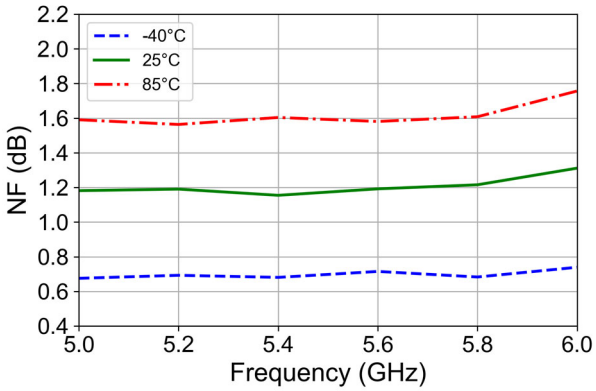
Typical Performance Curves: @ PCB level with De-Embedding, VD1 = VD2 = 3 V, TA = 25°C, Quiescent Bias Currents (ID_1 = 10 mA ID_2 = 30 mA)

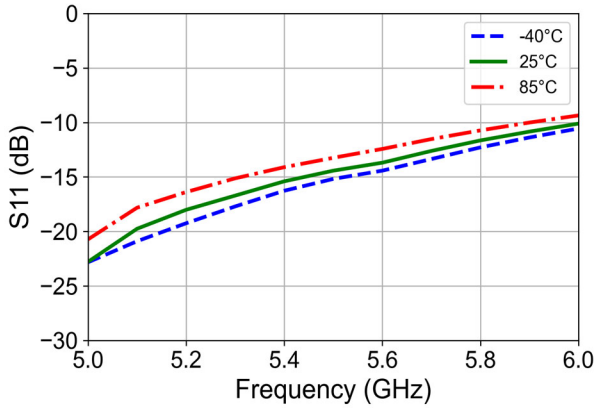
Gain over Frequency



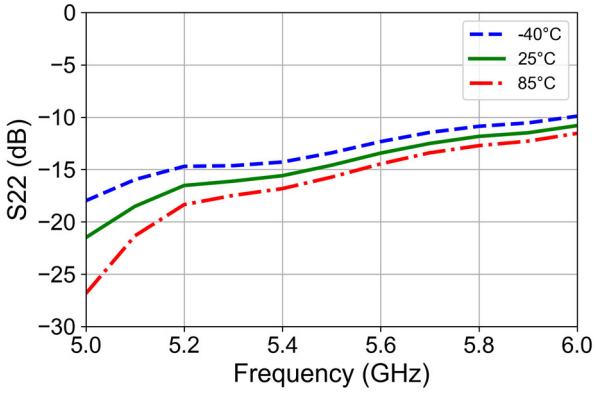
Noise Figure over Frequency



Input Return Loss over Frequency



Output Return Loss over Frequency



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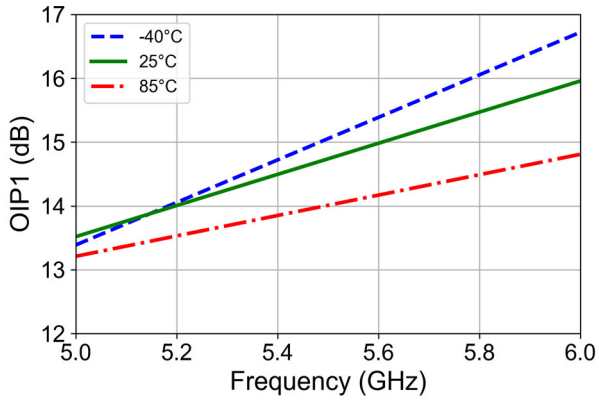
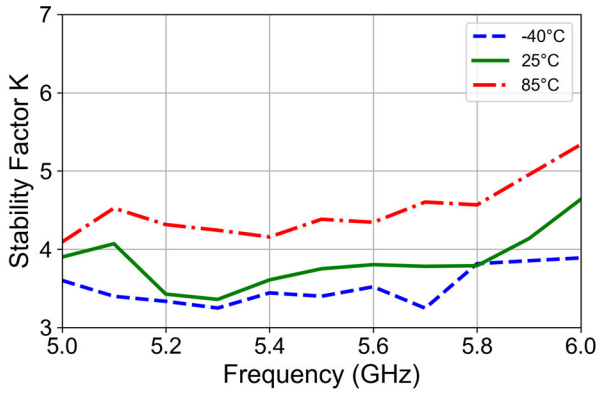
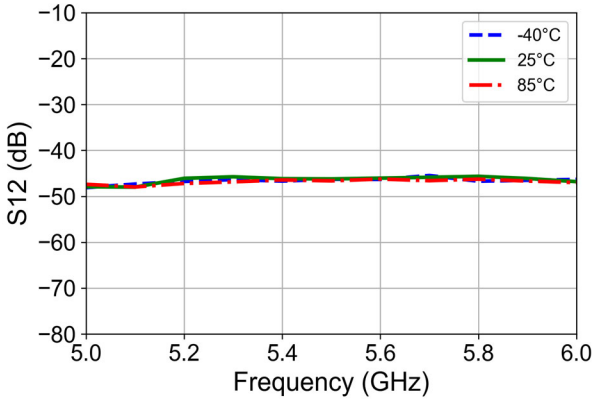
Output 1dB Compression Power over Frequency



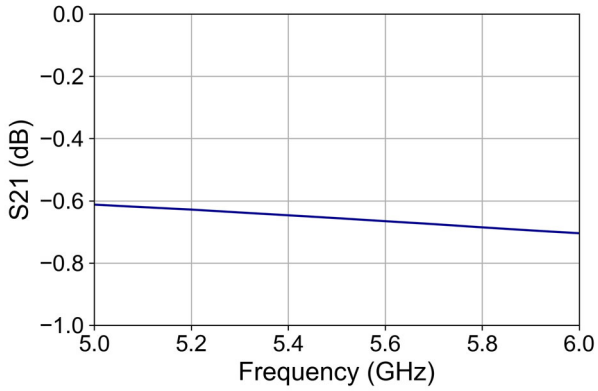
Stability Factor over Frequency



Reverse Isolation over Frequency



Access Line & Connector Losses over Frequency



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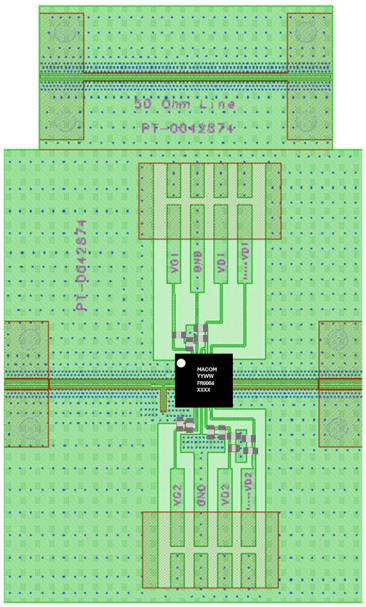
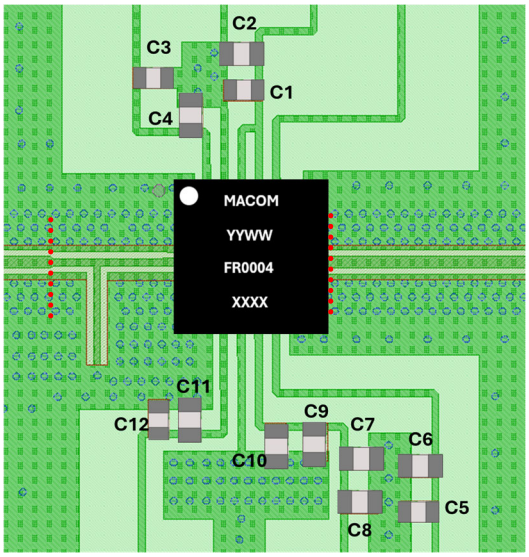
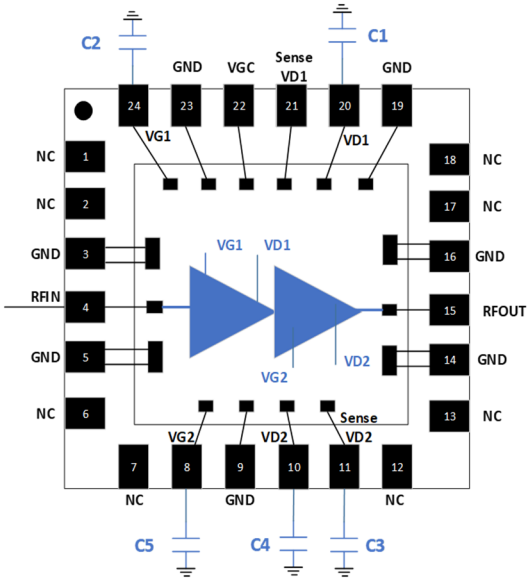
Reference Board

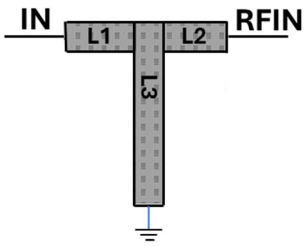




Red dashed lines indicate the reference planes at RFIN and RFOUT.

Application Schematic





Dimensions are given for Rogers RO4003 substrate material. (Height = 185 µm, Er = 3.4)

Component	Length (µm)	Width (µm)	Gap (µm)
L1	1170	200	200
L2	1603	200	200
L3	3033	200	200

Part	Value	Case Style	Manufacturer	Manufacturer's Part #
C1, C3, C5, C8, C12	100 nF	0402	KYOCERA AVX	0402YD104KAT2A
C2, C4, C6, C7, C9, C10, C11	NA	0402	NA	NA

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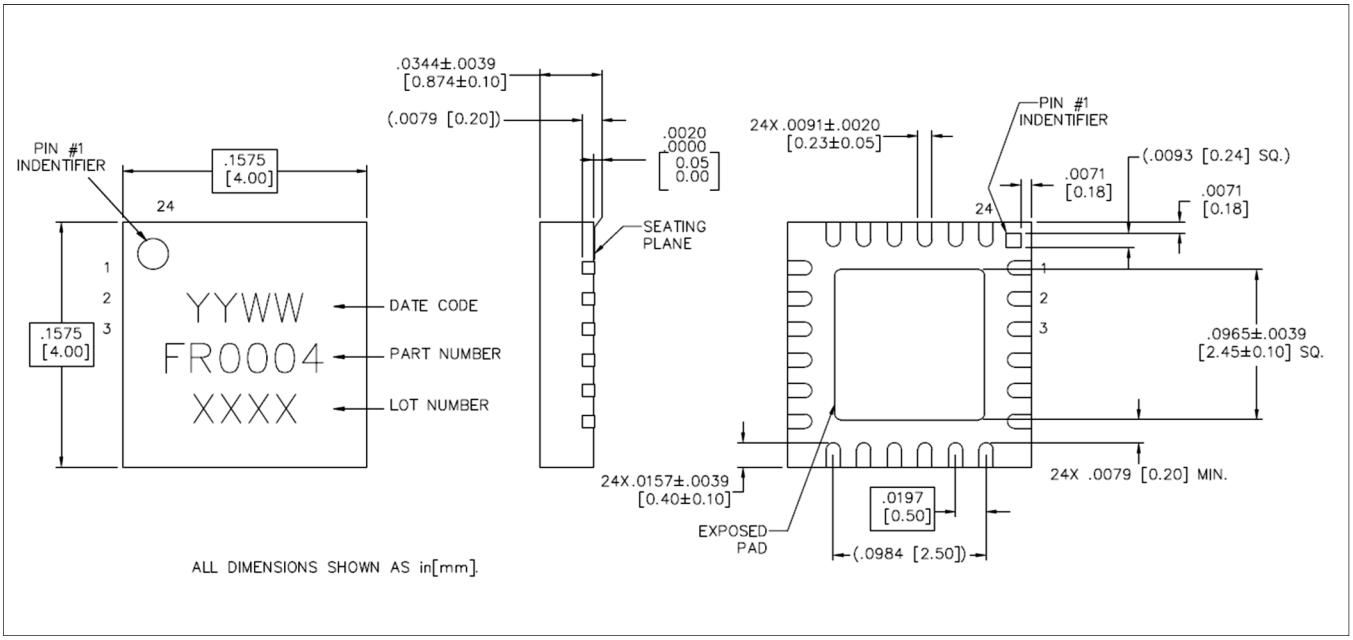
Lead-Free 4 mm 24-Lead PQFN



† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 1 requirements.
Plating is 100% matte tin over copper.

Revision History

Rev	Date	Change Description
V1	12/12/25	Initial Release

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