Features

- Single stage LNA with Bypass function
- Broadband: 1400 - 6000 MHz
- Gain:
  - 18.1 dB @ 1400 MHz
  - 16.3 dB @ 2500 MHz
  - 14.6 dB @ 4200 MHz
- Noise Figure:
  - 0.72 dB @ 1400 MHz
  - 0.85 dB @ 2500 MHz
  - 1.11 dB @ 4200 MHz
- Output P1dB: 18 dBm
- Output IP3: 32 dBm
- Bypass (BP) mode:
  - Insertion Loss: 0.7 dB
  - Input P0.1dB: 28 dBm
- Single 5 V Supply
- Low DC Current: 55 mA
- Integrated Control Circuitry with 1.8/3.3 V Logic
- Lead-Free 2 mm 8-Lead DFN Package
- RoHS* Compliant

Applications

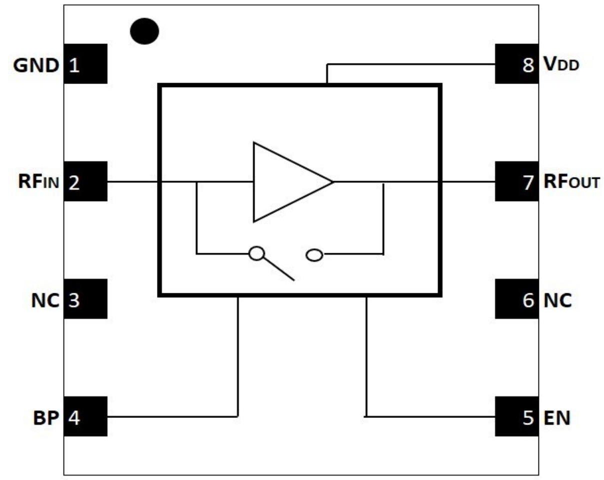
- 5G Base Stations
- Wireless Infrastructure
- General purpose wireless
- TDD or FDD systems

Description

The MAAL-011287 is a low noise amplifier (LNA) with Bypass function designed to operate from 1400 to 6000 MHz in a lead-free 2 mm 8-LD DFN plastic package.

This LNA features low noise figure, high linearity and low power consumption. The MAAL-011287 has an integrated active bias circuit to minimize variations over temperature and process and the ability to switch between LNA and bypass modes. It requires a single 5 V supply and the internal digital logic is 1.8/3.3 V CMOS compatible.

Functional Schematic



Pin Function[1]

Pin #	Pin Name	Description
1	GND	Ground
2	RF_{IN}	Input Port
3, 6	NC	No Connection
4	BP	Bypass Logic Control
5	EN	Enable Logic Control
7	RF_{OUT}	Output Port
8	V_{DD}	Supply Voltage
9	Paddle[2]	Ground

1. MACOM recommends connecting unused package pins to ground.
2. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

Ordering Information[3]

Part Number	Package
MAAL-011287-TR1000	1000 piece reel
MAAL-011287-001SMB	Sample Board

3. Reference Application Note M513 for reel size information.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Pin Description

Pin #	Name	Description
1	GND	Ground pin. This pin must be connected to RF/DC ground.
2	RF_{IN}	RF Input. DC blocking capacitor required at this pin.
3, 6	NC	Not connected internally. Recommend to be connected to RF/DC ground.
4	BP	Bypass logic control. Internally pulled down.
5	EN	Enable logic control. Internally pulled down.
7	RF_{OUT}	RF Output. DC blocking capacitor required at this pin.
8	V_{DD}	Supply voltage. DC decoupling capacitors required at this pin.
9	Paddle	Exposed Pad. The exposed pad must be connected to RF, DC and thermal GND.

AC Electrical Specifications:
Freq = 2.5 GHz, P_{IN} = -30 dBm, V_{DD} = 5 V, Z_0 = 50 Ω, T_C = +25ºC

Parameter	Test Conditions	Units	Min.	Typ.	Max.
LNA Gain	1400 MHz 2500 MHz 4200 MHz	dB	— — 13.0	18.1 16.3 15.0	—
LNA Noise Figure	1400 MHz 2500 MHz 4200 MHz	dB	—	0.72 0.85 1.11	—
LNA Output IP3	P_{IN}/tone = -18 dBm, Tone Delta = 2 MHz	dBm	—	32	—
LNA Output IP2	P_{IN}/tone = -18 dBm, Tone Delta = 2 MHz	dBm	—	36.5	—
LNA Output P1dB	—	dBm	—	18	—
LNA Input Return Loss	—	dB	—	17	—
LNA Output Return Loss	—	dB	—	21	—
LNA Reverse Isolation	RF_{OUT} to RF_{IN}	dB	—	24	—
Bypass Insertion Loss	2500 MHz 4200 MHz	dB	—	0.7 0.75	— 1.4
Bypass Input Return Loss	—	dB	—	24	—
Bypass Output Return Loss	—	dB	—	25	—
Bypass Input P0.1dB	—	dBm	—	28	—
Bypass Input IP3	Bypass Mode, P_{IN}/tone = +3 dBm, Tone Delta = 2 MHz	dBm	—	42.5	—

DC Electrical Specifications: V_{DD} = 5 V, Z_0 = 50 Ω, T_C = +25ºC

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Supply Voltage	—	V	4.75	5	5.25
Supply Current	LNA Mode BP Mode OFF	mA	—	55 0.6 0.6	—
EN Logic Input Voltage	LNA/BP Mode OFF	V	0 1.2	—	0.6 3.45
BP Logic Input Voltage	LNA Mode BP Mode	V	0 1.2	—	0.6 3.45
EN Logic Input Current	LNA/BP Mode OFF	µA	— 0	-4 40	— 80
BP Logic Input Current	LNA Mode BP Mode	µA	— 0	-4 40	— 80

Transient Electrical Specifications:
Freq. = 2.5 GHz, P_{IN} = -30 dBm, T_C = 25°C, V_{DD} = 5 V, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
BP Speed	LNA to BP mode 50% of Vctrl to final power - 0.1 dB	µs	—	0.4	—
	BP to LNA mode 50% of Vctrl to final power - 0.1 dB	µs	—	0.4	—
Power Down	LNA ON to OFF 50% of Vctrl to 5% of RF signal	µs	—	0.1	—
	LNA OFF to ON 50% of Vctrl to final power - 0.1 dB	µs	—	0.4	—

Control Truth Table

Mode	Enable	Bypass	Description
LNA mode	Logic Low or Open	Logic Low or Open	LNA ON, Bypass SW Open
BP mode	Logic Low or Open	Logic High	LNA OFF, Bypass SW Closed
OFF	Logic High	Logic Low or Open	LNA OFF, Bypass SW Open

Recommended Operating Conditions

Parameter	Operation Conditions
DC Supply V_{DD}	+4.75 to +5.25 V
Logic Control Voltage	0 to + 3.3 V
Case Temperature (T_C)[4]	-40°C to +105°C

4. Operating/Case temperature (T_C) is the temperature of the exposed paddle.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these Human Body Model (HBM) Class 1B and Charge Device Model (CDM) Class C3 devices.

Power Supplies

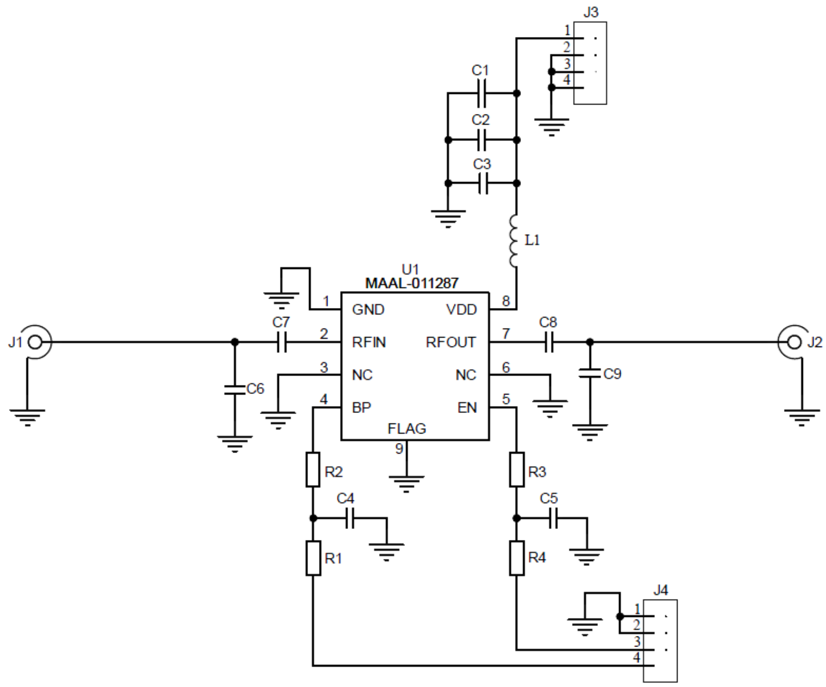
De-coupling capacitors should be placed at the V_{DD} supply pin to minimize noise and fast transients. Supply voltage change or transients should have a slew rate smaller than 1 V / 10 µs. In addition, all control pins should remain at 0 V (+/- 0.3 V) and no RF power should be applied while the supply voltage ramps or while it returns to zero.

Absolute Maximum Ratings[5,6]

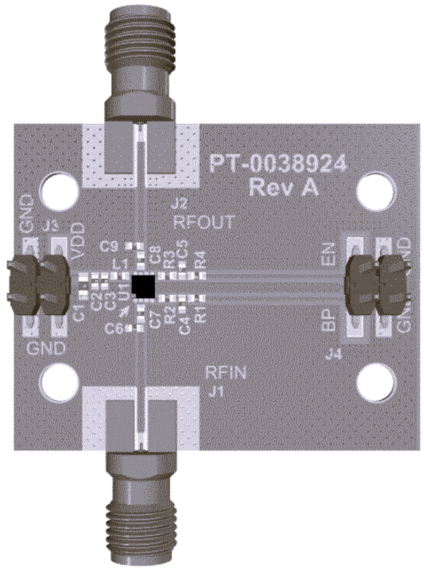
Parameter	Absolute Maximum
RF Input Power 2.5 GHz: LNA ON Mode	30 dBm CW
DC Supply V_{DD}	-0.5 to +5.5 V
Logic PD Control Voltage	-0.5 to +3.6 V
Junction Temperature[7,8] LNA ON Mode	+150°C
Storage Temperature	-55°C to +150°C

5. Exceeding any one or combination of these limits may cause permanent damage to this device.
6. MACOM does not recommend sustained operation near these survivability limits.
7. Operating at nominal conditions with T_J<150ºC (LNA ON Mode) will ensure MTTF >>$1x10^6$ hours
8. Junction Temperature (T_J) = T_C + Θ_{JC} * P_{DISS} where P_{DISS} is the total DC & RF dissipated power. Typical thermal resistance (Θ_{JC}) = 33.4ºC/W.
   a) For T_C = +25°C,
      T_J = 34°C @ 5 V, 55 mA
   b) For T_C = +105°C,
      T_J = 117°C @ 5 V, 70 mA

Applications Schematic
(As per MAAL-011287-001SMB)



Sample Board Layout

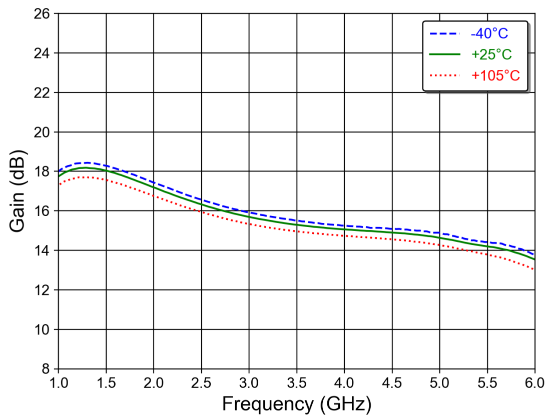


Parts list

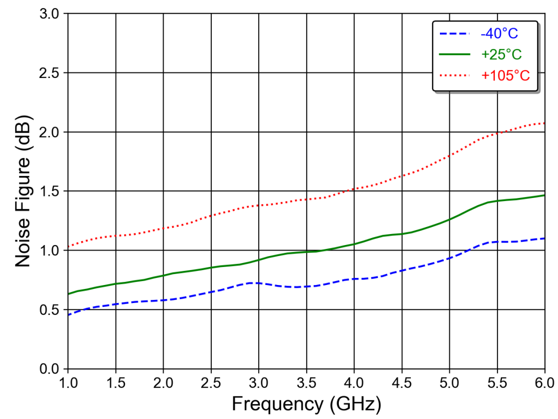
Schematic Component	Component Value	Size	Manufacturer
C1	10 µF	0603	Murata ZRB18AD71A106KE01
C2	10 nF	0402	Murata GRM155R71C103KA01D
C3	470 pF	0402	Murata GRM155R71H471KA01D
C4, C5	5 pF	0402	Kyocera CM05CG5R0B50AH
C6, C9	DNP	DNP	DNP
C7, C8	10 pF	0402	Murata GRM1555C1H100JA01D
L1	0 Ω	0402	Panasonic ERJ2GE0R00X
R1, R4	1 kΩ	0402	Yageo RC0402JR-071K
R2, R3	100 Ω	0402	Yageo RC0402JR-07100R

Typical Performance Curves: P_{IN} = -30 dBm, V_{DD} = 5 V, Z_0 = 50 Ω

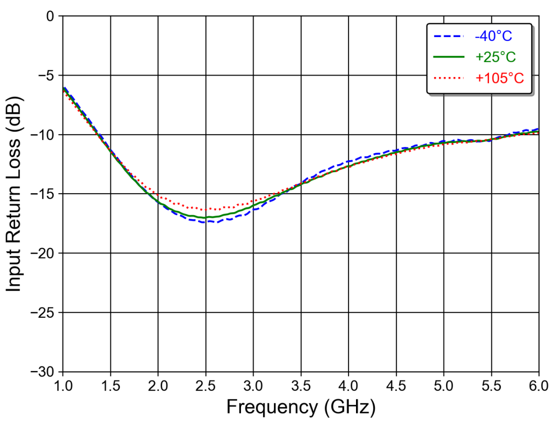
Gain[9]



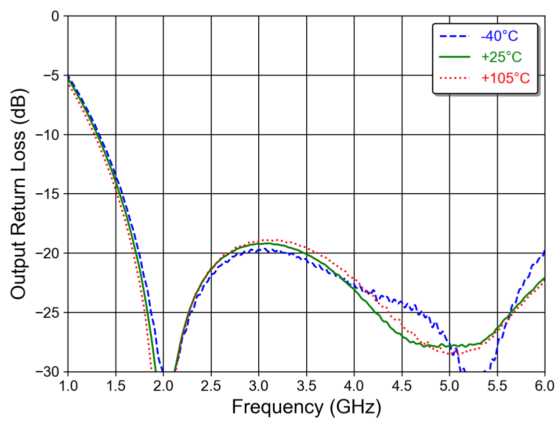
Noise Figure[9]



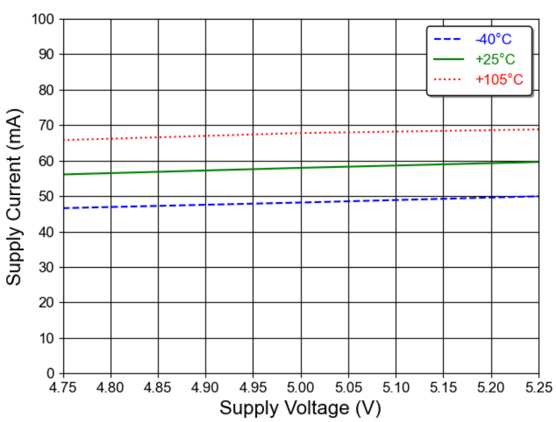
Input Return Loss



Output Return Loss



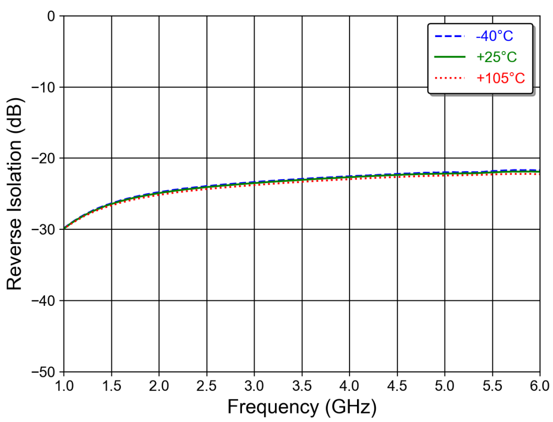
DC Current Over VDD and Temp



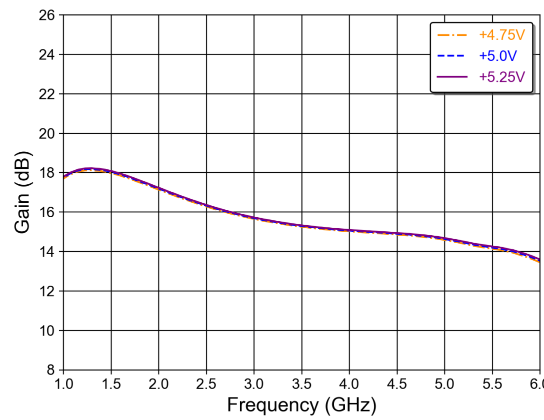
9. For gain, noise figure, reverse isolation, P1dB, IP3 and insertion loss plots, RF trace and connector losses are de-embedded.

Typical Performance Curves: P_{IN} = -30 dBm, V_{DD} = 5 V, Z_0 = 50 Ω

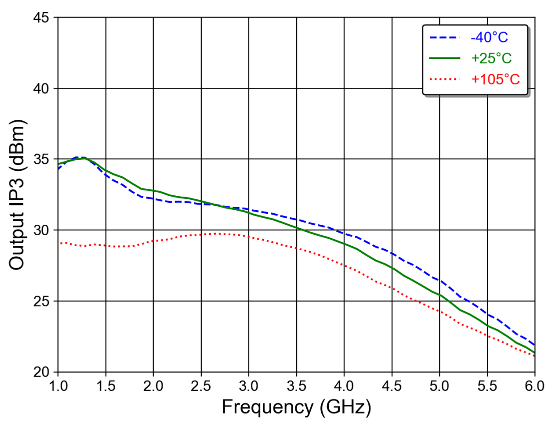
Reverse Isolation[9]



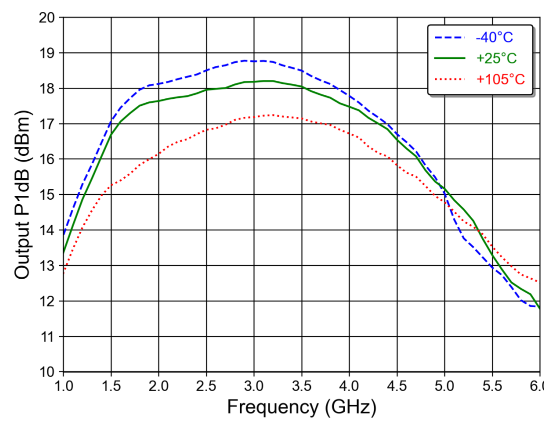
Gain[9] over Supply



Output IP3 (Pin = -18 dBm, Tone Delta = 2 MHz)[9]

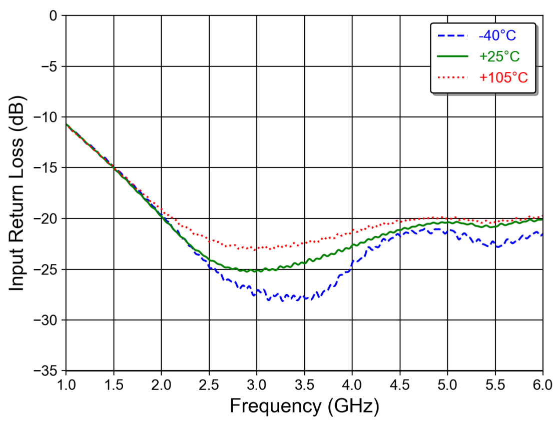


Output P1dB[9]

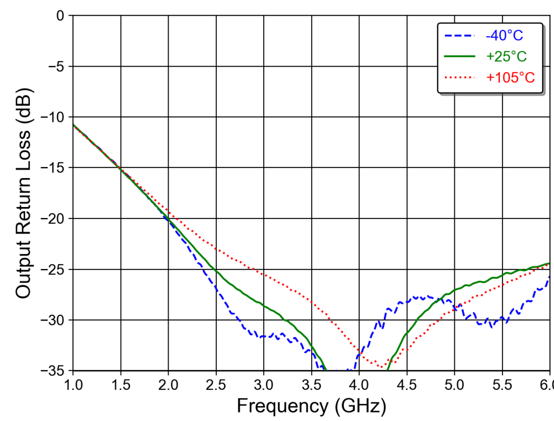


Typical Performance Curves: P_{IN} = -30 dBm, V_{DD} = 5 V, Z_0 = 50 Ω

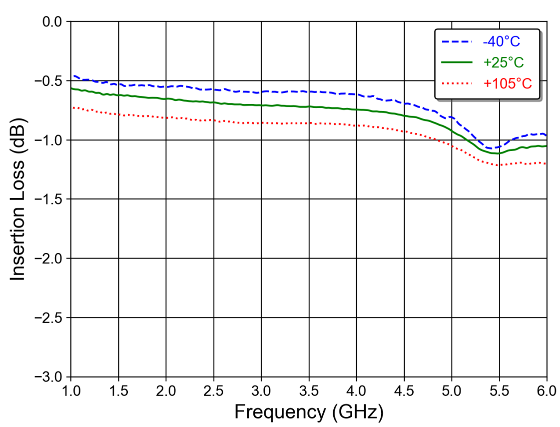
Bypass Input Return Loss



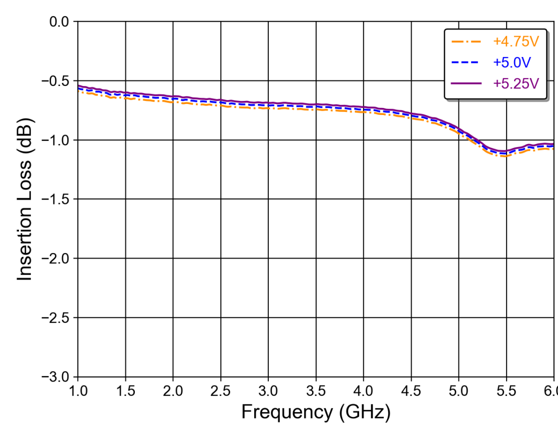
Bypass Output Return Loss



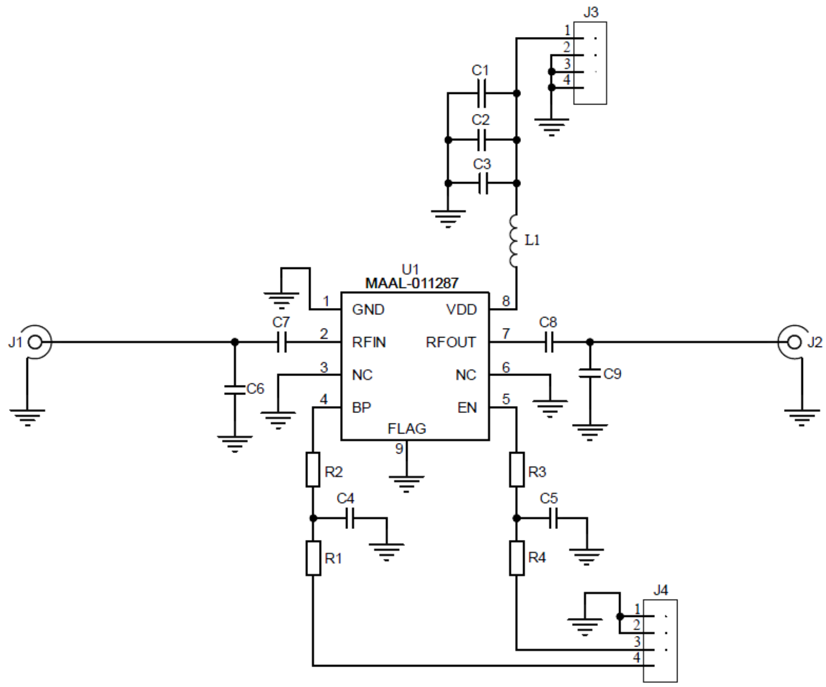
Bypass Insertion Loss[9]



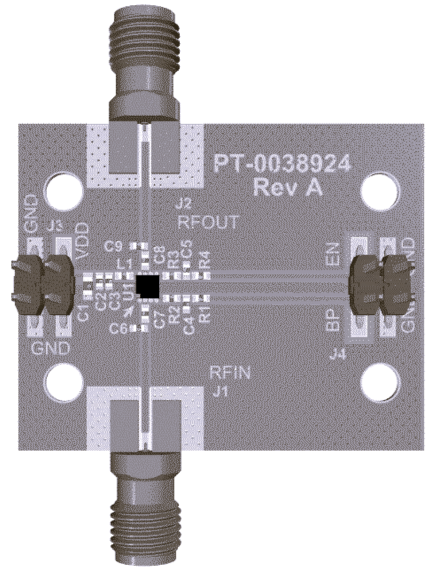
Bypass Insertion Loss over Supply[9]



Applications Section A: Matched for 4.4 - 5.0 GHz Band



Sample Board Layout



Parts list

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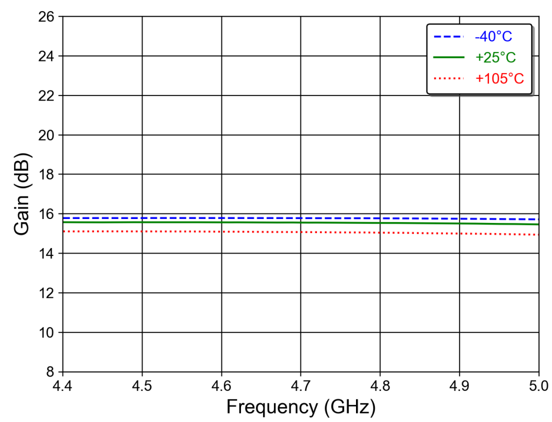
C2	10 nF	0402	Murata GRM155R71C103KA01D
C3	470 pF	0402	Murata GRM155R71H471KA01D
C4, C5	5 pF	0402	Kyocera CM05CG5R0B50AH
C6	0.2 pF	0402	Murata GJM1555C1HR20WB01
C7, C8	5.0 pF	0402	Murata GJM1555C1H5R0BB01
C9	DNP	DNP	DNP
L1	0 Ω	0402	Murata ERJ2GE0R00X
R1, R4	1 kΩ	0402	Yageo RC0402JR-071K
R2, R3	100 Ω	0402	Yageo RC0402JR-07100R

AC Electrical Specifications / Applications Section A: Matched for 4.4 - 5.0 GHz Band
Freq = 4.7 GHz, P_{IN} = -30 dBm, V_{DD} = 5 V, Z_0 = 50 Ω, T_C = +25ºC

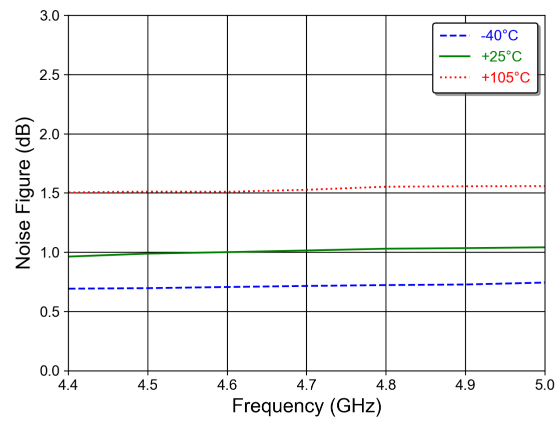
Parameter	Test Conditions	Units	Min.	Typ.	Max.
LNA Gain	—	dB	—	15.5	—
LNA Noise Figure	—	dB	—	1	—
LNA Output IP3	P_{IN}/tone = -18 dBm, Tone Delta = 2 MHz	dBm	—	26	—
LNA Output P1dB	—	dBm	—	16	—
LNA Input Return Loss	—	dB	—	18	—
LNA Output Return Loss	—	dB	—	18	—
LNA Reverse Isolation	RF_{OUT} to RF_{IN}	dB	—	22	—
Bypass Insertion Loss	—	dB	—	1.1	—
Bypass Input Return Loss	—	dB	—	12.5	—
Bypass Output Return Loss	—	dB	—	19	—

Typical Performance Curves (Matched for 4.4 - 5.0 GHz Band): Freq = 4.4 - 5.0 GHz, P_{IN} = -30 dBm, V_{DD} = 5 V, Z_0 = 50 Ω

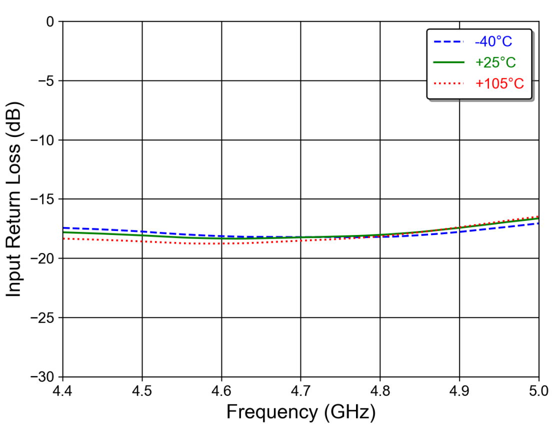
Gain[9]



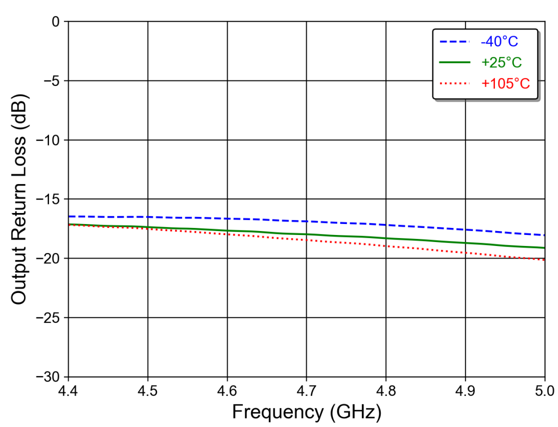
Noise Figure[9]



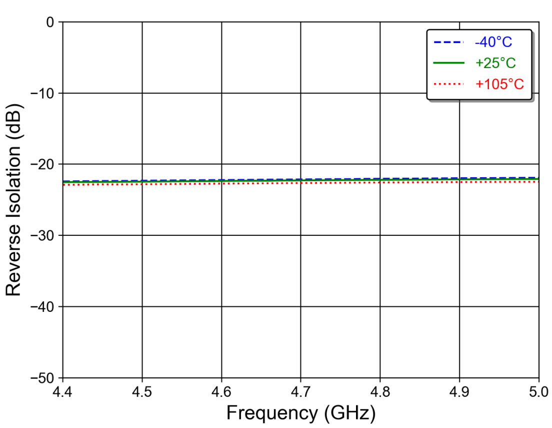
Input Return Loss



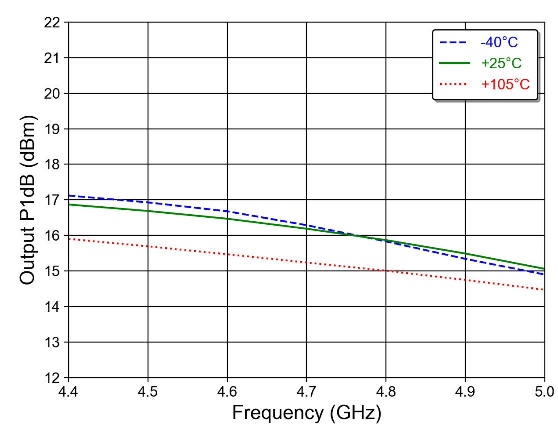
Output Return Loss



Reverse Isolation[9]

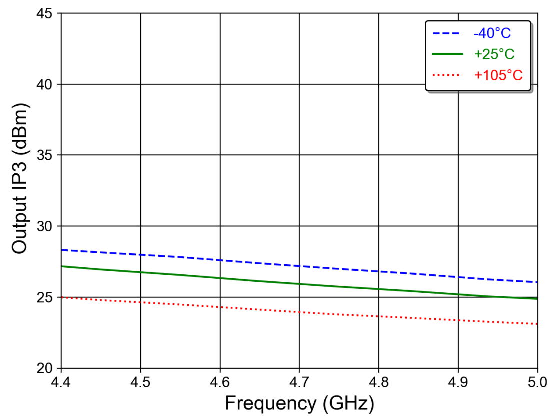


Output P1dB[9]

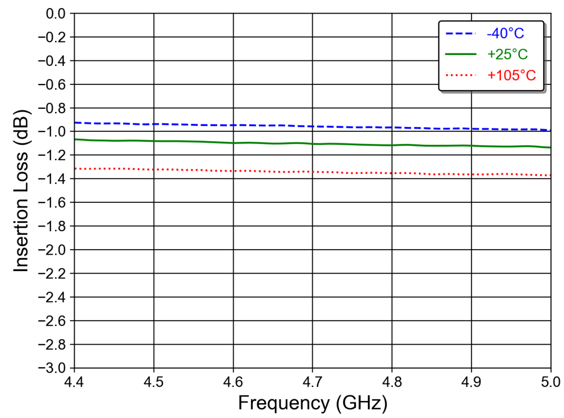


Typical Performance Curves (Matched for 4.4 - 5.0 GHz Band): Freq = 4.4 - 5.0 GHz, P_{IN} = -30 dBm, V_{DD} = 5 V, Z_0 = 50 Ω

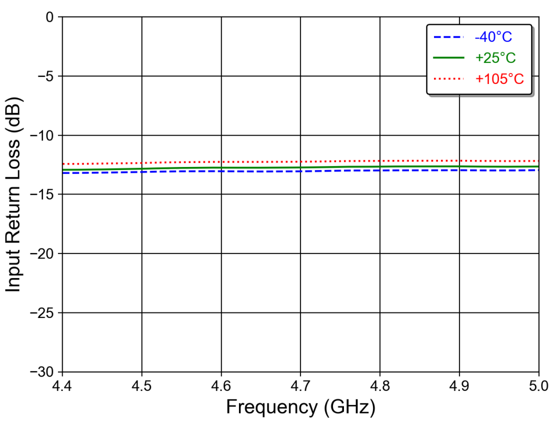
Output IP3 (Pin = -18 dBm, Tone Delta = 2 MHz)[9]



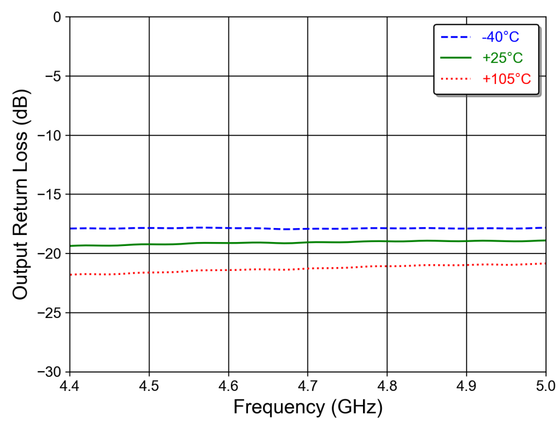
Bypass Insertion Loss[9]



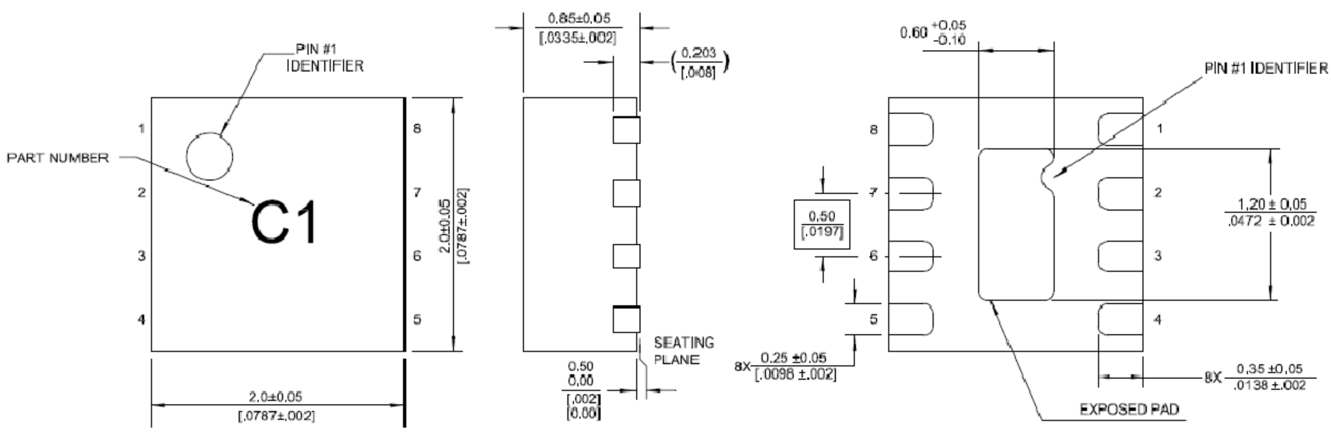
Bypass Input Return Loss



Bypass Output Return Loss



Lead-Free 2 mm 8-Lead DFN†



Notes:
1. Dimensions are in mm [in]
2. Reference JEDEC MO-220 for additional dimensional and tolerance information

† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 1 requirements in accordance to JEDEC J-STD-020D.
Plating is NiPdAu over Copper

Revision History

Rev	Date	Change Description
V1	June 2024	Initial Release