Features

- Wideband Performance
- Low Noise Figure: 3.2 dB
- Gain: 24 dB
- P_{SAT}: 22 dBm
- OIP3: 27 dBm
- Bias Voltage: V_{DD} = 3 V
- Bias Current: I_{DSQ} = 150 mA
- 50 Ω Matched Input and Output
- Die Size: 2.61 x 1.52 x 0.1 mm
- RoHS* Compliant

Applications

- Test and Measurement
- EW
- ECM
- Radar

Description

The MAAL-011229-DIE is an easy to use wideband low noise amplifier. It operates from 17 to 55 GHz and provides 3.2 dB noise figure, 24 dB gain and 22 dBm saturated output power. The input and output are fully matched to 50 Ω with typical return loss >12 dB.

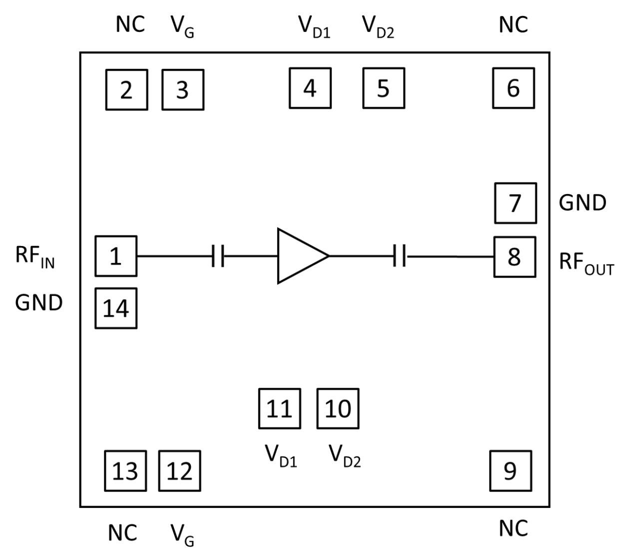
This product is fabricated using a GaAs pHEMT process which features full passivation for enhanced reliability.

The MAAL-011229-DIE can be used as a low noise amplifier stage or as a driver stage in higher power applications. All data in this datasheet is taken with 0.3 mm, 3 mil bond ribbon.

Ordering Information

Part Number	Package
MAAL-011229-DIE	Gel Pack
MAAL-011229-DIESB2	Sample Board

Functional Schematic



Pin Configuration[1]

Pin #	Function	Description
1	RF_{IN}	RF Input
2, 6, 9, 13	NC	Not Connected
3, 12	V_G	Gate voltage
4, 11	V_{D1}	Drain Supply One
5, 10	V_{D2}	Drain Supply Two
7, 14	GND	Ground
8	RF_{OUT}	RF Output

1. Backside of die must be connected to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

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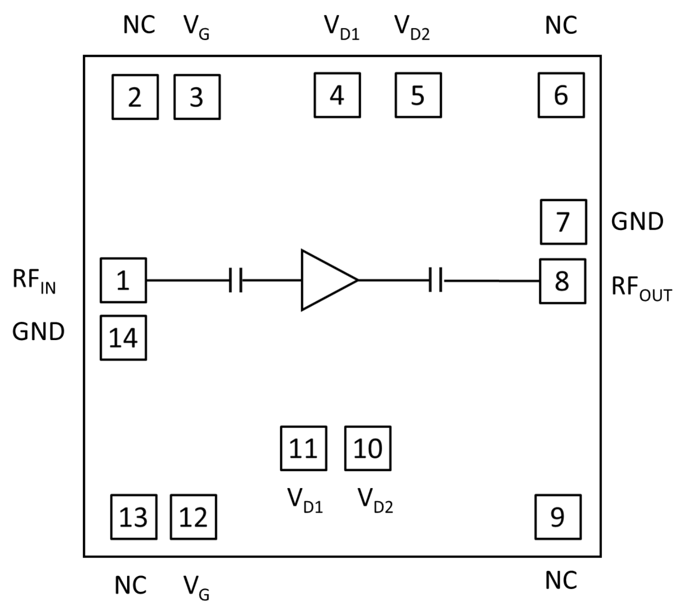
Pin Configuration and Functional Descriptions



Pin #	Pin Name	Description
1	RF_{IN}	RF Signal Input. This pad is matched to 50 Ω and is AC coupled.
2, 6, 9, 13	NC	These pads are connected to ground internally and are used from on-wafer testing in production. It is recommended these are not connected.
3, 11	V_G	Gate control voltage. Adjust from –1.5 V to 0 V to achieve the desired quiescent current. For bypassing 100 pF and 0.1 µF SMT capacitors are recommended. The 100 pF capacitor should be placed as closely to the package as physically possible. The positioning of the 0.1 µF capacitor is not as critical but should be placed as close as practically possible Pad 3 and 11 are connected. internally.
4, 10	V_{D1}	Drain bias 1. For bypassing 100 pF and 0.1 µF SMT capacitors are recommended. The 100 pF capacitor should be placed as closely to the package as physically possible. The positioning of the 0.1 µF capacitor is not as critical but should be placed as close as practically possible. Pads 4 and 10 are connected internally. Only one needs to be connected.
5, 9	V_{D2}	Drain bias 2. For bypassing 100 pF and 0.1 µF SMT capacitors are recommended. The 100 pF capacitor should be placed as closely to the package as physically possible. The positioning of the 0.1 µF capacitor is not as critical but should be placed as close as practically possible. Pads 5 and 9 are connected internally. Only one needs to be connected.
7, 14	GND	These pads are ground.
8	RF_{OUT}	RF Signal Output. This pad is matched to 50 Ω and is AC coupled

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AC Electrical Specifications: Freq. = 17 - 55 GHz, T_A = 25°C, V_{D1} = V_{D2} = 3 V, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Small Signal Gain	17 GHz 40 GHz 50 GHz	dB	21	25 27 24	—
Small Signal Gain Variation over Temperature	—	dB/°C	—	0.06	—
Gain Flatness	—	dB	—	±2	—
Noise Figure	25 GHz	dB	—	3.2	3.5
Input Return Loss	—	dB	—	12	—
Output Return Loss	—	dB	—	12	—
Saturated Output Power (P_{SAT})	17 GHz 40 GHz 50 GHz	dB	18 21 20	20 23 22	—
Output 3rd Order Intercept	—	dBm	—	27	—
Supply Current	—	mA	—	150	—

DC Electrical Specifications: V_{D1} , V_{D2} = 3 V, T_A = 25°C

Parameter	Test Conditions	Units	Min.	Typ.	Max.
DC Current: Quiescent (I_{DQ}) Drain (I_{DD}) Gate (I_{GS})	P_{OUT} = 0 dBm P_{OUT} = 22 dBm @ 50 GHz P_{OUT} = 22 dBm @ 50 GHz	mA	—	150 375 0.5	—

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Recommended Operating Conditions

Parameter	Unit
RF Input Power	1 dBm
DC Supply Voltage	3 V to 4 V
Junction Temperature	+150°C
Operating Temperature	-40°C to +85°C

Absolute Maximum Ratings[2,3]

Parameter	Unit
RF Input Power	21 dBm
DC Supply	4.3 V
Junction Temperature[4,5]	+175°C
Storage Temperature	-55°C to +150°C

2. Exceeding any one or combination of these limits may cause permanent damage to this device.
3. MACOM does not recommend sustained operation near these survivability limits.
4. Operating at nominal conditions with $T_J \leq +150°C$ will ensure MTTF > 1 x 10^6 hours.
5. Junction Temperature (T_J) = T_C + Ѳjc * (V * I)
   Typical thermal resistance (Ѳjc) = 10°C/W.
   a) For T_C = +25°C,
      T_J = 30°C @ 3.5 V, 130 mA
   b) For T_C = +85°C,
      T_J = 90°C @ 3.5 V, 130 mA

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these class 1B HBM and class C2A CDM devices.

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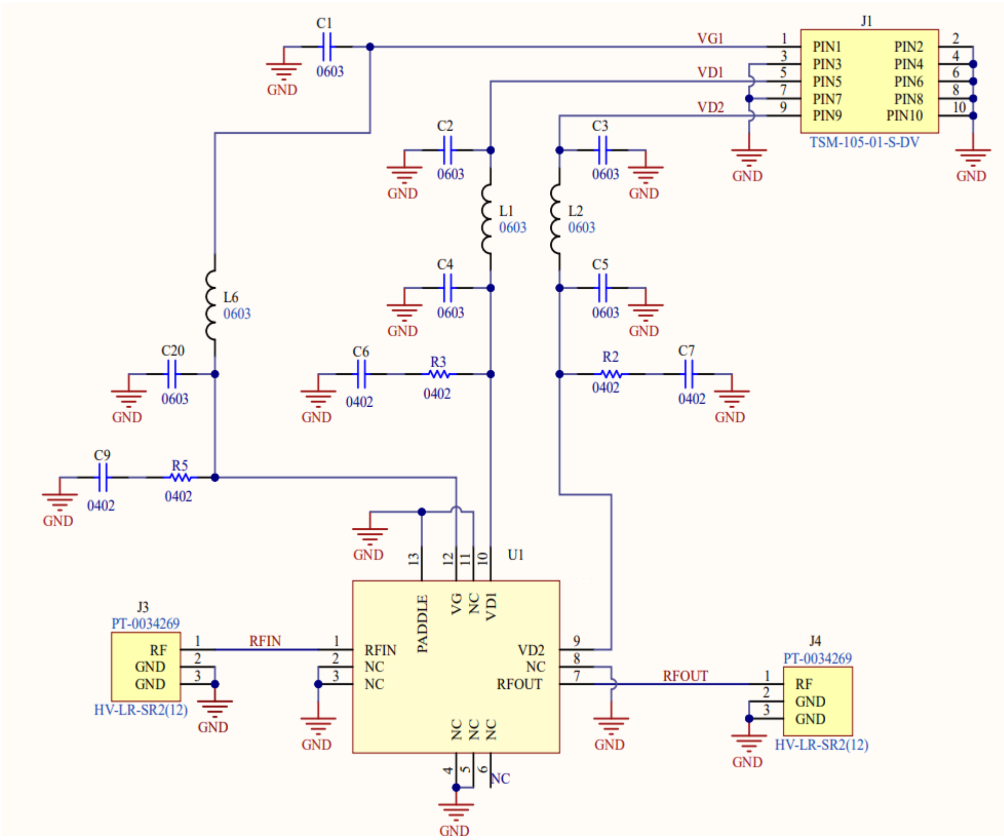
Application Circuit



Parts List

Part	Value	Case Style
R2,R3,R5	10 Ω	0402
C6,C7,C9	100 pF	chip capacitor MKVC-050100-1453
C4,C5,C20	0.1 µF	0602
C1,C2,C3	1 µF	0602
L1, L2, L6	10 nH	0603
U1	MAAL-011229-DIE	NA

Application Circuit Notes

The 100 pF chip capacitors should be placed as close as practically possible to the MMIC.

C4, C5, and C20 are SMT components which can be mounted on the application PCB, with the appropriate traces being bonded directly to the MMIC. These should be placed as closely as practically possible to the MMIC.

The circuit is not sensitive to the positioning of C1 - C3, however these should be on the same PCB as the rest of the biasing components.

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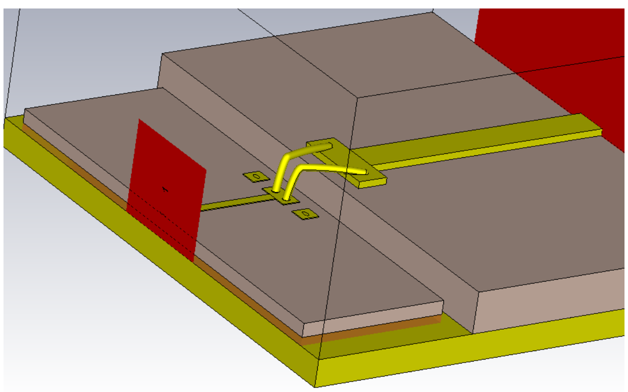
Wire Bonding

The loop height of the RF bonds should be minimized. Where the die is mounted above the PCB, it is recommended to use Reverse Ball-Stitch-on-Ball bonds (BSOB). If the die is mounted inside a cavity on the board, forward loop bonding may result in a lower loop height. V-shape RF bond with two wires (diameter = 25 µm) is recommended for optimum RF performance. RF bond wire length to be minimized to reduce the inductance effect. Simulations suggest no more than 300 µm. Substrate RF pad can be optimized to improve the microstrip to MMIC bond transition as shown in the example below.

Alternatively, a 3 mil bond ribbon could be used.



Handling the Die

This MMIC has fragile exposed airbridges on its surface and must be handled on the edges only using a vacuum collet or suitable tweezers. Do not touch the surface of the chip with a vacuum collet, tweezers, or fingers.

Operating the MAAL-011229-DIE

Turn-on

1. Apply V_G -2 V.
2. Increase V_{DD} to 3 V.
3. Set I_{DSQ} by adjusting V_G more positive. (typically -0.6 V for I_{DSQ} = 150 mA).
4. Apply RF_{IN} signal.

Turn-off

1. Remove RF_{IN} signal.
2. Decrease V_G to -2 V.
3. Decrease V_{DD} to 0 V.

Biasing Conditions

Recommended biasing conditions are V_{DD} = 3 V, I_{DSQ} = 150 mA (controlled with V_G).

Recommended PCB Information

RF input and output are 50 Ω transmission lines.
Single layer 8 mil Rogers RO4003C with 1/2 oz. Cu.
Use copper filled vias under ground paddle.

Grounding

It is recommended that the total ground (common mode) inductance not exceed 0.03 nH (30 pH). This is equivalent to placing at least four 8-mil (200-µm) diameter vias under the device, assuming an 8-mil (200-µm) thick RF layer to ground.

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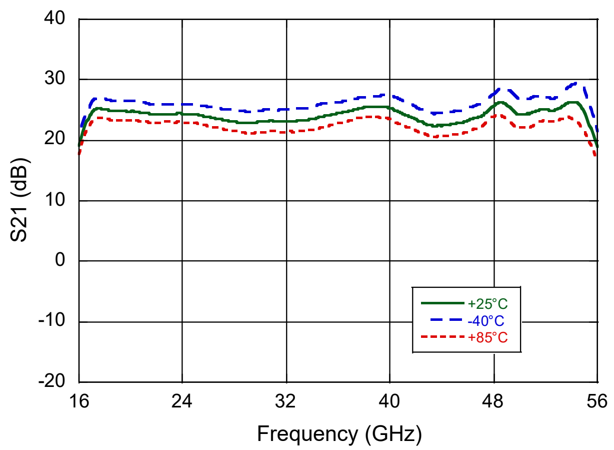
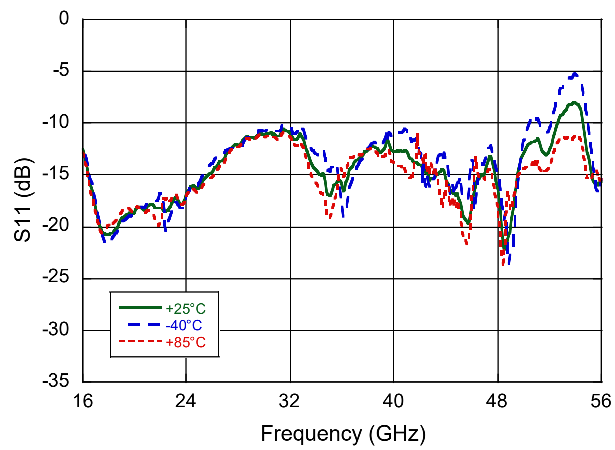
Typical Performance Curves @ V_D = 3 V, I_D = 150 mA, Z_0 = 50 Ω

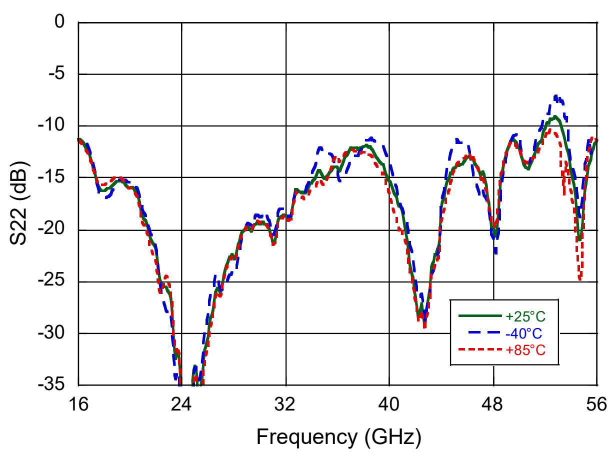
Gain



Input Return Loss



Output Return Loss



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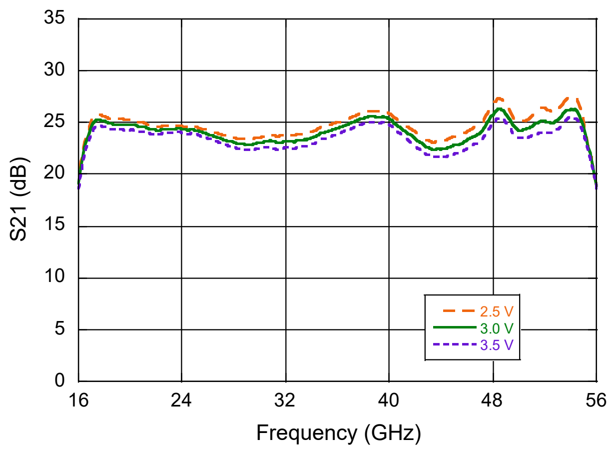
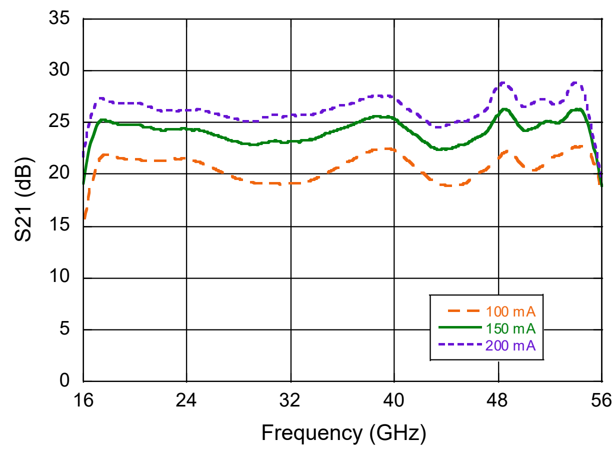
Typical Performance Curves: T_A = 25°C, Z_0 = 50 Ω

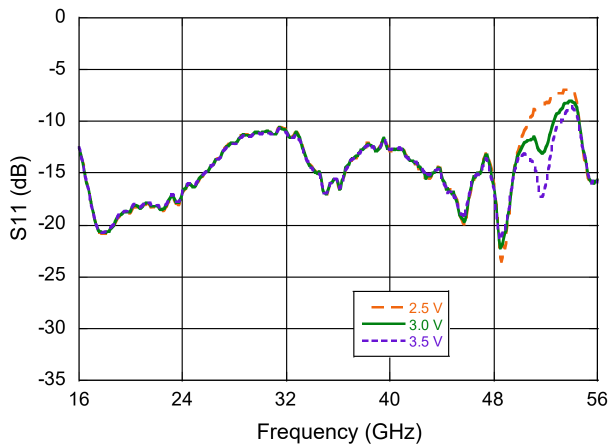
Gain @ 150 mA



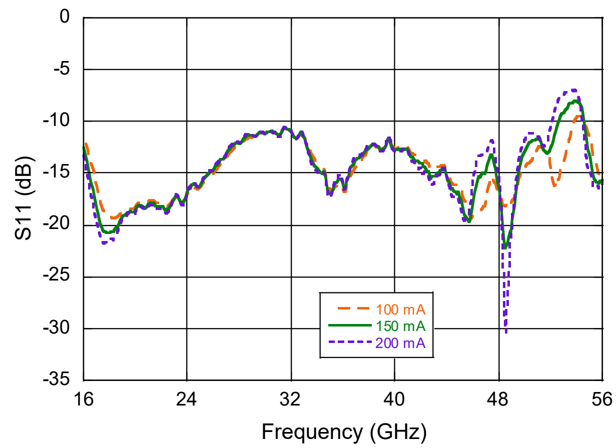
Gain @ 3 V



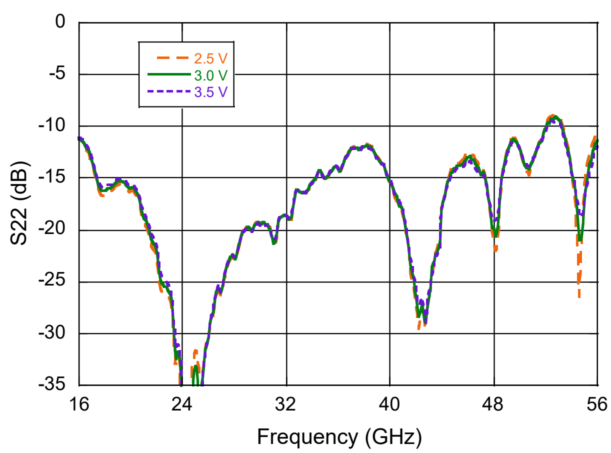
Input Return Loss @ 150 mA



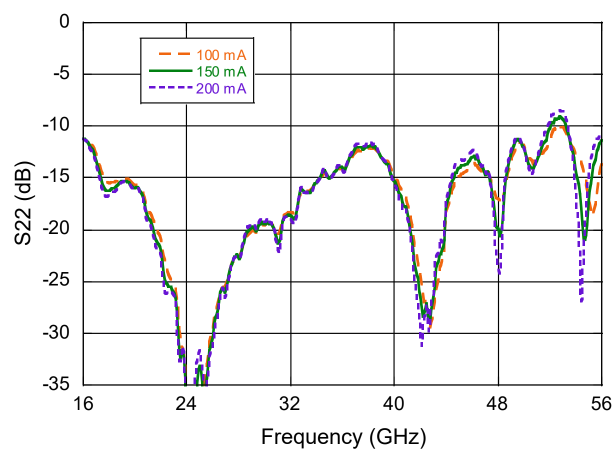
Input Return Loss @ 3 V



Output Return Loss @ 150 mA



Output Return Loss @ 3 V



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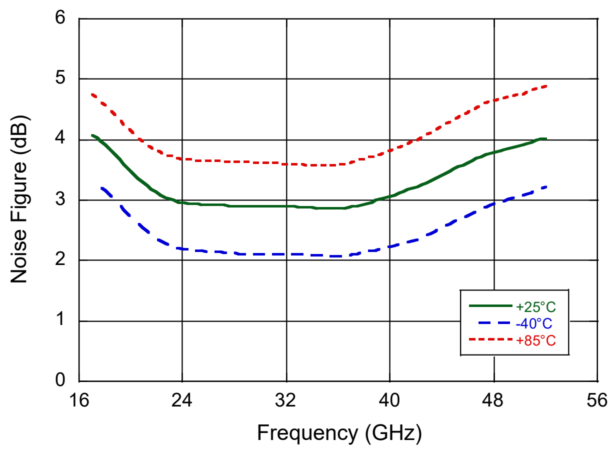
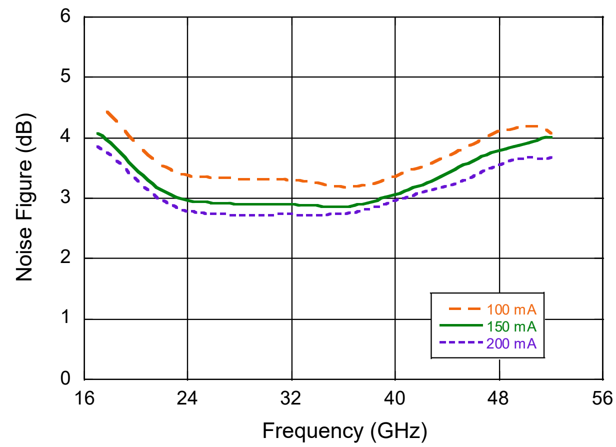
Typical Performance Curves: Z_0 = 50 Ω

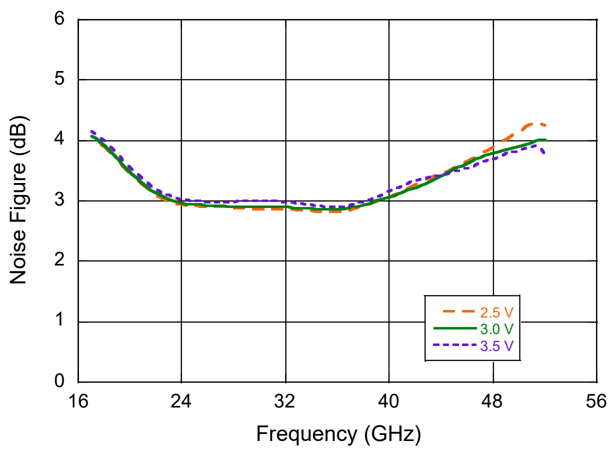
Noise Figure over Temperature @ 3 V, 150 mA



Noise Figure over Current @ 3 V, +25°C



Noise Figure over Voltage @ 150 mA, +25°C



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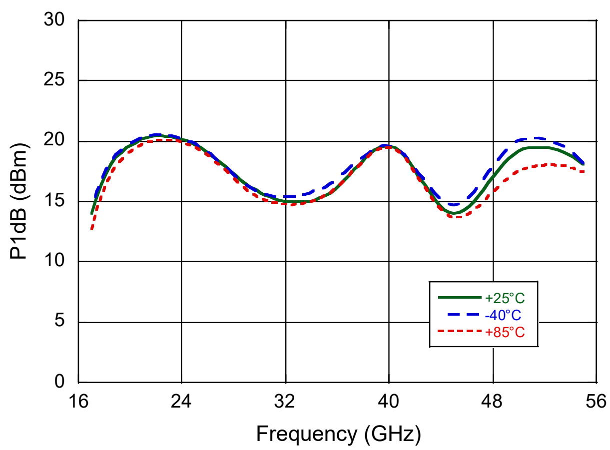
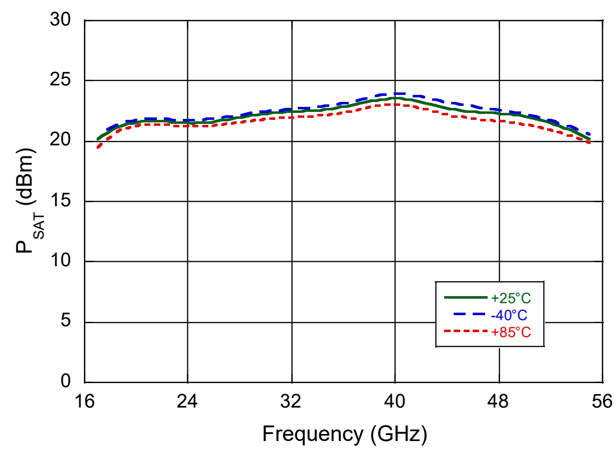
Typical Performance Curves: Z_0 = 50 Ω

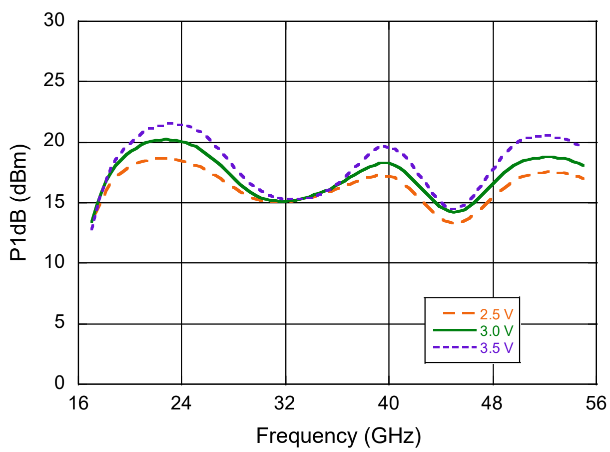
P1dB over Temperature @ 3 V, 150 mA



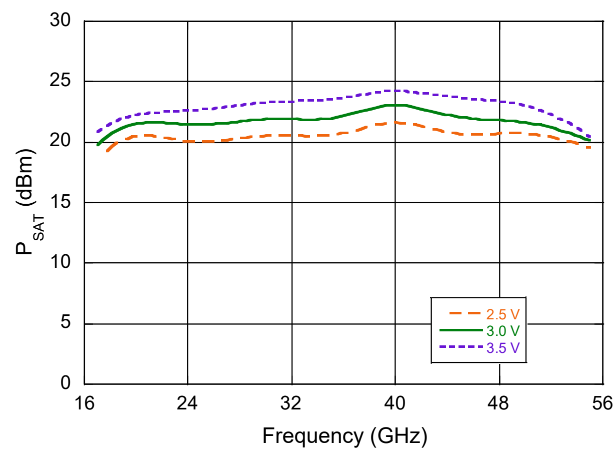
P_{SAT} over Temperature @ 3 V, 150 mA



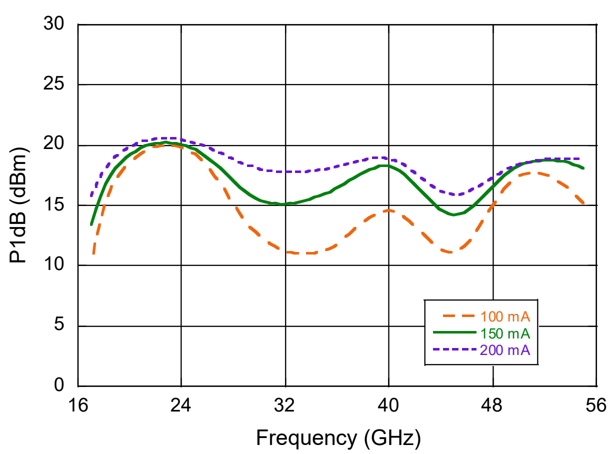
P1dB over Voltage @ 150 mA, +25°C



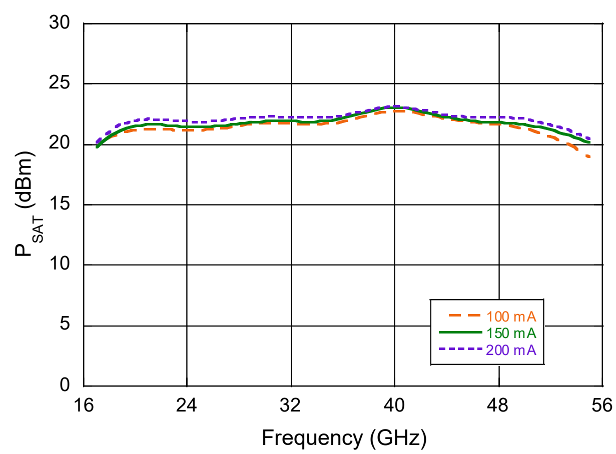
P_{SAT} over Voltage @ 150 mA, +25°C



P1dB over Current @ 3 V, +25°C



P3dB over Current @ 3 V, +25°C



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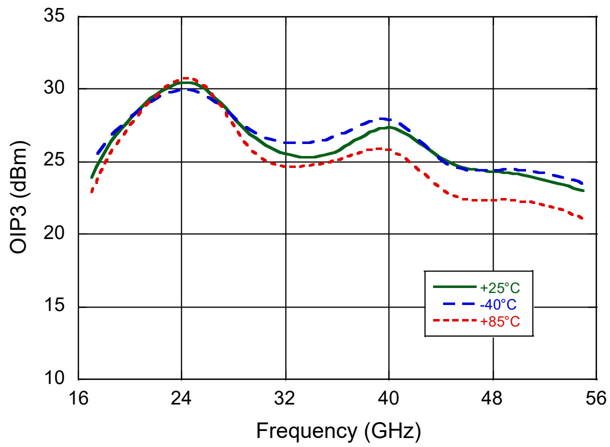
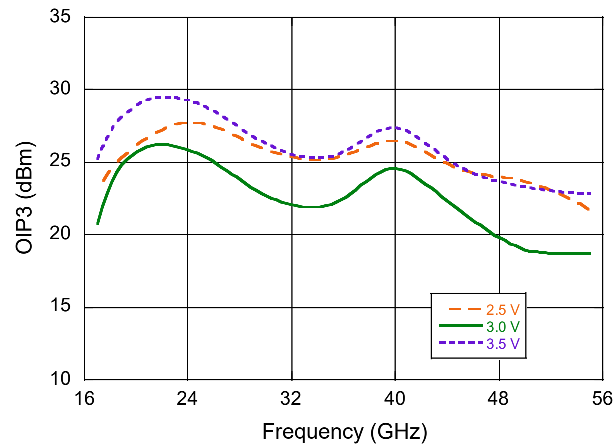
Typical Performance Curves: Z_0 = 50 Ω

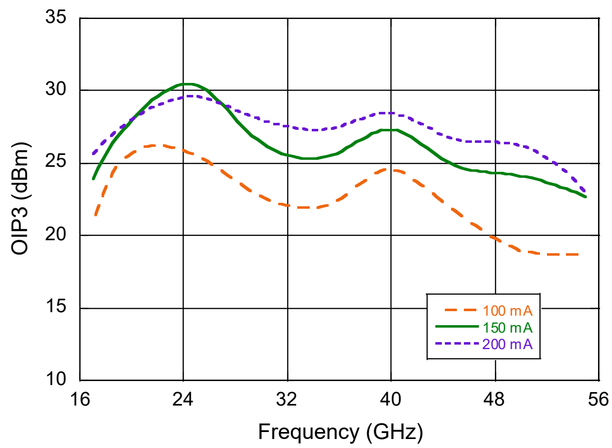
OIP3 over Temperature @ 3 V, 150 mA



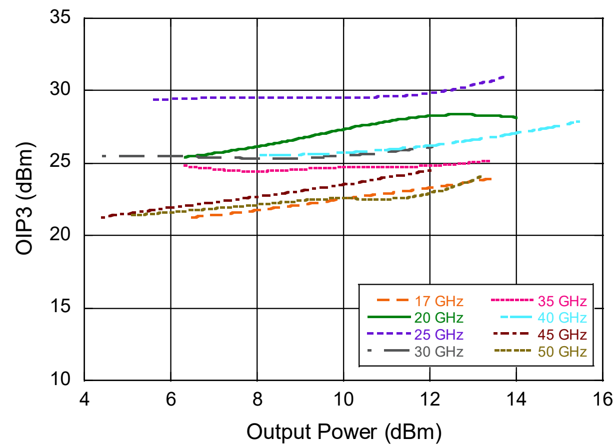
OIP3 over Voltage @ P_{IN} = -10 dBm, +25°C



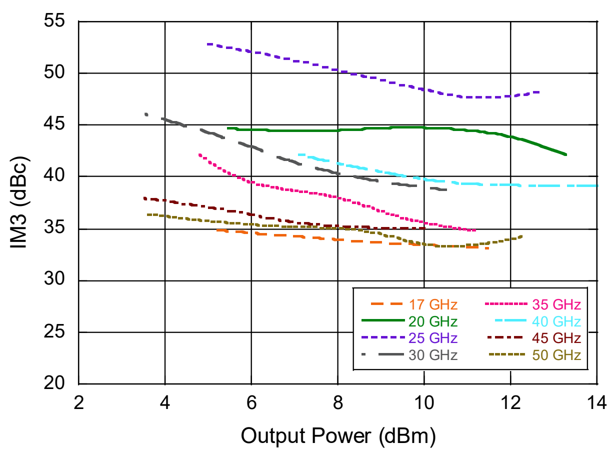
OIP3 over Current @ 3 V, +25°C



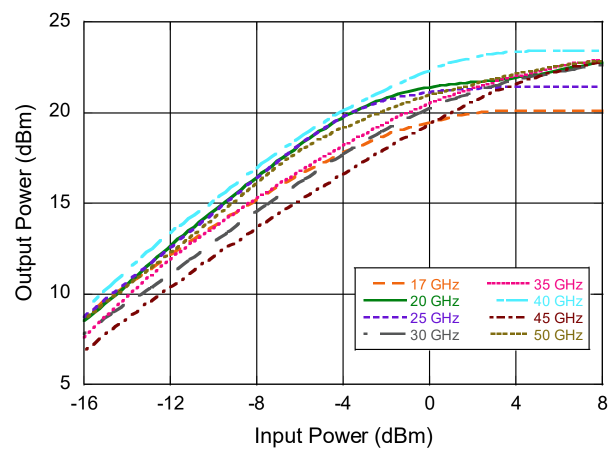
OIP3 vs Output Power @ 3 V, 150 mA, +25°C



IM3 vs Output Power @ 3 V, 150 mA, +25°C



Output Power vs Input Power @ 3 V, 150 mA, +25°C



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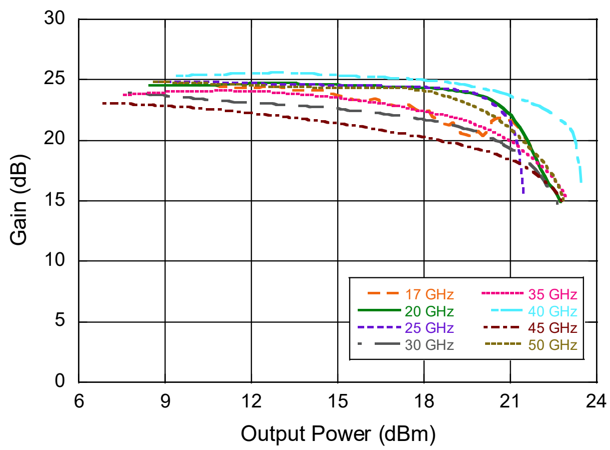
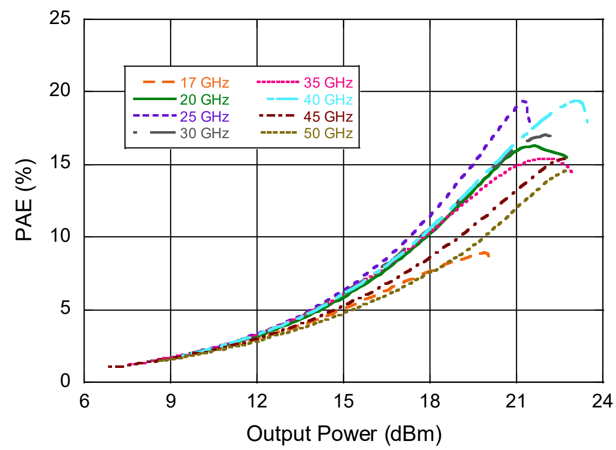
Typical Performance Curves @ V_D = 3 V, I_D = 150 mA, T_A = 25°C, Z_0 = 50 Ω

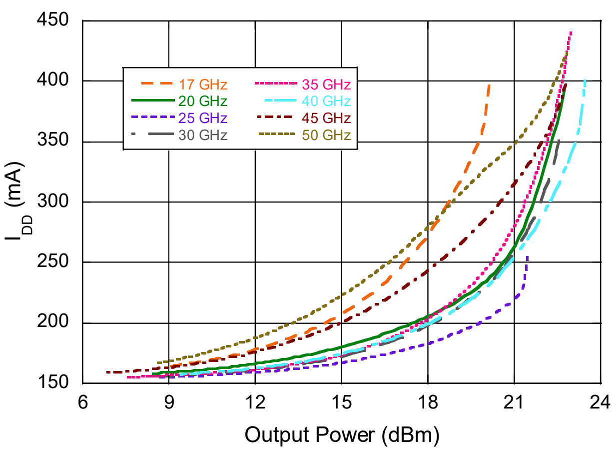
Gain vs Output Power



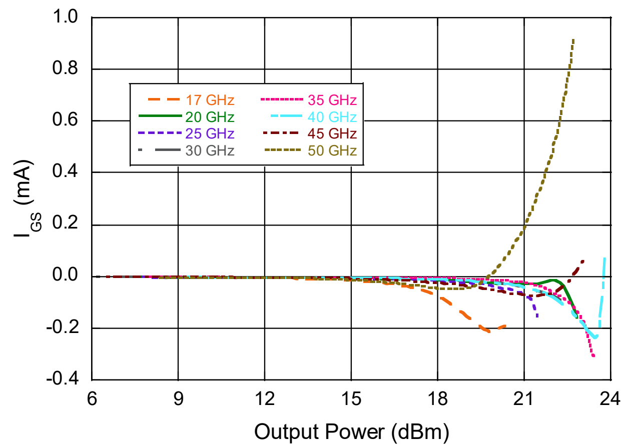
Power Added Efficiency vs Output Power



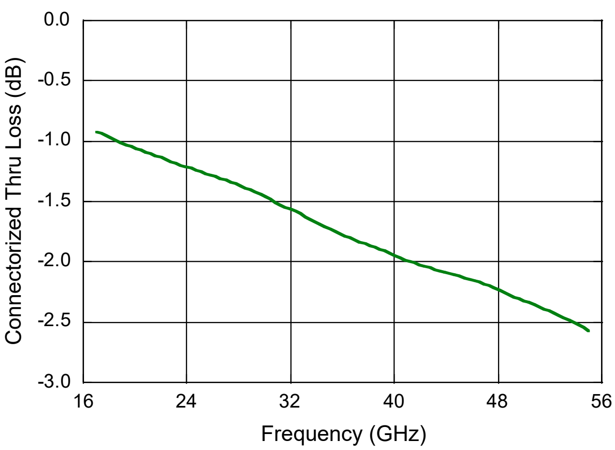
Drain Current vs Output Power



Gate Source Current vs Output Power



Evaluation Board Through Loss



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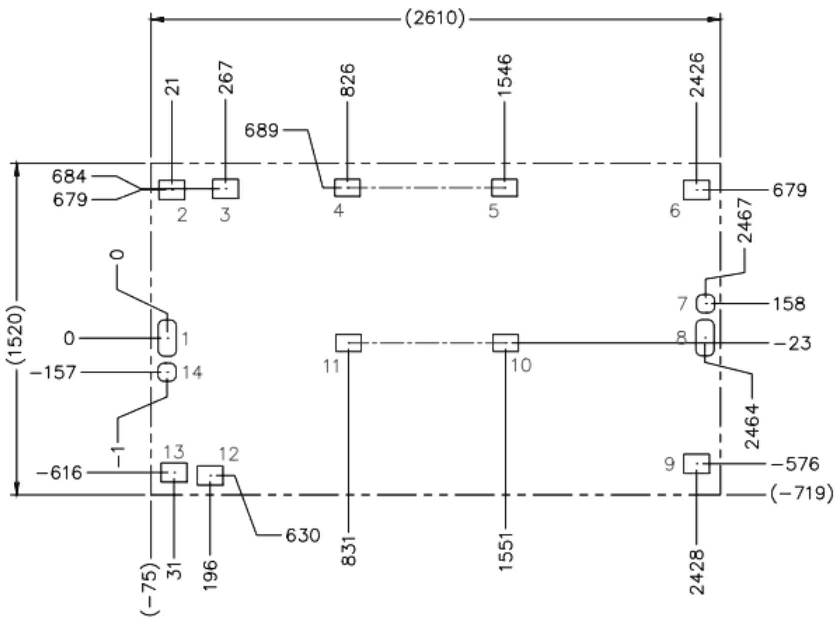
Die Outline



BOND PAD SIZE	
PAD	SQ(μm)
1,8	83x166
2,3,6, 9,12,13	118x88
4,5,10,11	116x78
7,14	83x83

NOTES:
1. UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS SHOWN ARE μm WITH A TOLERANCE OF ±5μm.
2. DIE THICKNESS IS 100μm ±10%
3. BOND/PAD BACKSIDE METALLIZATION: GOLD
4. DIE SIZE REFLECTS FINAL DIMENSIONS.

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