Features

- 15 dB Gain
- 2.5 dB Noise Figure
- 29 dBm Output IP3
- 5 V Drain Supply
- Bare Die (3.45 x 1.304 mm) 4 mil thickness
- RoHS* Compliant

Applications

- Multi Market
- ISM

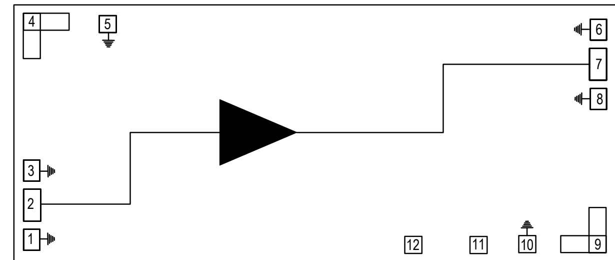
Description

The MAAL-011181-DIE is a wideband distributed low noise amplifier with an operating frequency range of 9 kHz to 20 GHz. This LNA has a typical 2.5 dB noise figure, 15 dB gain, 29 dBm OIP3, 19 dBm P1dB and 21 dBm P3dB. Only a single bias supply voltage of 5 V is required to bias the LNA. The typical current draw is 125 mA.

No external matching components are required, but external biasing components are needed. Large capacitors for bypassing are required on C_{BIAS1} and C_{BIAS2} for low frequency operation. A DC blocking capacitor is required on the RF input. An RF choke and blocking capacitor should be added to the RF output pin to bias the amplifier. 5 V must be applied to V_{BIAS} while V_{DD} can vary.

The MAAL-011181-DIE is designed for wideband low noise applications such as test equipment. It is available as a bare die. This LNA is also available in a 5 mm, 32 lead PQFN package under part number MAAL-011181.

Block Diagram



Pin Configuration[1,2]

Pin #	Pin Name	Description
1,3,5,6,8,10	GND	Ground
2	RF_{IN}	RF Input
4	C_{BIAS1}	Bypass Capacitor 1
7	RF_{OUT}/V_{DD}	RF Output/Voltage Supply
9	C_{BIAS2}	Bypass Capacitor 2
11	N/C	Internal Test
12	V_{BIAS}	Bias Voltage

1. Backside of die must be connected to RF, DC, and thermal ground.
2. It is not necessary to connect ground pads. Via holes connect these pads to the backside ground.

Ordering Information

Part Number	Package
MAAL-011181-DIE	Bare Die
MAAL-011181-DIESMB	Sample Board

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

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Electrical Specifications: V_{DD} = +5 V, V_{BIAS} = +5 V, T_A = +25°C, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	2 GHz 10 GHz 20 GHz	dB	13.0 12.5 11.0	15.5 14.5 13.0	—
Gain Flatness	9 kHz - 20 GHz	dB	—	+/-0.5	—
Gain Variation vs. Temperature	10 GHz	dB/°C	—	0.02	—
Noise Figure	10 GHz 20 GHz	dB	—	2.0 4.0	2.5 5.0
Input Return Loss	9 kHz - 20 GHz	dB	—	15	—
Output Return Loss	9 kHz - 20 GHz	dB	—	10	—
P1dB	10 GHz 20 GHz	dBm	15.0 10.5	18.0 13.5	—
P3dB	9 kHz - 20 GHz	dBm	—	21	—
IP3	9 kHz - 20 GHz -20 dBm per tone, 10 MHz spacing	dBm	—	29	—
Quiescent Current	9 kHz - 20 GHz	mA	—	125	165

Maximum Operating Conditions

Parameter	Maximum
Input Power	25 dBm
Junction Temperature[3,4]	+160°C
Operating Temperature	-40°C to +85°C

3. Operating at nominal conditions with $T_J \leq$ +160°C will ensure MTTF > 1 x 10^6 hours.
4. TX Junction Temp. (T_J) = T_C + Ɵjc * ((V * I) - (P_{OUT} - P_{IN})). Typical TX thermal resistance (Ɵjc) = 65°C/W.
   a) For T_C = +85°C, T_J = 125.6°C @ 5 V, 125 mA
   b) For Tc = +25°C, T_J = 65.6°C @ 5 V, 125 mA

Absolute Maximum Ratings[5,6]

Parameter	Absolute Maximum
Input Power	27 dBm
Junction Temperature[7]	+180°C
Storage Temperature	-55°C to +150°C

5. Exceeding any one or combination of these limits may cause permanent damage to this device.
6. MACOM does not recommend sustained operation near these survivability limits.
7. Junction temperature directly effects device MTTF. Junction temperature should be kept as low as possible to maximize lifetime.

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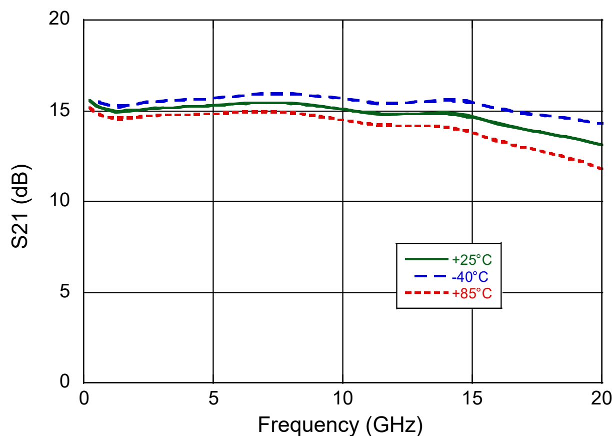
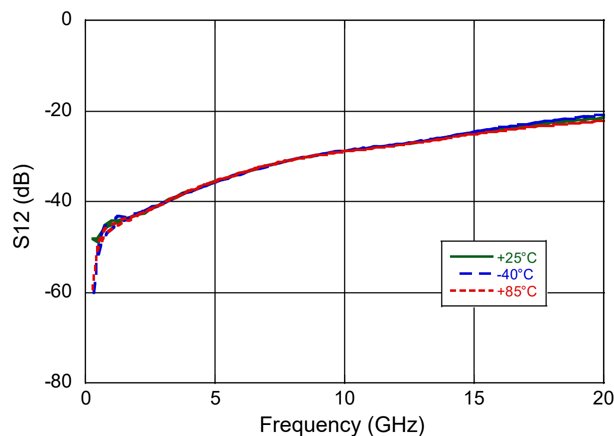
Typical Performance Curves (probed die mounted with 150 pF bypass capacitors)

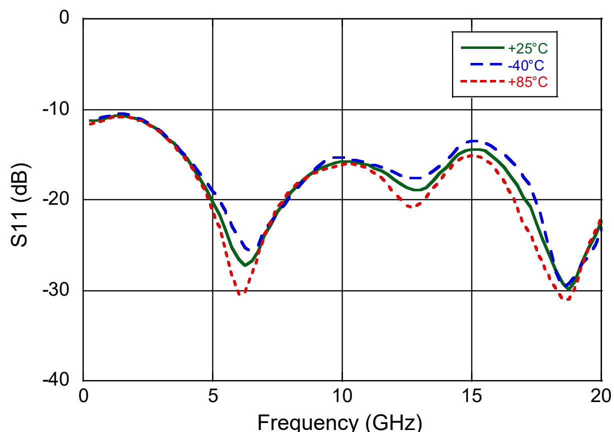
Gain



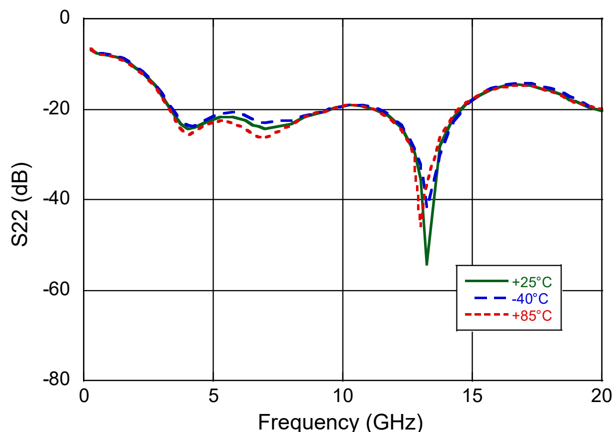
Isolation



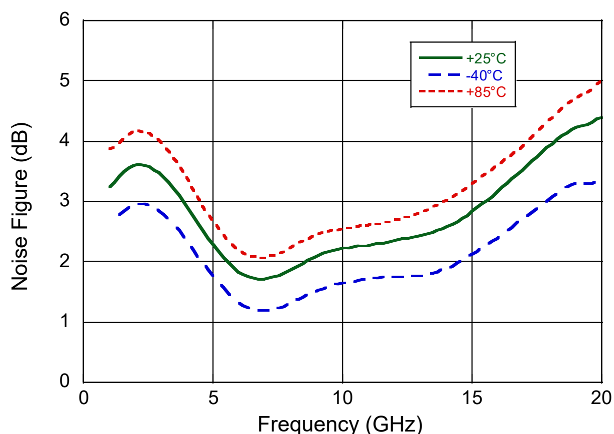
Input Return loss



Output Return Loss



Noise Figure



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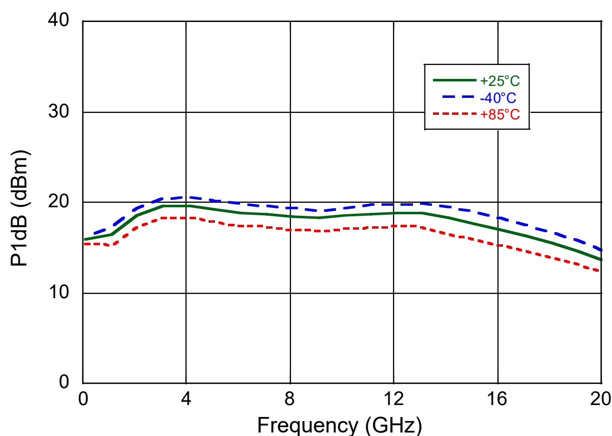
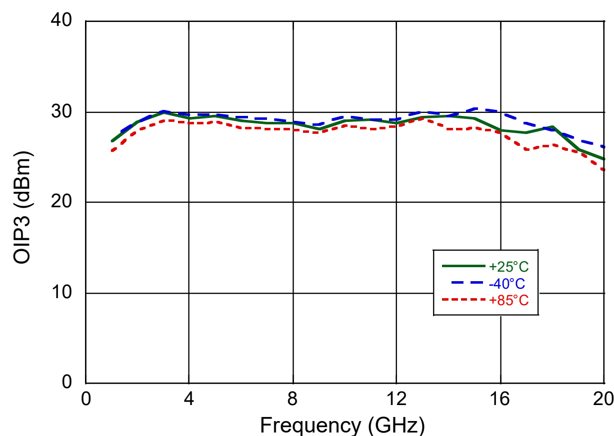
Typical Performance Curves (probed die mounted with 150 pF bypass capacitors)

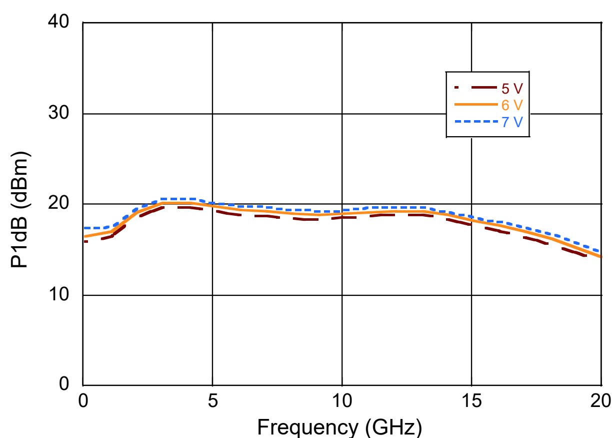
P1dB



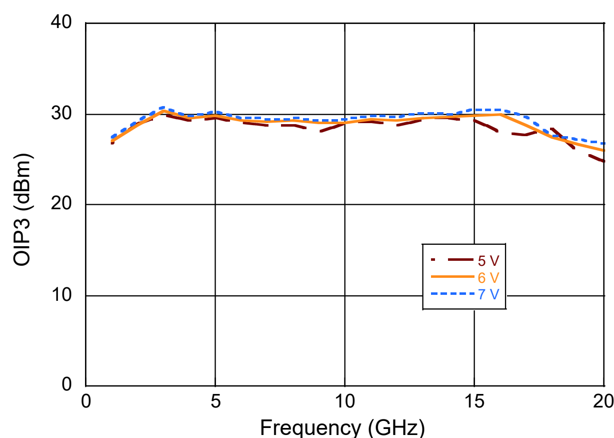
OIP3



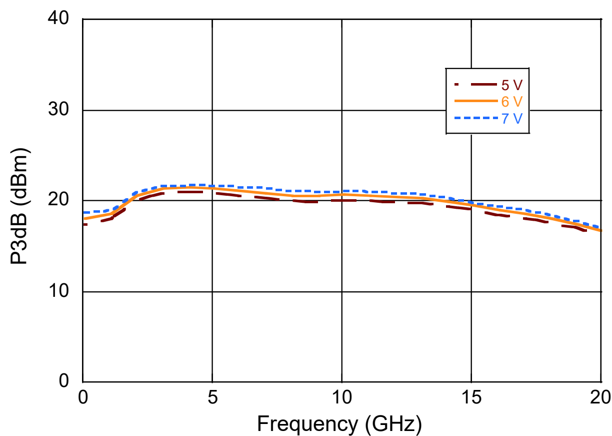
P1dB vs. V_{DD} (V_{BIAS} = +5 V)



OIP3 vs. V_{DD} (V_{BIAS} = +5 V)



P3dB vs. V_{DD} (V_{BIAS} = +5 V)



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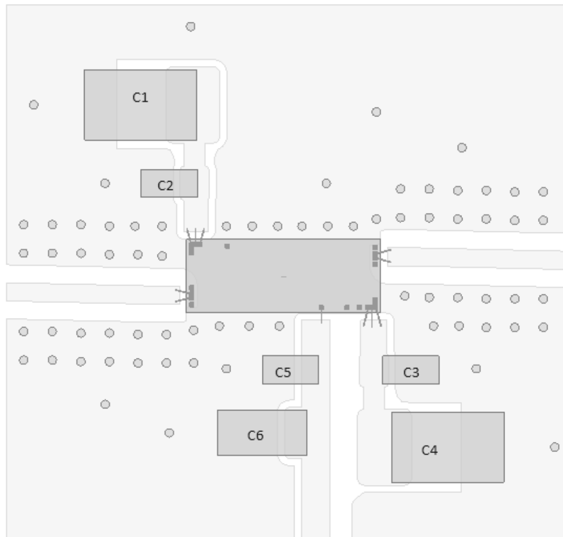
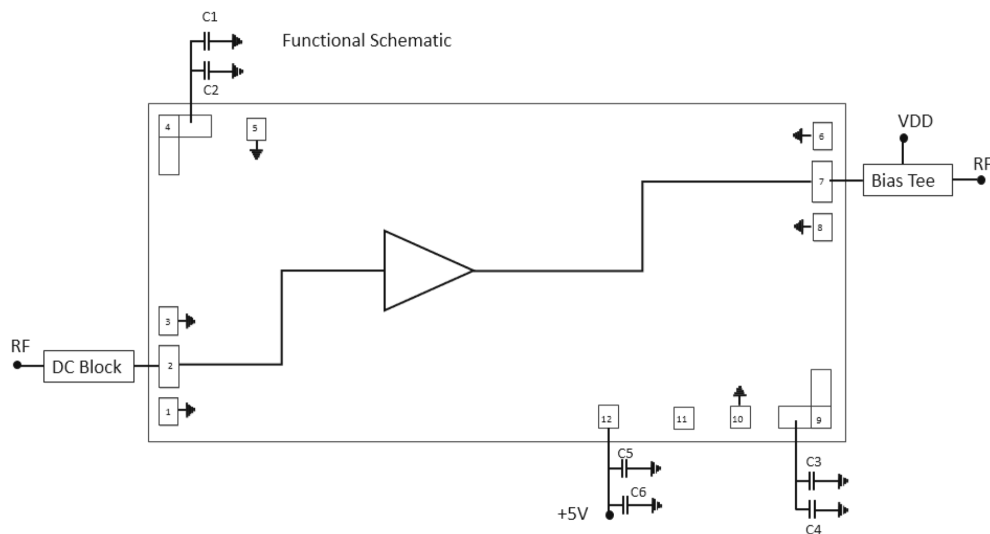
PCB Layout[8]



8. The DC blocking capacitor on RF_{IN} and Bias Tee on RF_{OUT} were connected externally on the MACOM Evaluation board and are not shown in this layout.

Functional Schematic



Parts List

Part	Value	Case Style	Manufacturer	Manufacturer's Part Number
C1, C4	1 µF	0805	TDK	C2012X5R1C106M085AC
C2, C3, C5	100 pF	0402	Murata	GRM39Y5V104Z016AB
C6	1000 pF	0603	Murata	GRM36X7R102K50AQ

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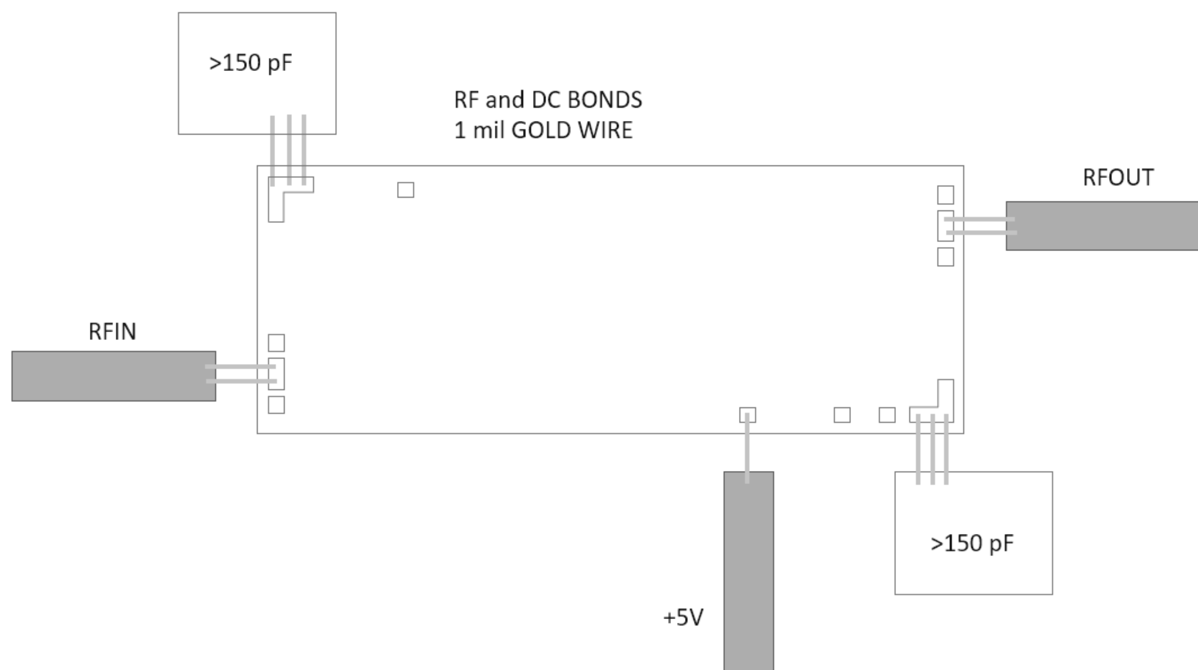
Recommended Bonding Diagram[9,10,11,12,13]



9. It is not necessary to wirebond GSG ground pads 1, 3, 6, and 8 to ground. They are already connected to ground through backside vias.
10. RF_{IN} requires off-chip RF blocking.
11. V_{DD} bias is to be applied using off-chip bias tee on RF_{OUT}.
12. V_{BIAS} should remain @ +5 V regardless of V_{DD}.
13. Low frequency performance is determined by value of bypass capacitors.

Die Attachment

This product is manufactured from 0.100 mm (0.004”) thick GaAs substrate and has vias through to the backside to enable grounding to the circuit.

Recommended conductive epoxy is Namics Unimec XH9890-6. Epoxy should be applied and cured in accordance with the manufacturer’s specifications and should avoid contact with the top of the die.

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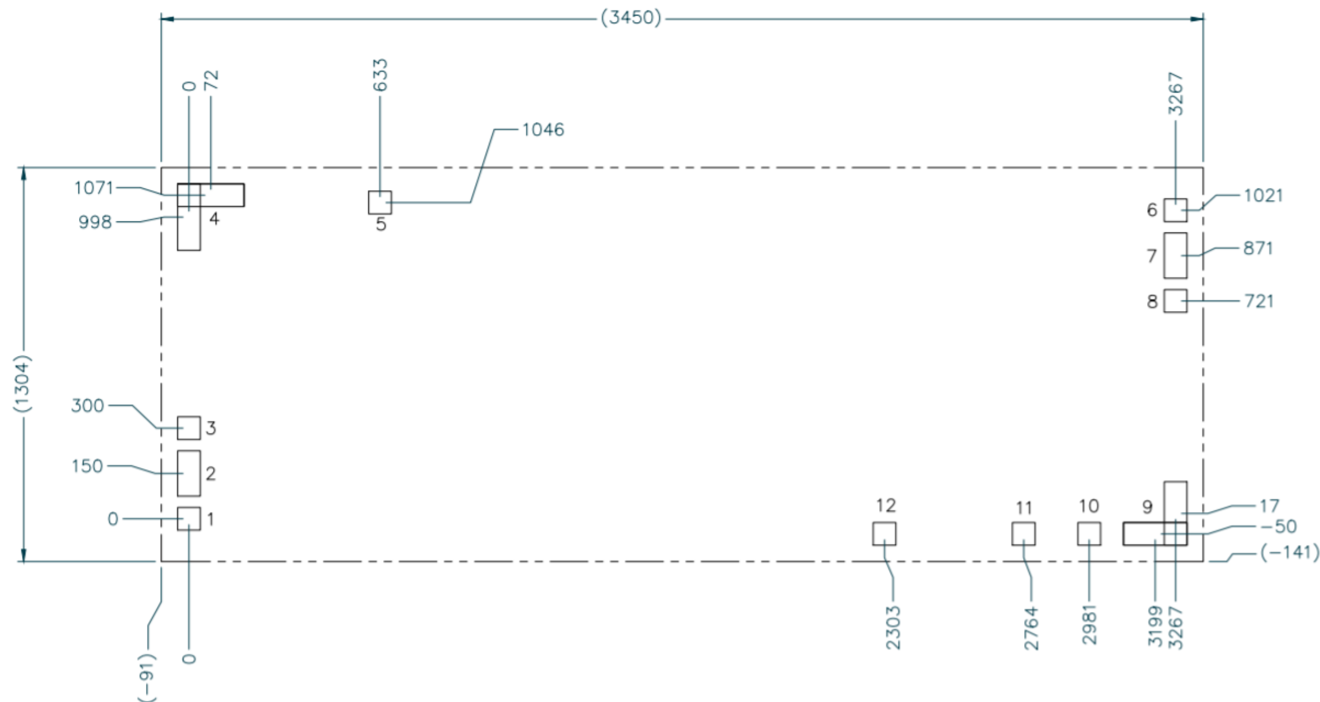
Die Outline[14,15,16,17]



14. Unless otherwise specified, all dimensions shown are µm with a tolerance of ±5 µm.
15. Die thickness is 100 ±10 µm.
16. Bond pad/backside metallization: Gold.
17. Die size reflects cut dimensions. Saw or laser kerf reduces die size ~25 µm each dimension.

Bond Pad Dimensions (µm)

Pad #	X	Y
1,3,5,6,8,10,11,12	75	75
2,7	75	150
4	220,75	75,220
9	210,75	75,210

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A devices.

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