Features

- Phase Noise: -164 dBc/Hz @ 10 kHz
- Gain: 24 dB
- P_{SAT}: 24 dBm
- Bias Voltage: V_{CC} = 6 V
- Bias Current: I_{CQ} = 215 mA
- 50 Ω Matched Input and Output
- Positive Voltage Only
- Lead-Free 5 mm AQFN 32-lead Package
- RoHS* Compliant

Applications

- Radar
- Electronic Countermeasures
- Test and Measurement
- Microwave Communication Systems

Description

The MAAL-011159 is an easy to use low phase noise amplifier assembled in a lead-free 5 mm 32-lead air cavity QFN plastic package. It operates from 2 - 27 GHz and provides -164 dBc/Hz phase noise, 24 dB gain and 24 dBm P_{SAT}. The input and output are fully matched to 50 Ω with typical return loss >14 dB.

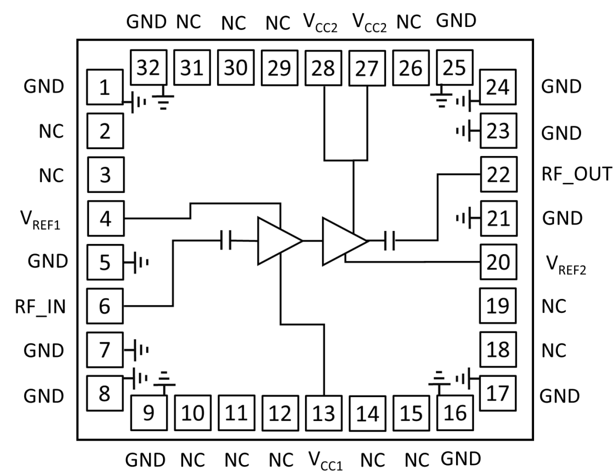
This product is fabricated using a GaAs HBT process which features full passivation for enhanced reliability.

Ordering Information

Part Number	Package
MAAL-011159-TR0100	100 piece reel
MAAL-011159-SMB	Sample Board

1. Reference Application Note M513 for reel size information.
2. All sample boards include 3 loose parts.

Functional Schematic



Pin Configuration[3]

Pad #	Pad Name	Description
1,5,7,8,9,16,17, 21,23,24,25,32	GND	Ground
2,3,10,11,12,14,15, 18,19,26,29,30,31	NC[4]	Not internally connected
4	V_{REF1}	Reference Voltage 1
6	RF_IN	RF Input
13	V_{CC1}	Collector Supply 1
20	V_{REF2}	Reference Voltage 2
22	RF_OUT	RF Output
27,28	V_{CC2}	Collector Supply 2

3. Backside of die must be connected to RF, DC and thermal ground.
4. It is recommended that these pins are grounded on the application PCB.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications: Freq. = 2 - 27 GHz, T_A = +25°C, V_{CC} = 6 V, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	P_{IN} = -10 dBm, 6 GHz P_{IN} = -10 dBm, 18 GHz P_{IN} = -10 dBm, 27 GHz	dB	22.5 21.0 17.0	24.5 24.0 21.0	—
Gain Flatness	—	dB	—	±2	—
Gain Variation over Temperature	—	dB/°C	—	0.028	—
Output Power	P_{IN} = -1.0 dBm, 6 GHz P_{IN} = -2.2 dBm, 18 GHz P_{IN} = -1.0 dBm, 27 GHz	dBm	20.5 18.0 15.0	23.0 20.5 18.5	—
Noise Figure	—	dB	—	4.5	—
Input Return Loss	—	dB	—	15	—
Output Return Loss	—	dB	—	14	—
P1dB	16 GHz	dBm	—	22	—
Psat	16 GHz	dBm	—	24	—
OIP3	16 GHz, -10 dBm P_{IN} per tone	dBm	—	32.5	—
Phase Noise	12 GHz, P_{SAT} 100 Hz 1 kHz 10 kHz 1 MHz	dBc/Hz	—	 -145 -157 -164 -172	—
Icq	—	mA	—	215	—

Absolute Maximum Ratings[5,6]

Parameter	Absolute Maximum
Input Power	8 dBm
V_{CC}	7.5 V
I_{CC}	520 mA
Junction Temperature[7,8]	+130°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +125°C

5. Exceeding any one or combination of these limits may cause permanent damage to this device.
6. MACOM does not recommend sustained operation near these survivability limits.
7. Operating at nominal conditions with $T_J \leq$ +130°C will ensure MTTF > 1 x 10^6 hours.
8. Junction Temperature (T_J) = T_C + Θjc * (V * I)
   Typical thermal resistance (Θjc) = 14.2 °C/W.
   a) For T_C = +25°C,
      T_J = 70.7°C @ 7.0 V, 460 mA
   b) For T_C = +85°C,
      T_J = 130.7°C @ 7.0 V, 460 mA

Maximum Operating Conditions

Parameter	Maximum
Input Power	5 dBm
V_{CC}	7.0 V
I_{CC}	460 mA
Junction Temperature	+130°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +125°C

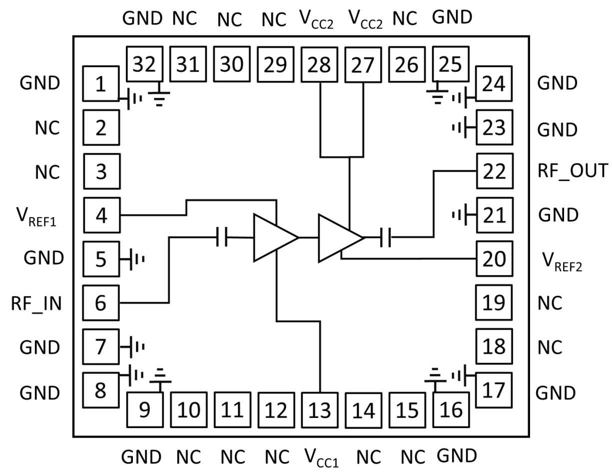
Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

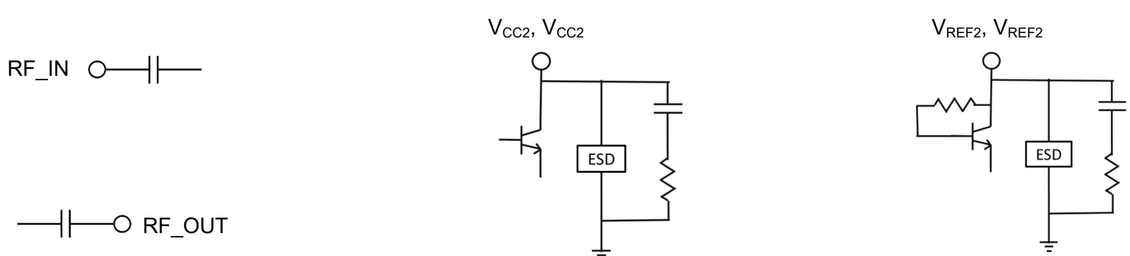
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A, 250 V devices.

Pad Configuration and Functional Descriptions

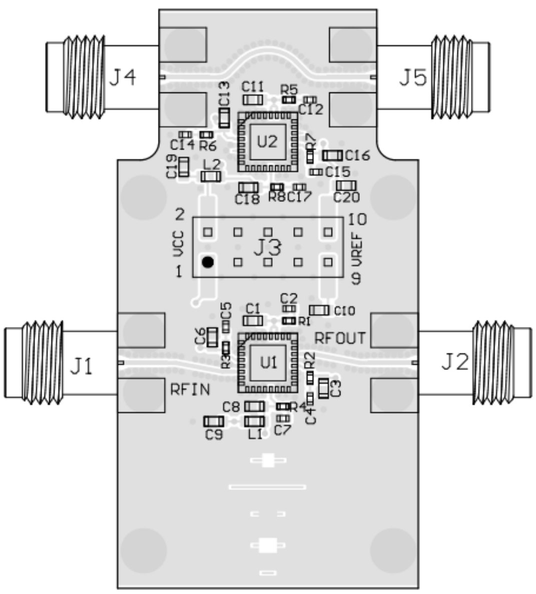


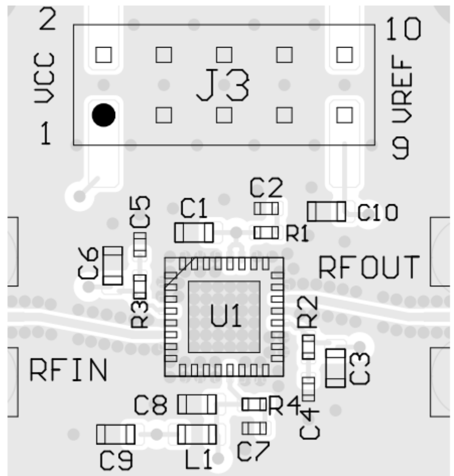
Pad #	Pin Name	Description
1,5,7,8,9,16,17, 21,23,24,25,32	GND	These pins are internally connected to ground.
2,3,10,11,12,14,15, 18,19,26,29,30,31	NC	These pins are not internally connected (i.e. open circuit). It is recommended that these are connected to ground on the application PCB.
4	V_{REF1}	Reference Voltage 1. This is the reference voltage used to set the quiescent collector current. External bypass capacitors are required as described in the applications schematic. This is not connected internally to V_{REF2}.
6	RF_IN	RF Signal Input. This pad is matched to 50 Ω and is AC coupled
13	V_{CC1}	Collector bias 1 for the amplifier. External bypass capacitors are required as described in the applications schematic. This is not connected internally to V_{CC2}.
20	V_{REF2}	Reference Voltage 2. This is the reference voltage used to set the quiescent collector current. External bypass capacitors are required as described in the applications schematic. This is not connected internally to V_{REF1}.
22	RF_OUT	RF Signal Output. This pad is matched to 50 Ω and is AC coupled
27,28	V_{CC2}	Collector bias 2 for the amplifier. External bypass capacitors are required as described in the applications schematic. This is not connected internally to V_{CC1}.

Interface Schematics



Evaluation Board Layout

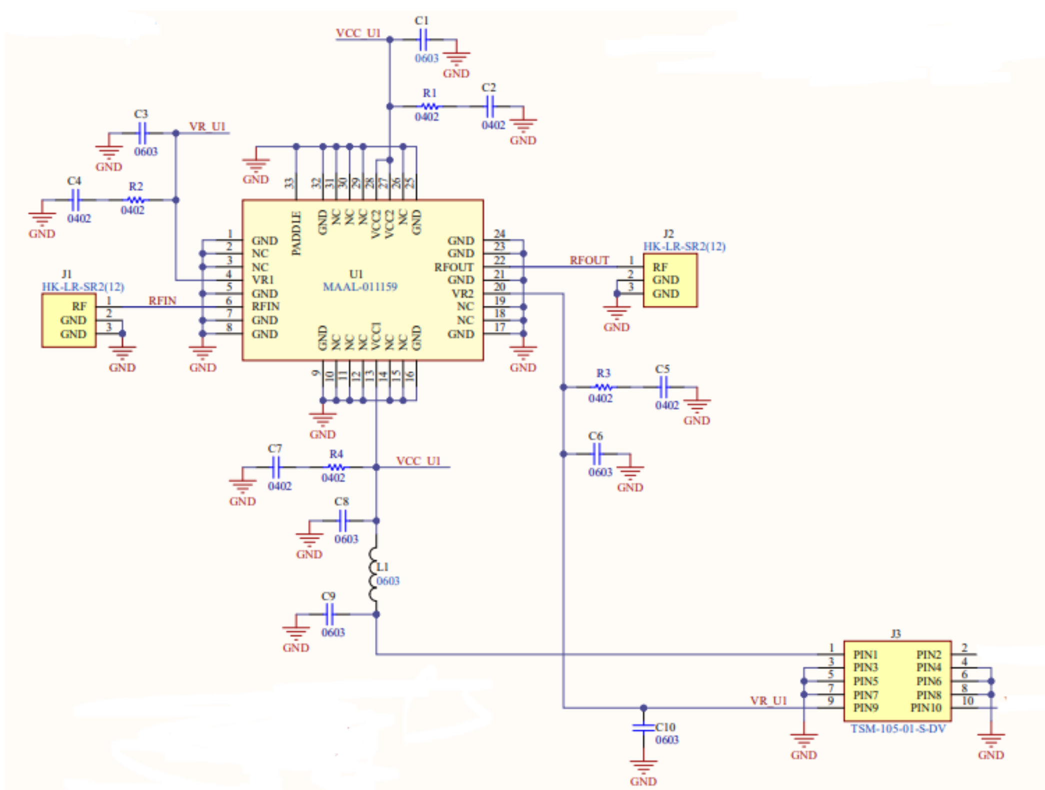




PCB DESIGN NOTES:

- RO4003C, 8 mil thick
- 1/2 copper
- Plating: solderable gold
- RF Trace: 14.0 mil width
- RF Space: 6.5 mil space
- 370 hr. or FR-406 backing 4 layers, total thickness 0.062"

Evaluation Board Schematic



Parts List

Part	Value	Case Style
C9, C10	1 µF	0603
C1, C3, C6, C8	0.1 µF	0603
C2, C4, C5, C7	100 pF	0402
R1-R4	10 Ω	0402
L1	10 nH	0603
C11-C20,R5-R8,L2,U2	DNI	DNI

Evaluation Board Notes

The 100 pF capacitors should be placed as close to the amplifier as practically possible. For the larger 0.1 µF capacitors proximity to the MMIC die is less important. The circuit is not sensitive to the positioning of the 1.0 µF capacitors however these should be on the same PCB as the rest of the biasing components.

To ensure proper grounding the number of ground vias under the device should be maximized (within practical limits imposed by the PCB vendor).

Biasing Conditions

Recommended biasing conditions are V_{CC} = 6 V, I_{CC} = 215 mA (controlled with V_{REF}). The collector bias voltage range is 4 to 6 V, and the quiescent collector current biasing range is 195 to 245 mA.

Operation

To turn-on:

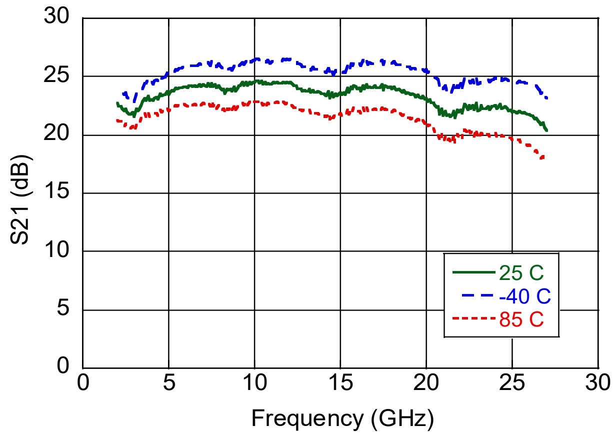
1. Apply +5 V to V_{CC1} and V_{CC2}
2. Starting at 0 V, adjust V_{REF1} and V_{REF2} connected together for target I_{CC}

To turn-off:

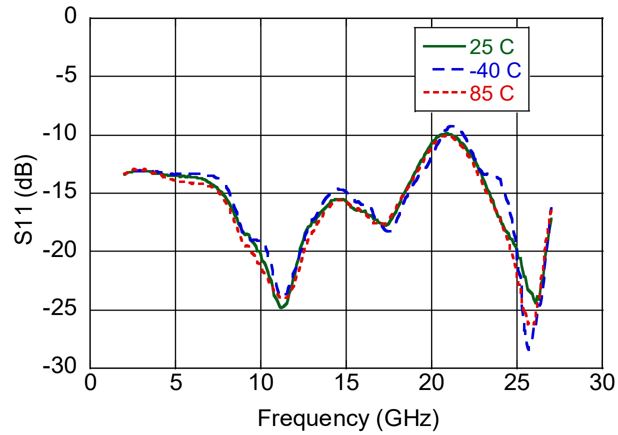
1. Set V_{REF1} and V_{REF2} connected together to 0 V
2. Set V_{CC1} and V_{CC2} to 0 V

Typical Performance Curves: V_{CC} = 6 V, I_{CC} = 215 mA

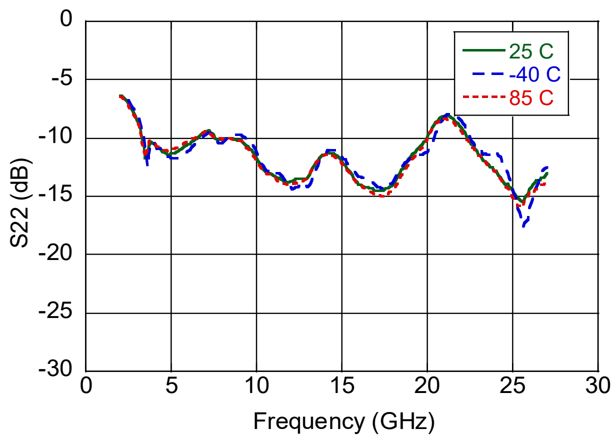
Gain



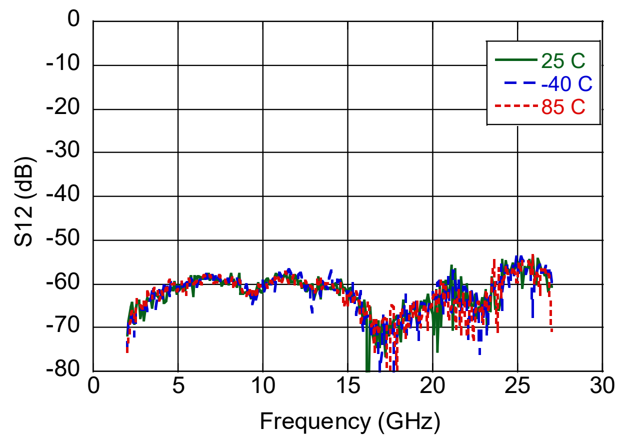
Input Return Loss



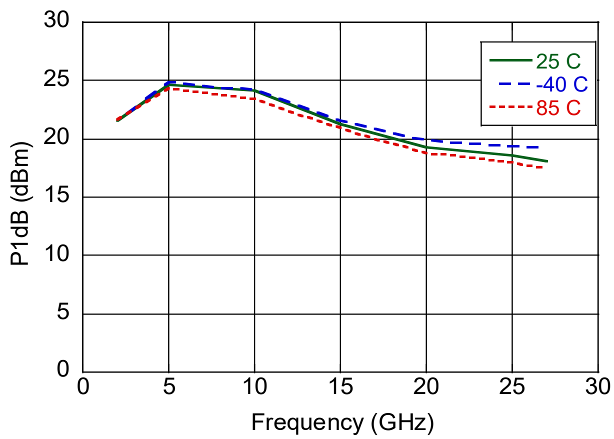
Output Return Loss



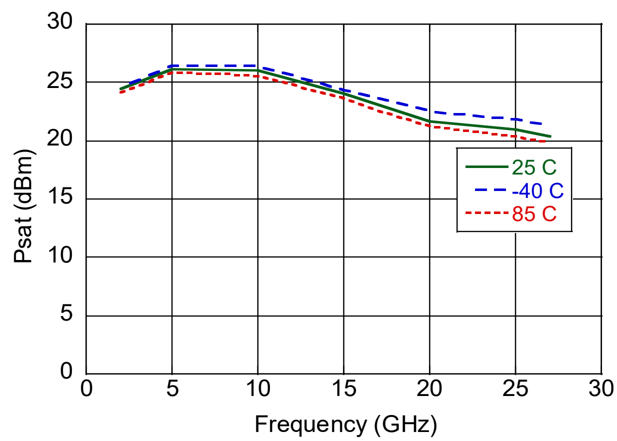
Reverse Isolation



P1dB

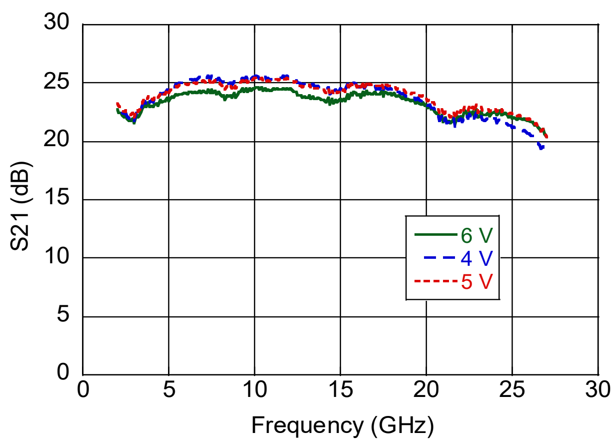


P_{SAT}

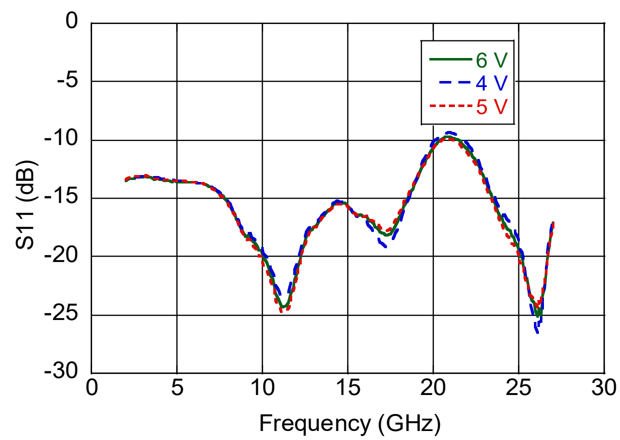


Typical Performance Curves: I_{CC} = 215 mA, +25°C

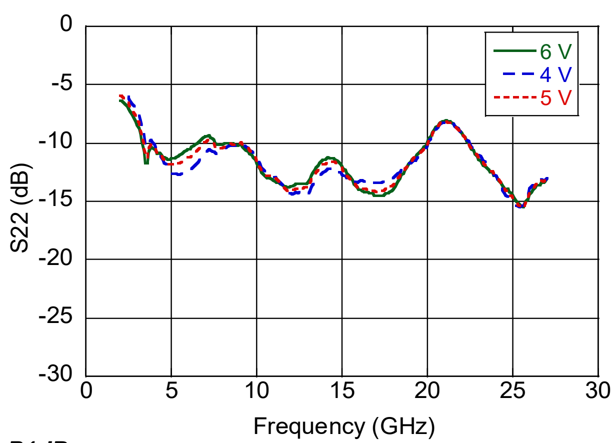
Gain



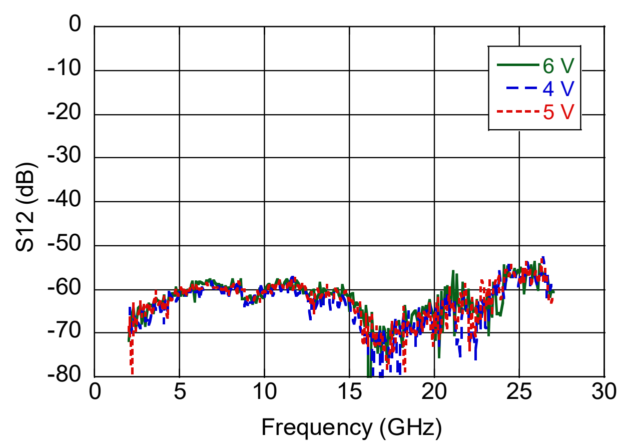
Input Return Loss



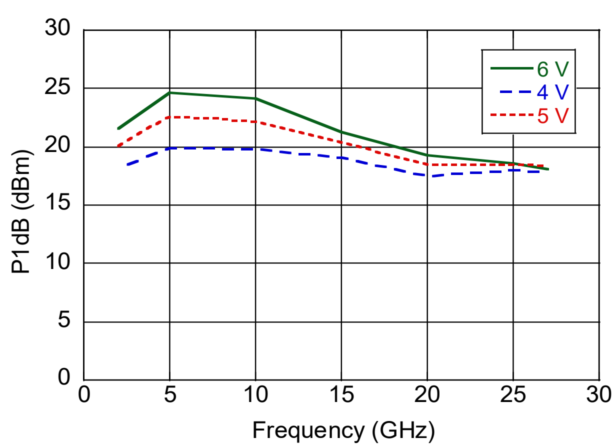
Output Return Loss



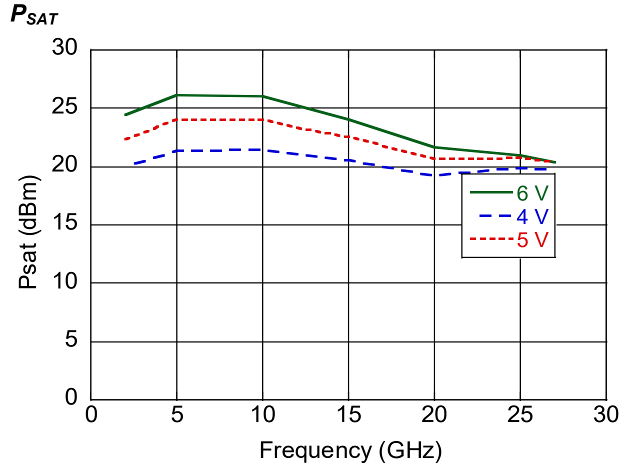
Reverse Isolation



P1dB

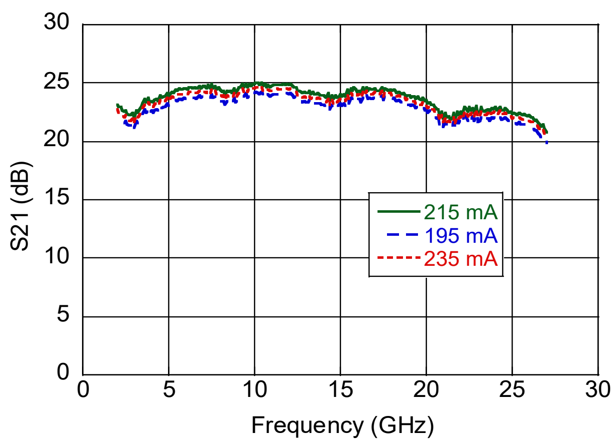


P_{SAT}

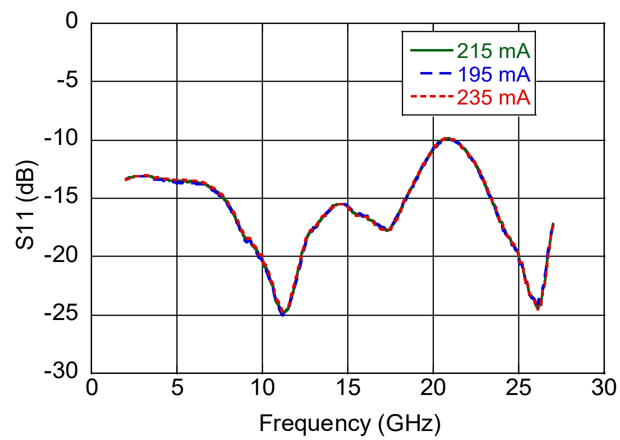


Typical Performance Curves: V_{CC} = 6 V, +25°C

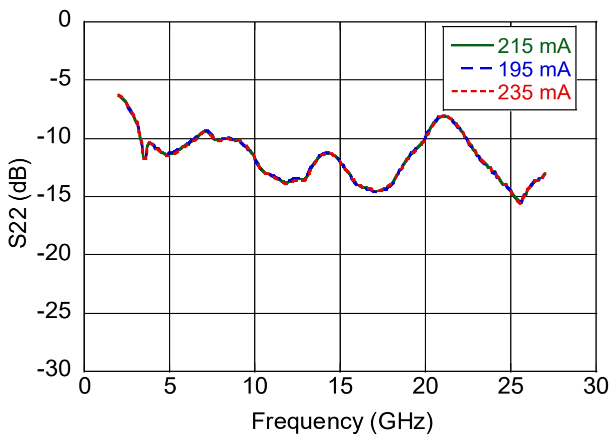
Gain



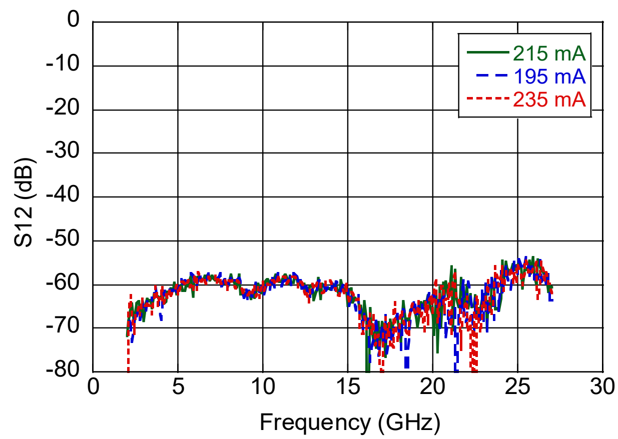
Input Return Loss



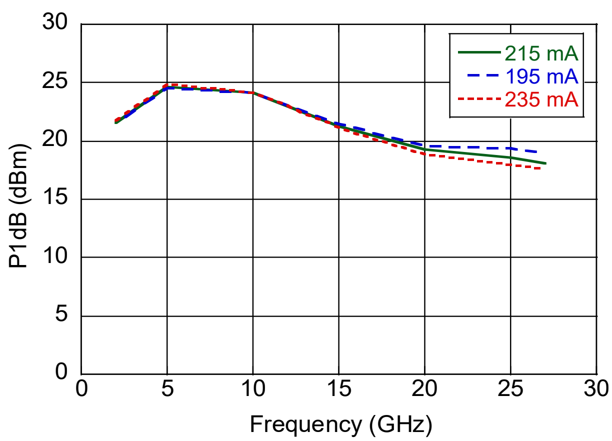
Output Return Loss



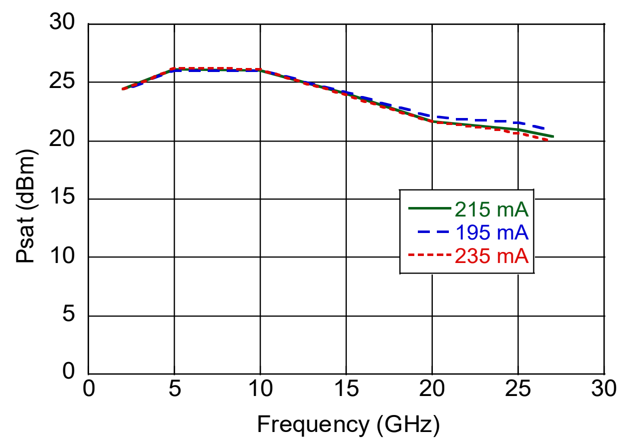
Reverse Isolation



P1dB

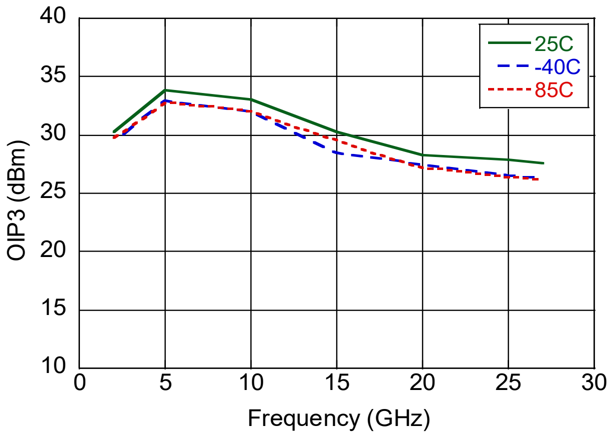


P_{SAT}

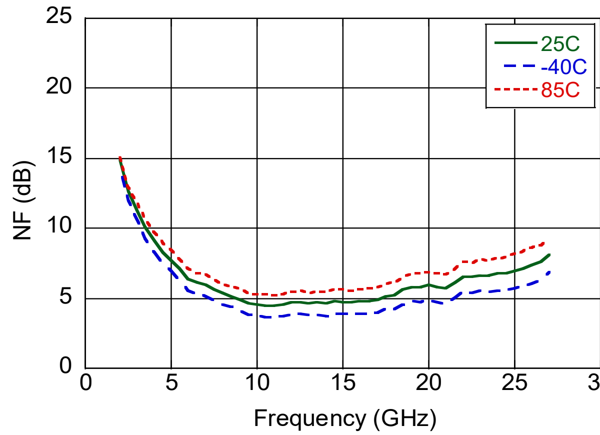


Typical Performance Curves: V_{CC} = 6 V, I_{CC} = 215 mA, +25°C

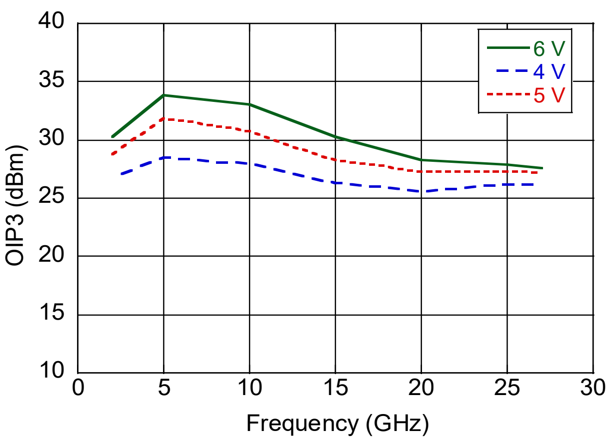
Output IP3
(10 MHz Tone Spacing, P_{IN} = -10 dBm per tone)



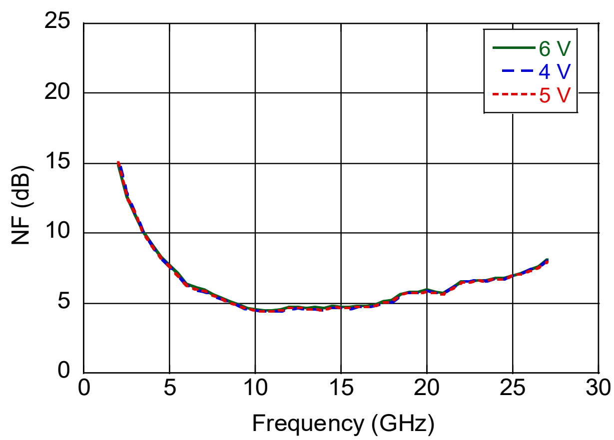
Noise Figure



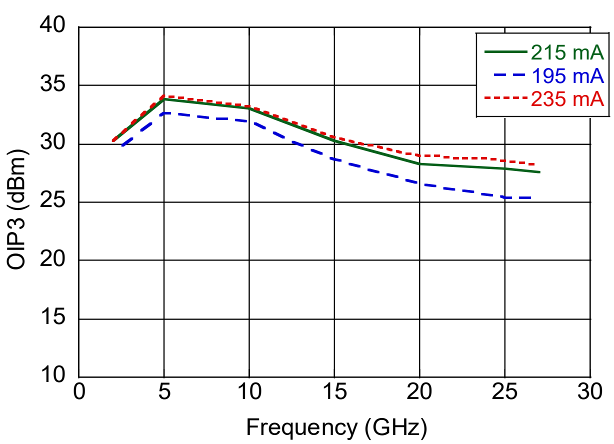
Output IP3
(10 MHz Tone Spacing, P_{IN} = -10 dBm per tone)



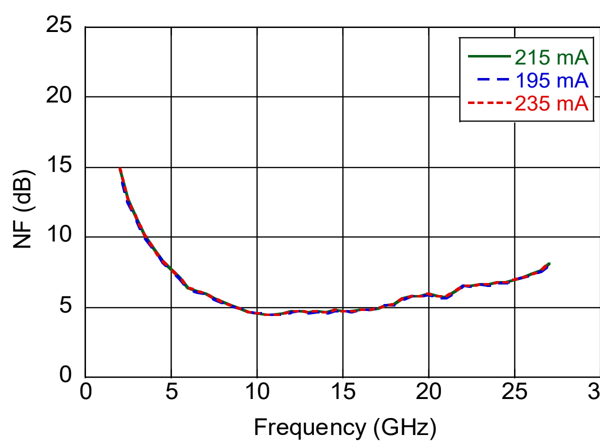
Noise Figure



Output IP3
(10 MHz Tone Spacing, P_{IN} = -10 dBm per tone)

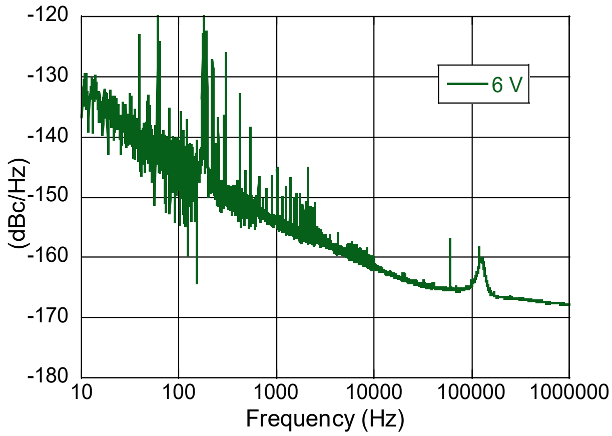


Noise Figure

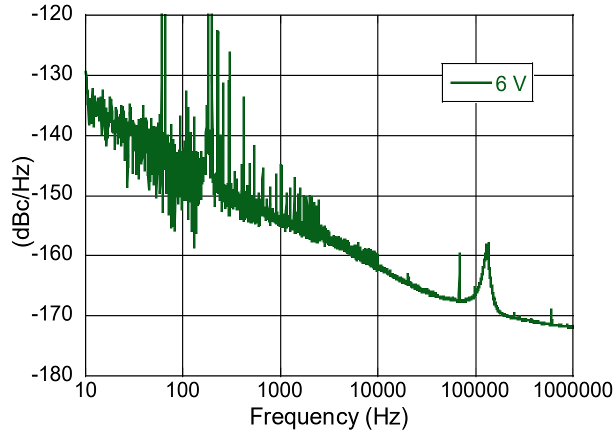


Typical Performance Curves[6]: I_{CC} = 135 mA, +25°C

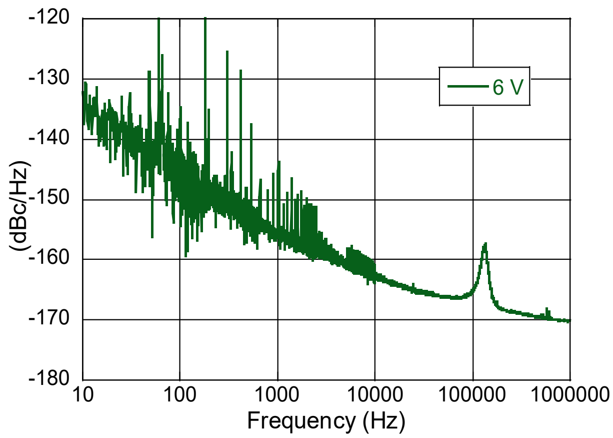
Phase Noise @ 4 GHz, P1dB



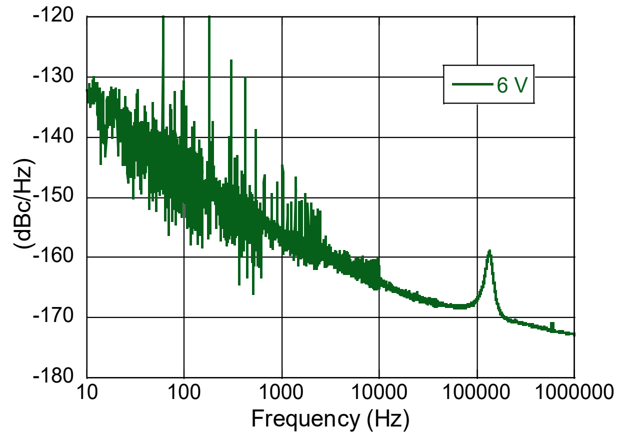
Phase Noise @ 4 GHz, P3dB



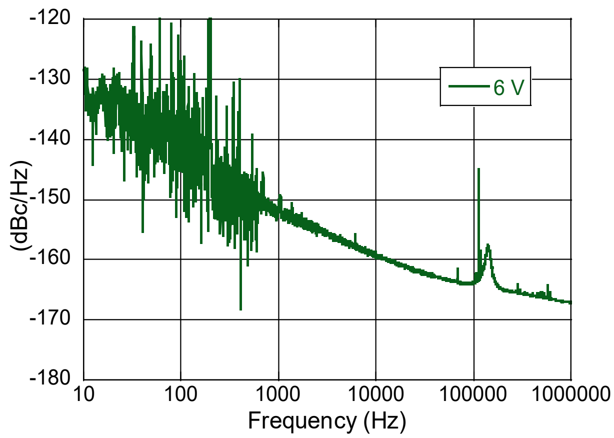
Phase Noise @ 12 GHz, P1dB



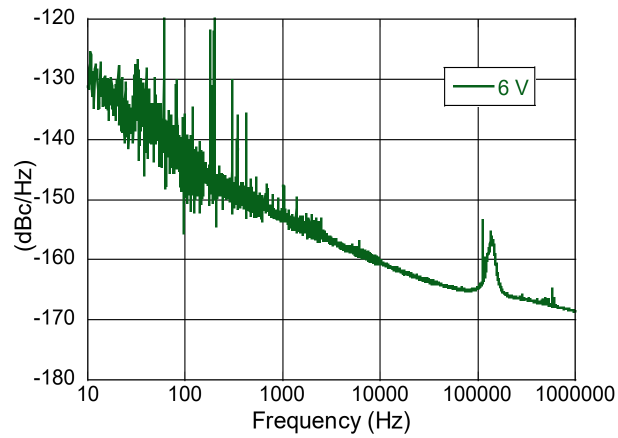
Phase Noise @ 12 GHz, P3dB



Phase Noise @ 20 GHz, P1dB



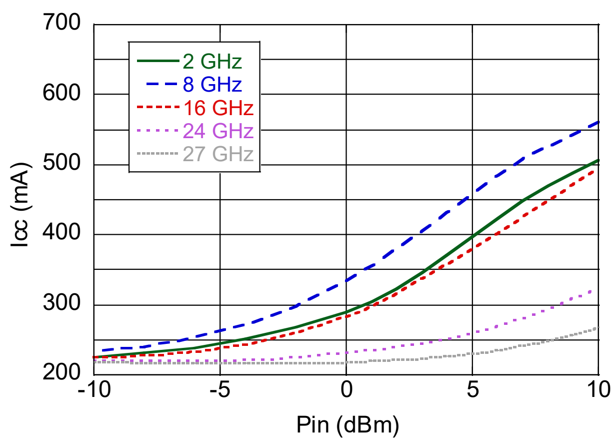
Phase Noise @ 20 GHz, P3dB



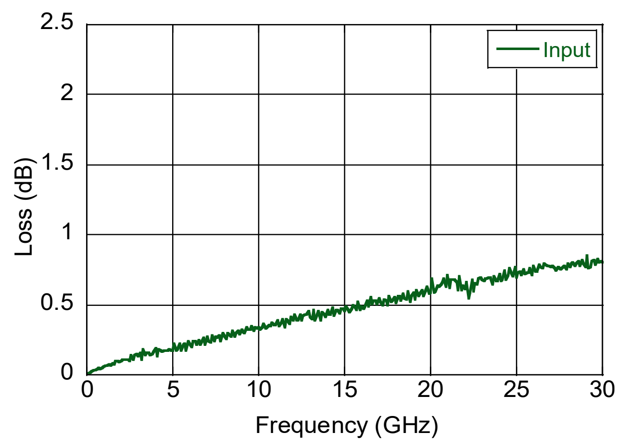
6. The aberration in the phase noise data at approximately 500MHz is due to the test equipment used and not the amplifier itself.

Typical Performance Curves: V_{CC} = 6 V, I_{CC} = 135 mA, +25°C

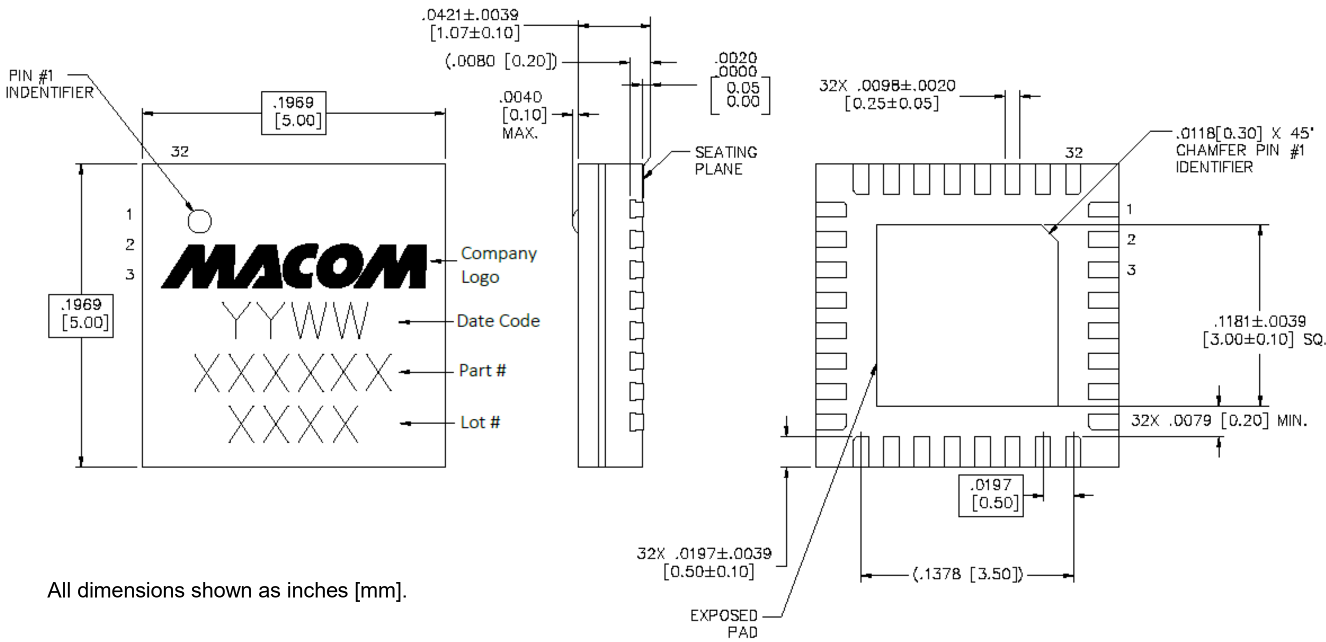
Bias Current vs Input Power



Test Board Loss (Including Connectors)



Lead-Free 5 mm 32-Lead AQFN Package†



All dimensions shown as inches [mm].

† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 3 requirements.
Plating is NiPdAu.