Features

- Ultra Wideband Performance
- Noise Figure: 1.4 dB @ 8 GHz
- High Gain: 17.5 dB @ 8 GHz
- Output IP3: 27.5 dBm @ 8 GHz
- Bias Voltage: $V_{DD} = 5 - 6$ V
- Bias Current: $I_{DSQ} = 60 - 100$ mA
- 50 Ω Matched Input / Output
- Positive Voltage Only
- Lead-Free 5 mm 32-lead AQFN Package
- RoHS* Compliant

Description

The MAAL-011141 is an easy to use, wideband low noise distributed amplifier die. It operates from DC to 28 GHz and provides 17.5 dB of linear gain, 16 dBm of P1dB and 1.4 dB of noise figure at 8 GHz. The input and output are fully matched to 50 Ω with typical return loss >15 dB.

This amplifier employs an active termination circuit to achieve a lower noise figure at the lower end of the frequency range than is possible using traditional resistive termination techniques.

This product is fabricated using a GaAs pHEMT process which features full passivation for enhanced reliability.

The MAAL-011141 can be used as a low noise amplifier stage or as a driver stage in higher power applications. This device is ideally suited for Test and Measurement, EW, ECM, and Radar applications.

Ordering Information\(^1,2\)

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAAL-011141-TR0500</td>
<td>500 piece reel</td>
</tr>
<tr>
<td>MAAL-011141-001SMB</td>
<td>Sample Board</td>
</tr>
</tbody>
</table>

1. Reference Application Note M513 for reel size information.
2. All sample boards include 3 loose parts.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.
## Electrical Specifications: $T_A = +25^\circ C$, $V_{DD} = 6 \, V$, $I_{DSQ} = 75 \, mA$, $V_{AT} = 5 \, V$, $Z_0 = 50 \, \Omega$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Units</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
</tr>
</thead>
</table>
| **Gain**           | $P_{IN} = -20 \, dBm$  
  2.0 GHz  
  8.0 GHz  
  12.0 GHz  
  18.0 GHz  
  26.5 GHz | dB    | 16.0 | 18.0 | —    |
|                    |                                                                                  |       | 17.5 | 17.5 | —    |
|                    |                                                                                  |       | 17.5 | 17.5 | —    |
| **Output P1dB**    | 2.0 GHz  
  8.0 GHz  
  12.0 GHz  
  18.0 GHz  
  26.5 GHz | dBm   | —    | 17.0 | 16.0 | 15.5 |
|                    |                                                                                  |       | 15.5 | 12.0 | —    |
| **OIP3**           | $P_{IN} = -20 \, dBm$ / tone, 10 MHz Tone Spacing  
  2.0 GHz  
  8.0 GHz  
  12.0 GHz  
  18.0 GHz  
  26.5 GHz | dBm   | —    | 29.5 | 27.5 | 26.0 |
|                    |                                                                                  |       | 25.0 | 22.5 | —    |
| **Input Return Loss** | $P_{IN} = -20 \, dBm$ | dB    | —    | 15   | —    |
| **Output Return Loss** | $P_{IN} = -20 \, dBm$ | dB    | —    | 15   | —    |
| **Noise Figure**   | 2.0 GHz  
  8.0 GHz  
  12.0 GHz  
  18.0 GHz  
  26.5 GHz | dB    | —    | 2.7  | 1.4  | 1.5  |
|                    |                                                                                  |       | 2.2  | —    | 2.2  |
|                    |                                                                                  |       | 3.4  | —    | —    |
| **Isolation**      | $P_{IN} = -20 \, dBm$  
  2.0 GHz  
  8.0 GHz  
  12.0 GHz  
  18.0 GHz  
  26.5 GHz | dB    | —    | 55   | 40   | 37   |
|                    |                                                                                  |       | 35   | 33   | —    |
| **$V_G$**          | Adjusted to set $I_{DSQ} = 75 \, mA$ | V     | —    | 0.7  | —    |
| **$I_{AT}$**       | $V_{AT} = 5 \, V$ | mA    | —    | 10   | —    |
Operating Conditions
Recommended biasing conditions are $V_{DD} = 6$ V, $I_{DSQ} = 75$ mA. Bias of 5 V must be applied to $V_{AT}$ pin. $I_{DSQ}$ is set by adjusting $V_G$ after setting $V_{DD}$ and $V_{AT}$. The drain bias voltage range, $V_{DD}$, is 5 to 6 V, and the quiescent drain current biasing is 60 to 100 mA. To maintain the best performance MACOM recommends using an active bias circuit for constant $I_{DD}$.

There are three possible bias methods:

1. The use of an external bias tee where the required $V_{DD}$ is applied at RF OUT/VOID and $V_G$ is set to provide a current bias ($I_{DSQ}$) of 60 to 100 mA. This provides wide band performance of DC - 28 GHz (depending on the bandwidth of the bias tee).

2. The direct application of $V_{DD}$ to AUX1. Using this method provides for an operational frequency of 2 - 28 GHz. However, a voltage drop across an internal 17 $\Omega$ resistance and a 1.5 $\Omega$ typical series DC inductor resistance must be accounted for. For example, with $I_{DSQ} = 75$ mA, 7.4 V must be applied at AUX1 for a $V_{DD}$ of 6 V.

3. The direct application of $V_{DD}$ to AUX2. Using this method provides for an operational frequency of DC - 28 GHz. However, a voltage drop across series 17 $\Omega$ and 32 $\Omega$ resistors must be accounted for. For example, with $I_{DSQ} = 75$ mA, 9.67 V must be applied at AUX2 for a $V_{DD}$ of 6 V.

In all cases DC blocking is required on the RF input. Additionally options 2 and 3 require DC blocking on the RF output line. It should also be noted that when using the internal bias circuit (option 2 or 3) $I_{DSQ}$ is limited to a maximum of 80 mA.

Regardless of bias method used, a bypass capacitor of 0.1 $\mu$F should be connected to AUX2. This provides for increased device stability margins and improved gain flatness below 2 GHz when required. When using bias method 2, an 82 nH series inductor combined with a 0.1 $\mu$F shunt capacitor and 220 $\Omega$ resistor is recommended. This increases gain flatness below 2 GHz.

The available evaluation board is configured for bias option 3 using AUX2 for the supply of $V_{DD}$.

Maximum Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Operating Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Power $^5$</td>
<td>$P_{IN} \leq 1$ dB compression level</td>
</tr>
<tr>
<td>Junction Temperature $^6$</td>
<td>$+150^\circ C$</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>$-40^\circ C$ to $+85^\circ C$</td>
</tr>
</tbody>
</table>

5. MACOM does not recommend sustained operation at power levels above 1 dB gain compression.
6. Operating at nominal conditions with junction temperature $\leq +150^\circ C$ will ensure MTTF $> 1 \times 10^6$ hours.

Absolute Maximum Ratings $^7,^8$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Absolute Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Power</td>
<td>18 dBm</td>
</tr>
<tr>
<td>Drain Voltage</td>
<td>7 V</td>
</tr>
<tr>
<td>Gate Voltage</td>
<td>0.9 V</td>
</tr>
<tr>
<td>Active Termination Voltage</td>
<td>6 V</td>
</tr>
<tr>
<td>AUX1 Current</td>
<td>80 mA</td>
</tr>
<tr>
<td>AUX2 Current</td>
<td>80 mA</td>
</tr>
<tr>
<td>Junction Temperature $^9$</td>
<td>$+175^\circ C$</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>$-65^\circ C$ to $+125^\circ C$</td>
</tr>
</tbody>
</table>

7. Exceeding any one or combination of these limits may cause permanent damage to this device.
8. MACOM does not recommend sustained operation near these survivability limits.
9. Junction temperature directly effects device MTTF, and should be kept as low as possible to maximize product lifetime.

Handling Procedures
Please observe the following precautions to avoid damage:

Static Sensitivity
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A devices.
Applications Section: Sample board layout for bias option 3 using AUX2

Cut trace for AUX2 operation

Parts List

<table>
<thead>
<tr>
<th>Part</th>
<th>Value</th>
<th>Case Style</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1 - C4</td>
<td>0.1 µF</td>
<td>0402</td>
</tr>
<tr>
<td>R1</td>
<td>220 Ω</td>
<td>0402</td>
</tr>
<tr>
<td>R2</td>
<td>0 Ω</td>
<td>0402</td>
</tr>
<tr>
<td>L1</td>
<td>82 nH</td>
<td>0402</td>
</tr>
</tbody>
</table>

Evaluation PCB Specifications

Top Layer: 1/2 oz Copper Cladding, 0.017 mm thickness
Dielectric Layer: Rogers RO4003C 0.203 mm thickness
Bottom Layer: 1/2 oz Copper Cladding, 0.017 mm thickness
Finished overall thickness: 0.237 mm
Sample Board Layout: Input and Output Tuning

All units are in microns

Evaluation PCB Specifications

Top Layer: 1/2 oz Copper Cladding, 0.017 mm thickness
Dielectric Layer: Rogers RO4003C 0.203 mm thickness
Bottom Layer: 1/2 oz Copper Cladding, 0.017 mm thickness
Finished overall thickness: 0.237 mm

10. Input and output use the same tuning.
Typical Performance Curves: $V_{DD} = 6$ V, $I_{DSQ} = 75$ mA, $V_{AT} = 5$ V

**Gain**

![Gain Graph](image)

**Noise Figure**

![Noise Figure Graph](image)

**Input Return Loss**

![Input Return Loss Graph](image)

**Output Return Loss**

![Output Return Loss Graph](image)

**Low Frequency S-Parameters**

![Low Frequency S-Parameters Graph](image)

**Reverse Isolation**

![Reverse Isolation Graph](image)
Low Noise Amplifier
DC - 28 GHz

Typical Performance Curves: $V_{DD} = 6$ V, $I_{DSQ} = 75$ mA, $V_{AT} = 5$ V

**Output P1dB**

**Output IP3 (10 MHz tone spacing)**
**Lead-Free 5 mm 32-Lead AQFN Package†**

All dimensions shown as inches [mm].

† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 3 requirements.
Plating is NiPdAu.
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