Low Noise Amplifier
0.7 - 6.0 GHz

MAAL-011134-CQ3
Rev. V1

Features

- Broad 0.7-6 GHz Performance
- Tuning Optimizes Narrower Bands
- Low Noise Figure: 0.7 dB @ 2 GHz
- High Gain: 26 dB @ 2 GHz (tuned)
- Single Voltage Bias: 3 - 5 V
- Integrated Active Bias Circuit
- Lead-Free 3 mm 12-Lead Ceramic QFN Package
- Hermetically Sealed
- Hydrogen Getter Included Inside Package
- RoHS* Compliant

Description

The MAAL-011134-CQ3 is a high dynamic range, single stage MMIC LNA designed to operate from 700 MHz - 6 GHz assembled in a lead-free 3 mm 12-LD ceramic QFN plastic package. This amplifier has low noise figure, high gain and excellent linearity. In the 50 Ω environment and at 3 V, this device offers less than 0.6 dB noise figure at 2 GHz, with 25 dB of gain and 31 dBm output IP3.

This low noise amplifier has an integrated active bias circuit allowing direct connection to 3 V or 5 V bias and minimizing variations over temperature and process. The bias current is set by an external resistor, so the user can customize the power consumption to fit the application. V_{BIAS} can be utilized as an enable pin to power the device up and down during operation.

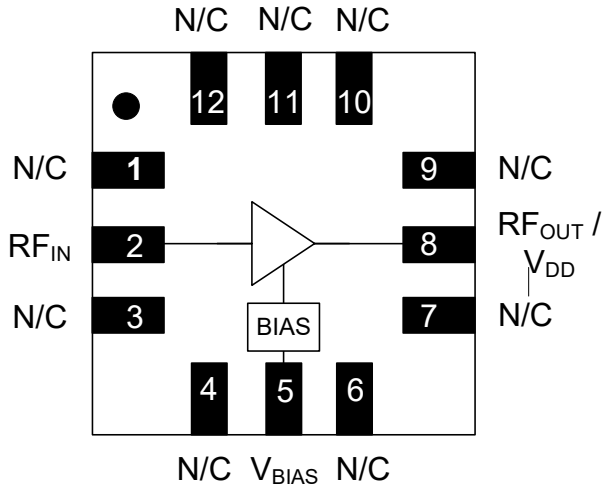
This MAAL-011134-CQ3 is may be used in many applications due to the wide bandwidth and may be optimize for narrower bands with external tuning.

Ordering Information[1,2]

Part Number	Package
MAAL-011134-CQ3	Samples
MAAL-011134-CQ3SB1	Sample Board Broadband
MAAL-011134-CQ3SB2	Sample Board 2.05 GHz

1. Reference Application Note M513 for reel size information.

Functional Block Diagram



Pin Configuration[2]

Pin #	Pin Name	Description
1,3,4,6,7, 9-12	N/C	No Connection
2	RF_{IN}	RF Input
5	V_{BIAS}	Bias Voltage
8	RF_{OUT} / V_{DD}	RF Output / Drain Voltage
backside	Pad[3]	Ground

2. MACOM recommends connecting all No Connection (N/C) pins to ground.
3. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications: Broadband Operation, Freq = 5.8 GHz, V_{DD} = 3 V, +25ºC, Z_0 = 50 Ω, R_{BIAS} = 680 Ω[4]

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Noise Figure	—	dB	—	1.1	1.7
Gain[5]	—	dB	12.5	14.5	—
Input Return Loss[5]	—	dB	—	8	—
Output Return Loss[5]	—	dB	—	4	—
Output IP3[5]	P_{IN} = -22 dBm per tone, 11 MHz spacing	dBm	—	31	—
Output P1dB	—	dBm	—	16	—
Current	$I_{DQ} + I_{BIAS}$	mA	—	51	72

Electrical Specifications: Broadband Operation, Freq = 5.8 GHz, V_{DD} = 5 V, +25ºC, Z_0 = 50 Ω, R_{BIAS} = 680 Ω[4]

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Noise Figure	—	dB	—	1.0	—
Gain[5]	—	dB	—	14.9	—
Input Return Loss[5]	—	dB	—	4	—
Output Return Loss[5]	—	dB	—	5.5	—
Output IP3[5]	P_{IN} = -22 dBm per tone, 11 MHz spacing	dBm	—	32	—
Output P1dB	—	dBm	—	19	—
Current	$I_{DD} + I_{BIAS}$	mA	—	91	—

4. Current may be adjusted by through R_{BIAS} value. See biasing section for more information.
5. Performance can be optimized over narrower bands using matching circuits provided in the applications sections.

Maximum Operating Conditions

Parameter	Maximum
RF Input Power CW	6 dBm
V_{DD}	5.5 V
V_{BIAS}	4.5 V
Operating Temperature	-40ºC to +105ºC
Junction Temperature[6,7]	+150ºC

6. Operating at nominal conditions with $T_J \leq 150°C$ will ensure MTTF > 1 x 10^6 hours.
7. Junction Temperature (T_J) = T_C + Θ_{JC} * ((V * I) - (P_{OUT} - P_{IN}))
   Typical thermal resistance (Θ_{JC}) = 83°C/W
   a) For T_C = +25°C,
   T_J = 38°C @ 3 V, 0.051 A, P_{OUT} = 0 dBm, P_{IN} = -20 dBm
   b) For T_C = +85°C,
   T_J = 98°C @ 3 V, 0.051 A, P_{OUT} = 0 dBm, P_{IN} = -20 dBm

Absolute Maximum Ratings[8,9]

Parameter	Absolute Maximum
RF Input Power CW	18 dBm
V_{DD}	6 V
V_{BIAS}	5 V
Storage Temperature	-55ºC to +150ºC

8. Exceeding any one or combination of these limits may cause permanent damage to this device.
9. MACOM does not recommend sustained operation near these survivability limits.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Pin Descriptions

Pin #	Pin Name	Description
1,3,4,6,7,9-12	N/C	No internal Connection, Grounding this pin on the board is recommended to maximize isolation.
2	RF_{IN}	RF Input , an external DC block is required
5	V_{BIAS}	Bias Voltage. Change the bias resistor value to adjust the DC current. See the Bias Table on page 5.
8	RF_{OUT} / V_{DD}	RF Output / Drain Voltage, external bias tee required (see Figure 1)
Pad	Pad	Ground with as many board vias as practical, starting at the perimeter of the paddle

Biasing Options

The MAAL-011134-CQ3 bias can be set in 2 different ways: using only V_{DD} or using separate V_{DD} and V_{BIAS} voltages. A separate V_{BIAS} voltage allows pin 5 (V_{BIAS}) to be used as an enable pin to power the device up and down during operation.

For both bias methods select the value of R_{BIAS} to achieve the desired current based on the tables on page 4, and use DC blocks at pin 2 (RF_{IN}) and pin 8 (RF_{OUT} / V_{DD}).

Biasing Option - V_{DD} only

To use only V_{DD}, connect pin 8 (RF_{OUT} / V_{DD}) to V_{DD} through an RF choke inductor and connect pin 5 (V_{BIAS}) to V_{DD} through bias resistor R_{BIAS} as shown in Figure 1.

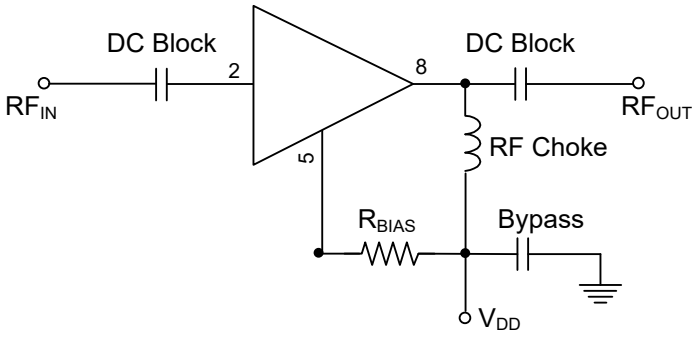


Figure 1

Biasing Option - Separate V_{DD} and V_{BIAS} Voltages ($V_{BIAS} \leq V_{DD}$)

To use separate V_{DD} and V_{BIAS} voltages, connect pin 8 (RF_{OUT} / V_{DD}) to V_{DD} through an RF choke inductor and connect pin 5 (V_{BIAS}) to V_{BIAS} through bias resistor R_{BIAS} as shown in Figure 2. Typical current (I_{BIAS}) draw for pin 5 (V_{BIAS}) is 1.4 mA @ V_{BIAS} = 3 V and 1 µA @ V_{BIAS} = 0 V. Typical current (I_{DD}) draw for pin 8 (RF_{OUT} / V_{DD}) is < 1 µA @ V_{BIAS} = 0 V.

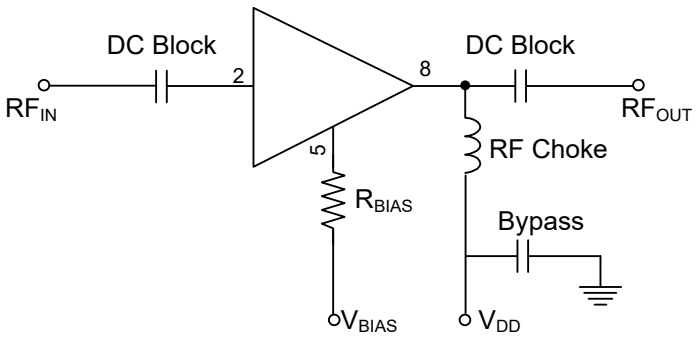
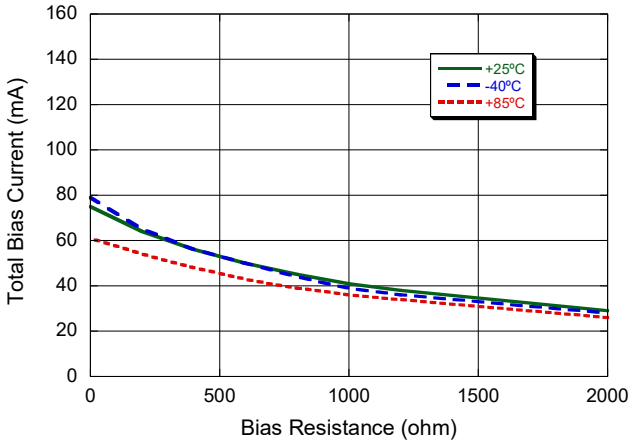


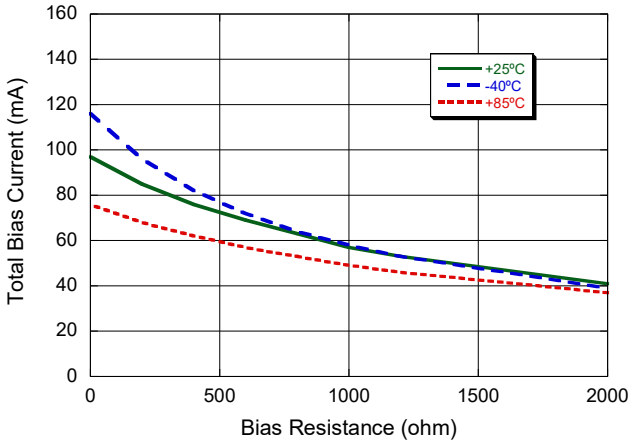
Figure 2

Typical Performance Curves of the Active Bias Circuit

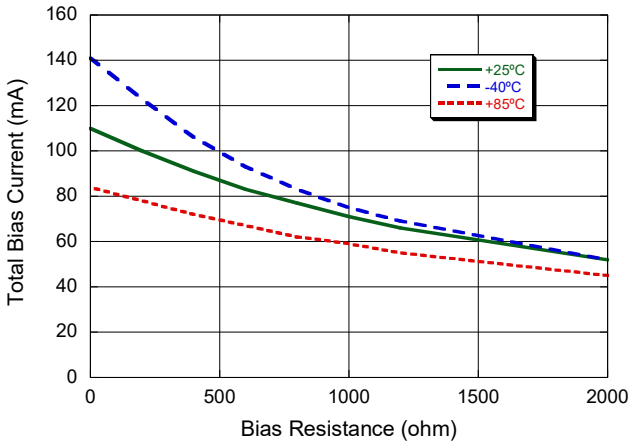
Current, V_{DD} = 3 V



Current, V_{DD} = 4 V



Current, V_{DD} = 5 V

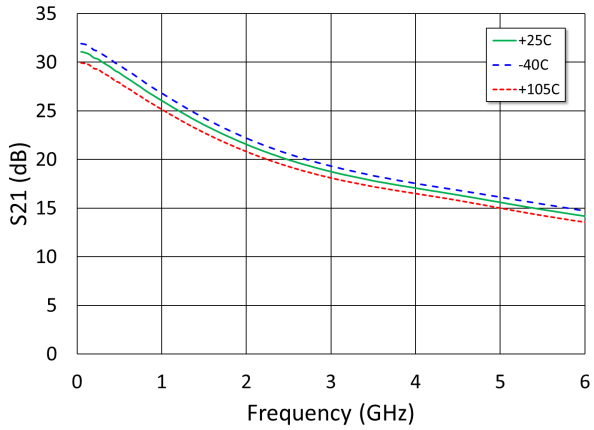


Bias Table

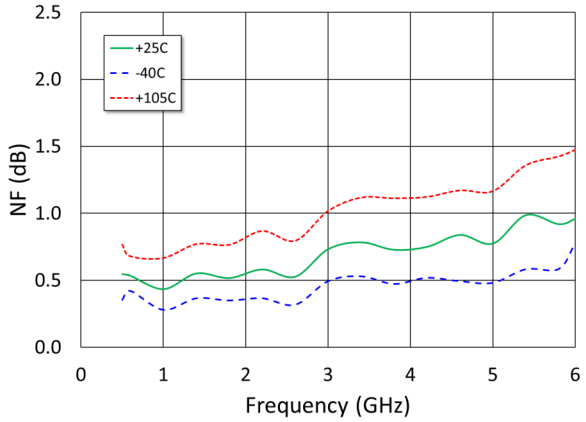
Bias Resistance (Ω)	Total Current (mA)								
	V_{DD} = 3 V			V_{DD} = 4 V			V_{DD} = 5 V		
	+25°C	-40°C	+85°C	+25°C	-40°C	+85°C	+25°C	-40°C	+85°C
2000	29	28	26	41	39	37	52	52	45
1200	38	36	34	53	53	46	66	69	55
1000	41	39	36	57	58	49	71	75	59
800	45	44	39	63	64	53	77	83	62
600	50	50	43	69	72	57	83	93	67
400	56	56	48	76	82	62	91	106	72
200	64	65	54	85	96	68	100	123	78
0	75	79	61	97	116	76	110	141	84

Typical Performance Curves @ 3 V / 51 mA, Z_0 = 50 Ω

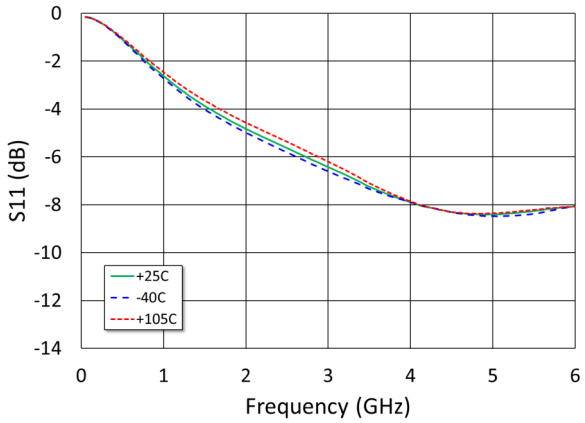
Gain



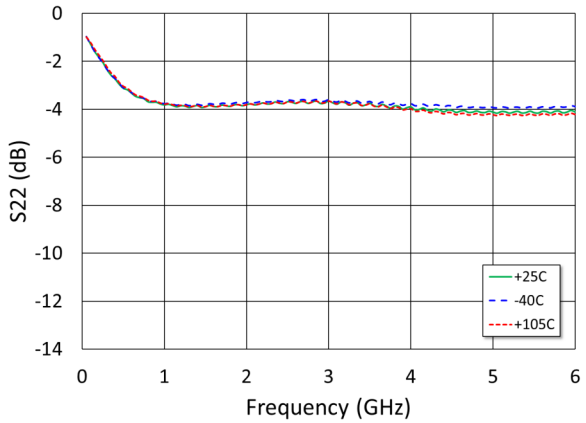
Noise Figure



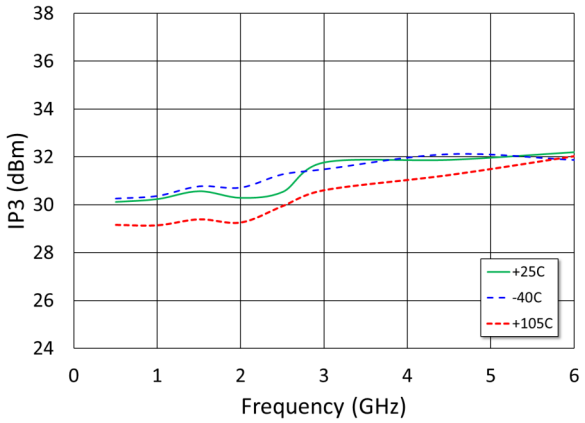
Input Return Loss



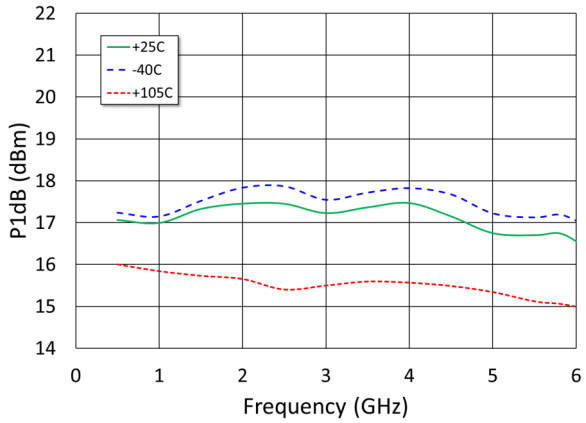
Output Return Loss



Output IP3

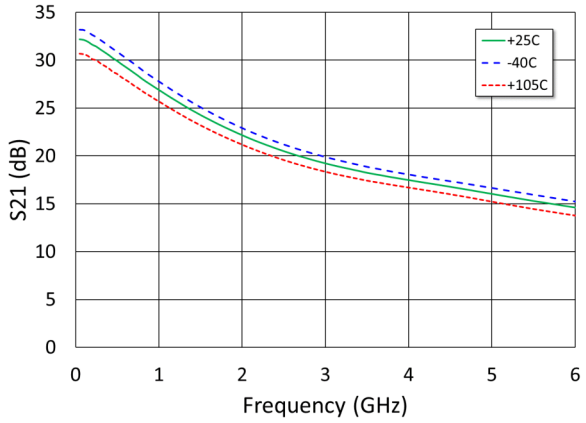


P1dB

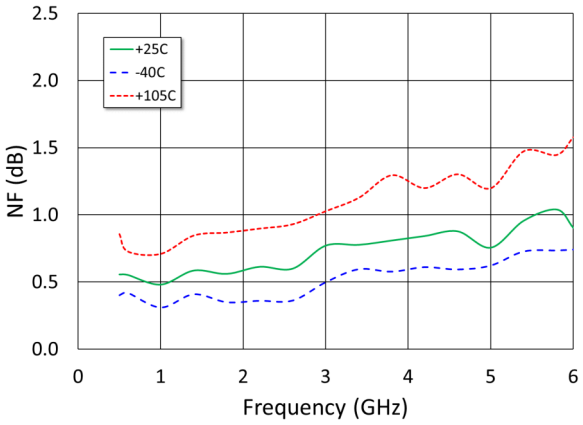


Typical Performance Curves @ 5 V / 91 mA, Z_0 = 50 Ω

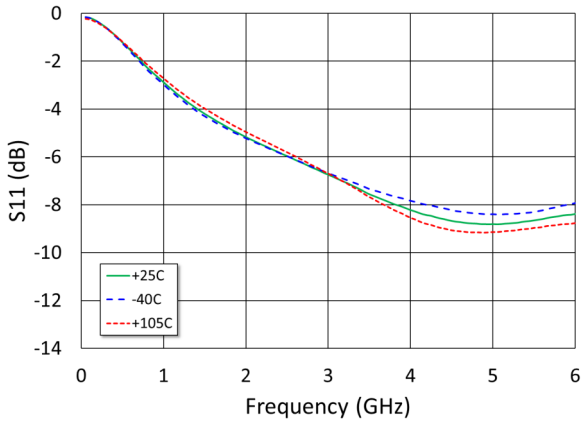
Gain



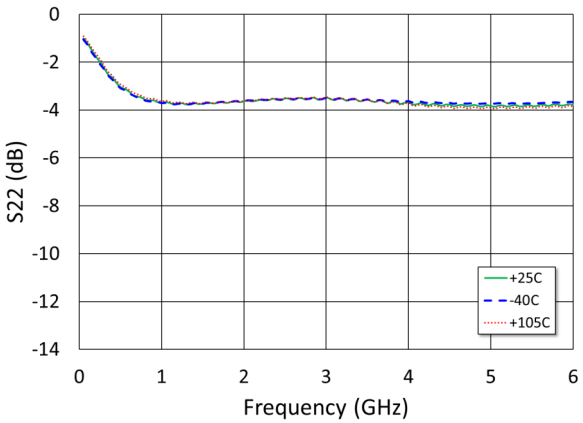
Noise Figure



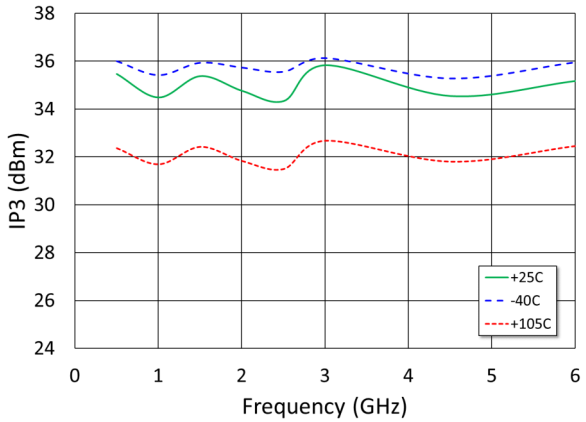
Input Return Loss



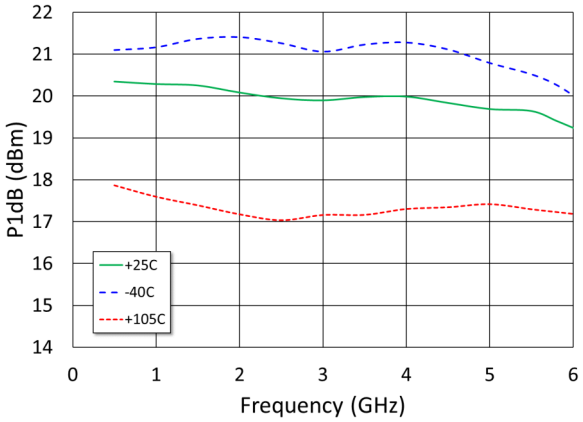
Output Return Loss



Output IP3



P1dB



2.0 - 2.1 GHz Application Section

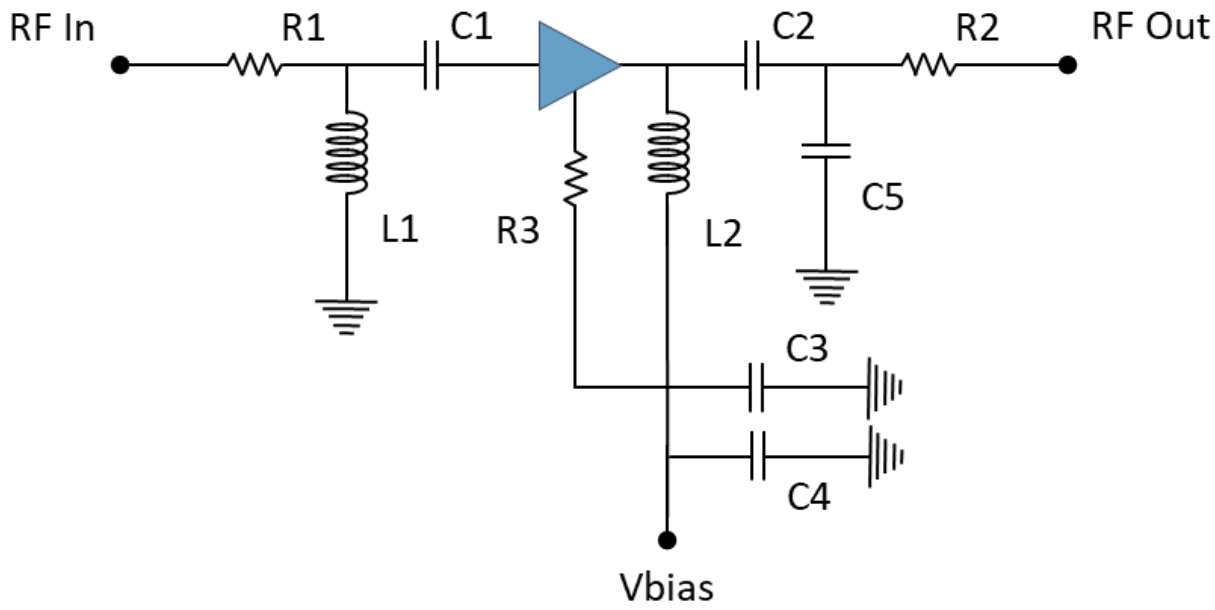
The MAAL-011134-CQ3 is designed to work as a low noise gain block over a wide range of frequencies in a 50 Ω environment.

Input and output can be tuned to improve return loss over a specific frequency band.

The evaluation board shown has been designed for tuning flexibility. The parts list on page 9 details the components needed to tune the MAAL-011134-CQ3 for operation from 2.0 - 2.1 GHz. R1 may be used as R_{BIAS} according to the biasing option chosen.

Evaluation Board, 2.0 - 2.1 GHz

Schematic, 2.0 - 2.1 GHz



Parts List: 2.0 - 2.1 GHz

Component	Value	Size	Manufacturer	Manufacturer Part #
C1	100 pF	0402	Murata	GRM1555C1H101JA01
C2	1 pF	0402	Murata	GJM1555C1H1R0BB01
C3	100 pF	0402	Murata	GRM1555C1H101JA01
C4	0.1 µF	0402	Murata	GRM155R71C104K
C5	DNP	—	—	—
L1	2.2 nH	0402	Coilcraft	0402HP-2N2XJRW
L2	2.4 nH	0402	Coilcraft	0402CS-2N4XJBU
R1	0 Ω	0402	Panasonic	ERJ-2GE0R00X
R2	0 Ω	0402	Panasonic	ERJ-2GE0R00X
R3	680 Ω	0402	Vishay Dale	CRCW0402-681JRT7

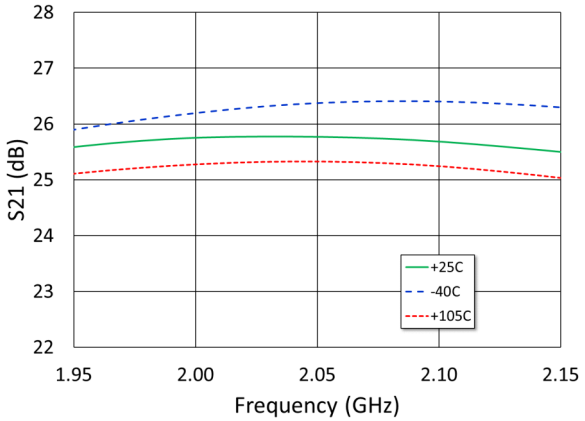
Electrical Specifications[10]: Freq = 2.05 GHz, V_{DD} = 3.4 V, +25ºC, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Noise Figure	—	dB	—	0.7	—
Gain	—	dB	—	26	—
Input Return Loss	—	dB	—	18	—
Output Return Loss	—	dB	—	15	—
Output IP3	P_{IN} = -22 dBm per tone, 11 MHz spacing	dBm	—	30	—
Output P1dB	—	dBm	—	11.5	—
Current	$I_{DD} + I_{BIAS}$	mA	—	59	—

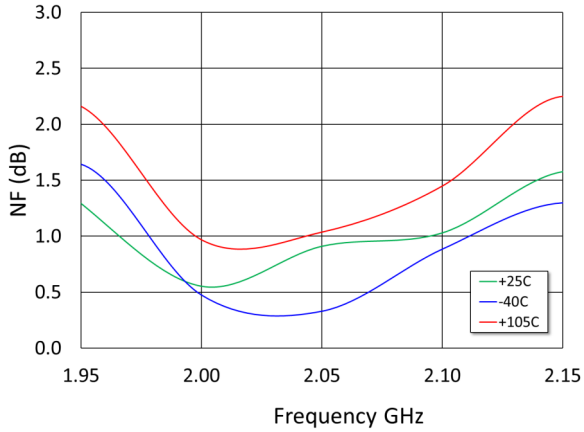
10. Tuned to 2.05 GHz using schematic and part list shown above.

Typical Performance Curves @ 3.4 V / 59 mA, Z_0 = 50 Ω

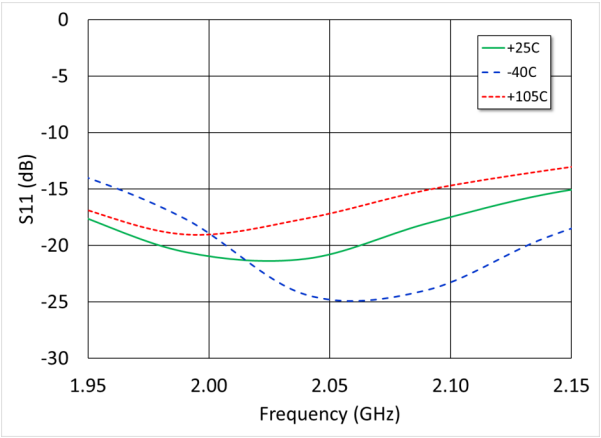
Gain



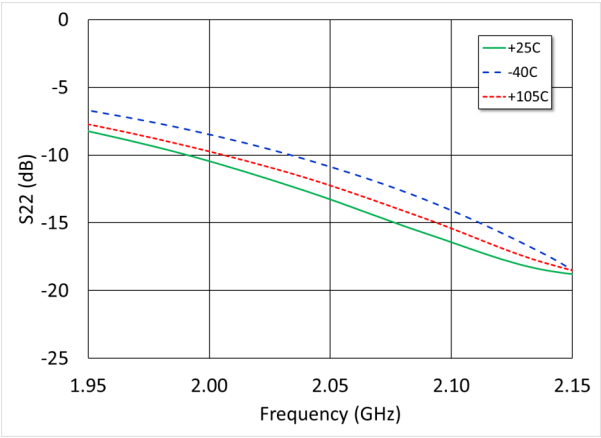
Noise Figure



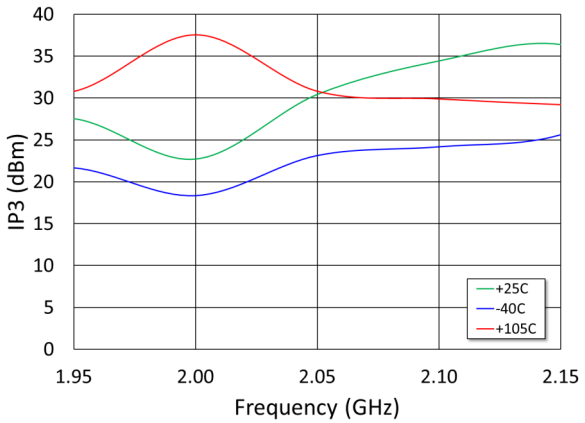
Input Return Loss



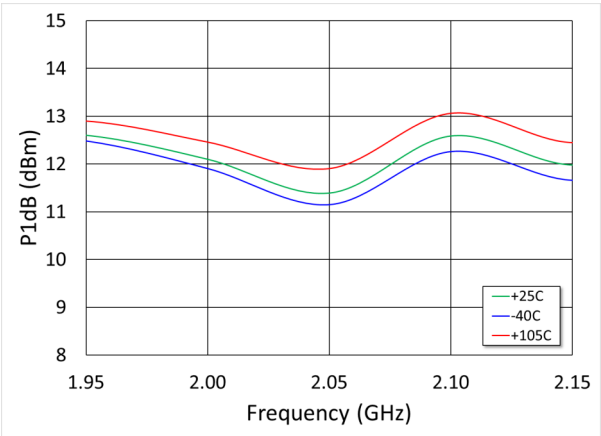
Output Return Loss



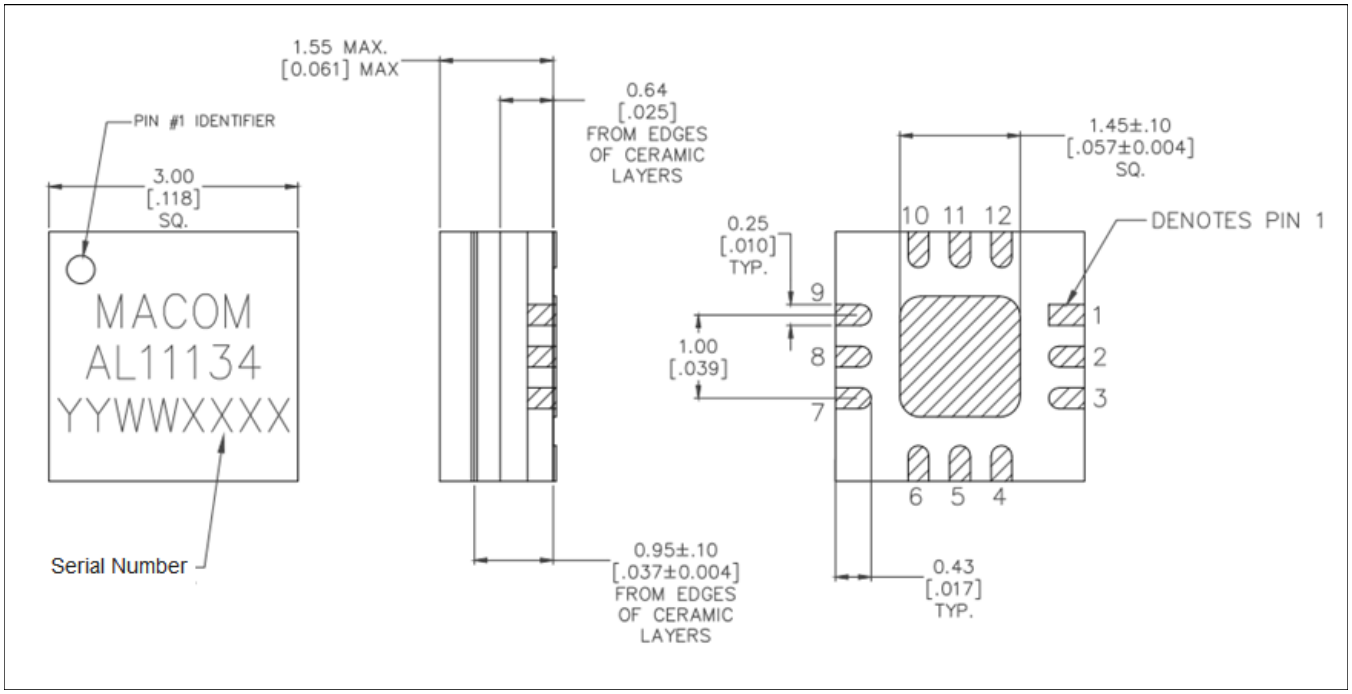
Output IP3



P1dB



Lead-Free Hermetic 3 mm 12-Lead QFN Ceramic Package†



† Plating is ENEPIG
Reference Application Note S2083 for surface mount instructions for QFN packages