MAAL-010705-CR10

Low Noise Amplifier
0.5 - 3 GHz

Rev. V1

Features

- Low Noise Figure
- Excellent Input Return Loss
- Single Voltage Bias 4 V
- Integrated Active Bias Circuit
- Current Adjustable 20 - 80 mA with an External Resistor
- High Linearity, OIP3 >32 dBm
- 8-Lead Hermetic Package
- RoHS* Compliant

Description

The MAAL-010705-CR10 is a high dynamic range single stage MMIC LNA with excellent linearity and low noise figure designed for operation from 0.5 to 3 GHz. The LNA is packaged in an RoHS compliant, 8-lead hermetically sealed ceramic package.

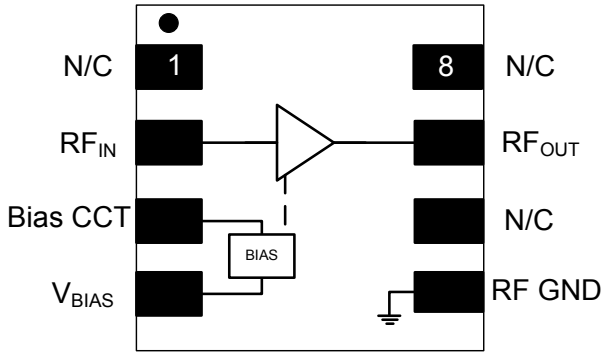
This MMIC has an integrated active bias circuit allowing direct connection to 4 V voltage supply and minimizing variation over temperature and process. The bias current and gain can be set with external resistors to allow the user to customize the current and gain value to fit the application.

The MAAL-010705-CR10 offers less than 0.7 dB noise figure, more than 32 dBm OIP3 and 20 dB output return loss. The excellent match, low noise figure and high OIP3 along with the flexibility of setting current and gain make this LNA ideal UHF, L, and S-band satellite applications.

Ordering Information

Part Number	Package
MAAL-010705-CR10	Chip Scale Package

Functional Block Diagram



Pin Configuration[1]

Pin No.	Pin Name	Description
1	N/C	No Connection
2	RF_{IN}	RF Input
3	Bias CCT	Bias Circuit Reference
4	V_{BIAS}	Bias Voltage
5	RF GND	RF Ground
6	N/C	No Connection
7	RF_{OUT}	RF Output
8	N/C	No Connection

1. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

Electrical Specifications[2]: Freq = 0.9 GHz, V_D = 4 V, 25°C, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	—	dB	18	21	—
Input Return Loss	—	dB	—	15	—
Output Return Loss	—	dB	—	27	—
Noise Figure	—	dB	—	0.7	—
Output IP3	P_{OUT} = 5 dBm, Tone Spacing = 1 MHz	dBm	—	33	—
Output P1dB	—	dBm	17.5	18.5	—
Total Current	$I_{DQ} = I_D + I_{BIAS}$	mA	—	60	70

2. V_D and V_{BIAS} are connected together to 4 V, R3 = 150 Ω and R4 = 240 Ω; reference recommended schematic on page 5.

Absolute Maximum Ratings[3,4]

Parameter	Absolute Max.
Voltage	5.5 V
Current	100 mA
RF Input Power	20 dBm
Storage Temperature	-55ºC to +150ºC
Operating Temperature	-40ºC to +85ºC
Junction Temperature[5]	+150ºC

3. Exceeding any one or combination of these limits may cause permanent damage to this device.
4. MACOM does not recommend sustained operation near these survivability limits.
5. Typical thermal resistance (Θjc) = 45°C/W.

Handling Procedures

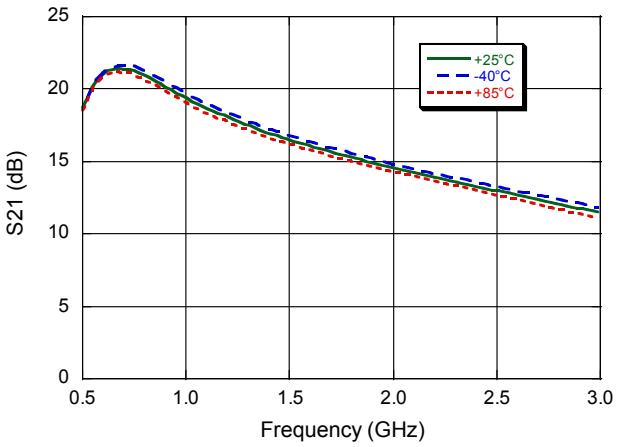
Please observe the following precautions to avoid damage:

Static Sensitivity

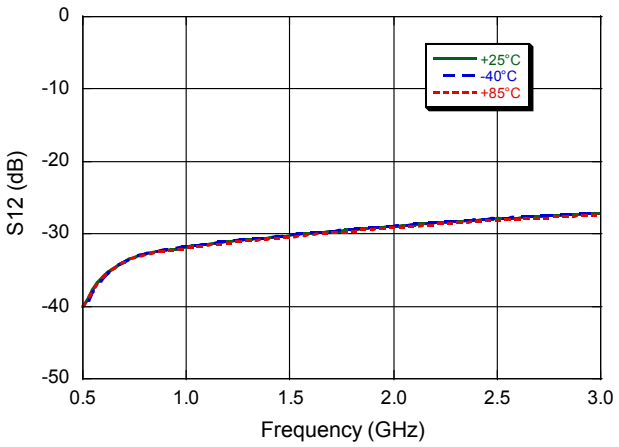
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Typical Performance Curves: 4 V (over temperature)

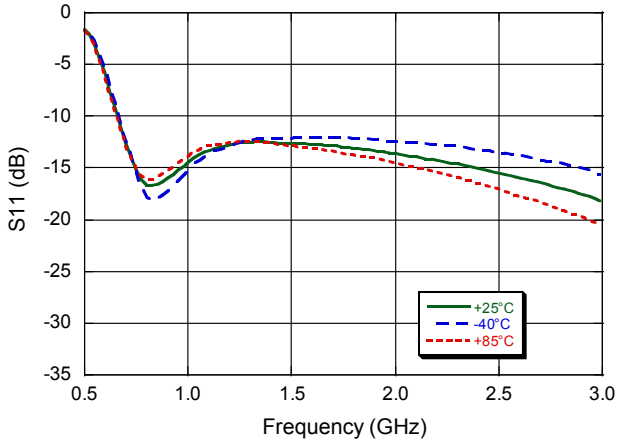
Gain



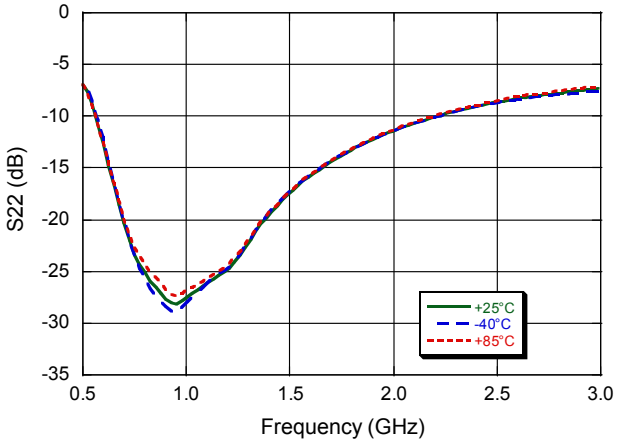
Reverse Isolation



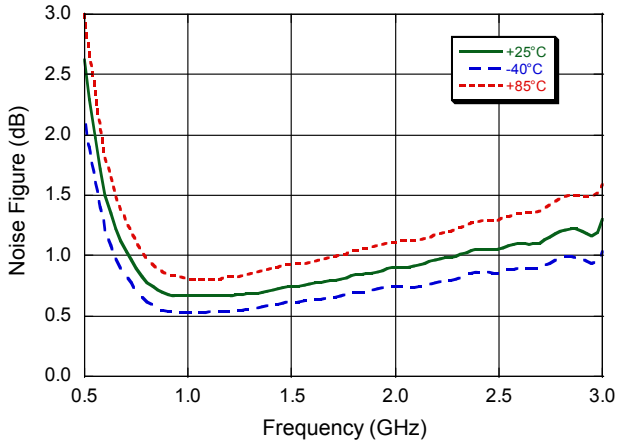
Input Return Loss



Output Return Loss

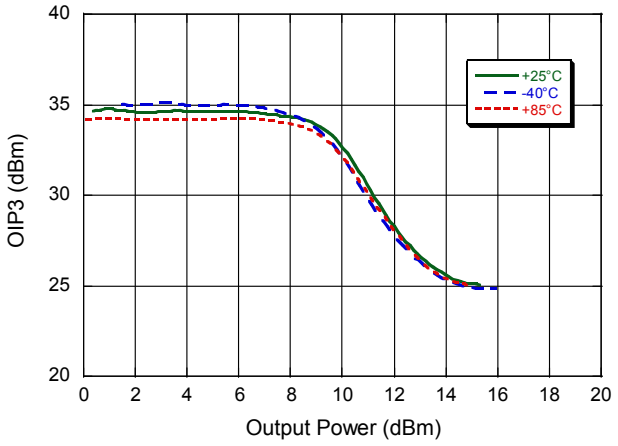


Noise Figure

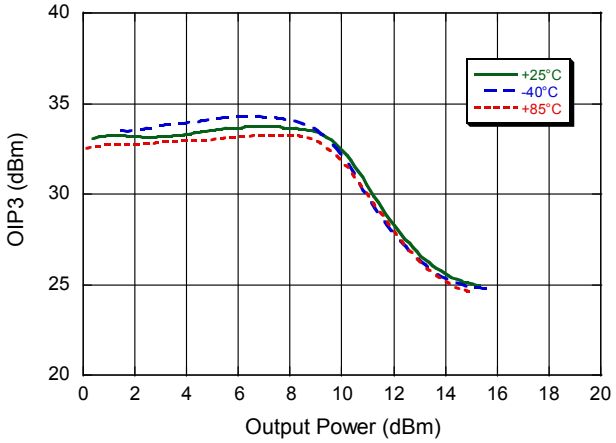


Typical Performance Curves @ 900 MHz, 4 V

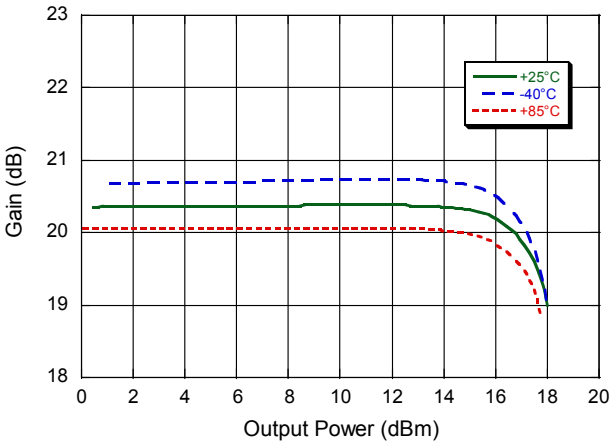
OIP3 High vs. Output Power



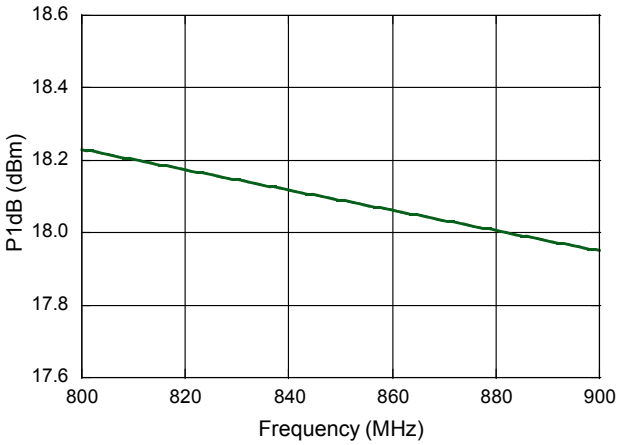
OIP3 Low vs. Output Power



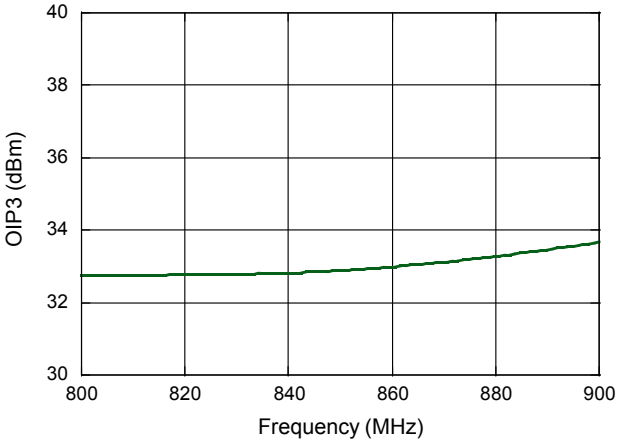
Gain vs. Output Power



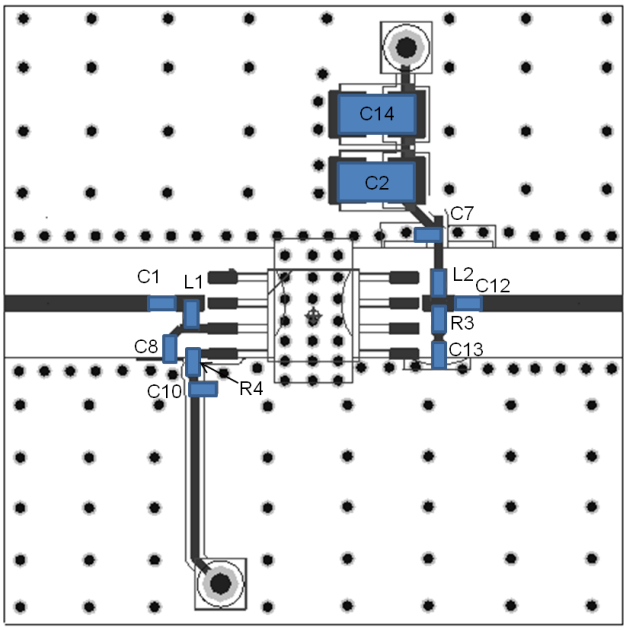
P1dB vs. Frequency



OIP3 vs. Frequency



Recommended Layout



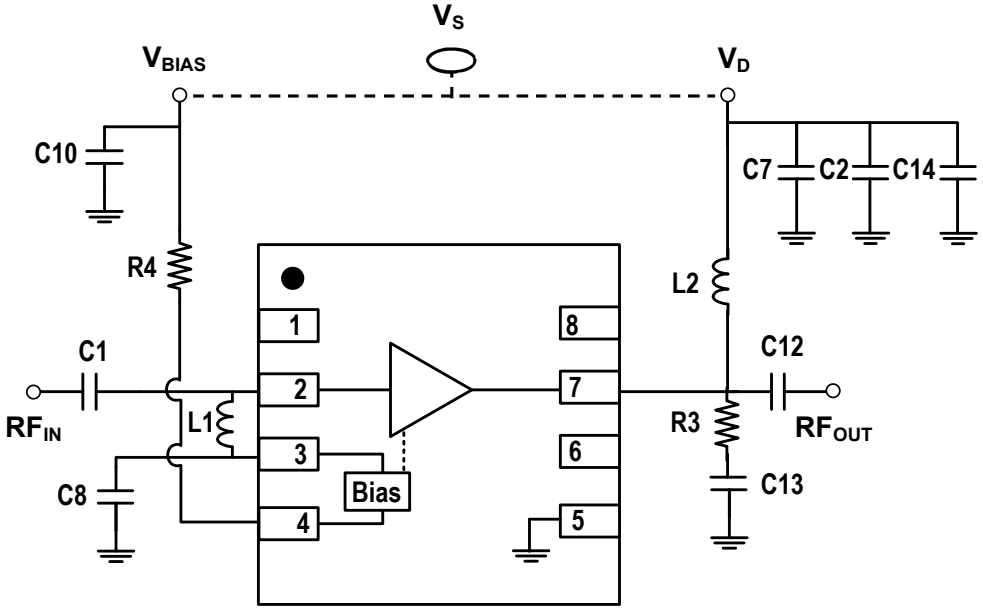
Off-Chip Component Values

Component	Value	Package
C1	3.3 pF	0402
C7, C8, C10	1000 pF	0402
C12, C13	100 pF	0402
C2, C14	4.7 µF	Tantalum, 1210
L1	9 nH	0402
L2	15 nH	0402
R3	150 Ω	0402
R4	240 Ω	0402

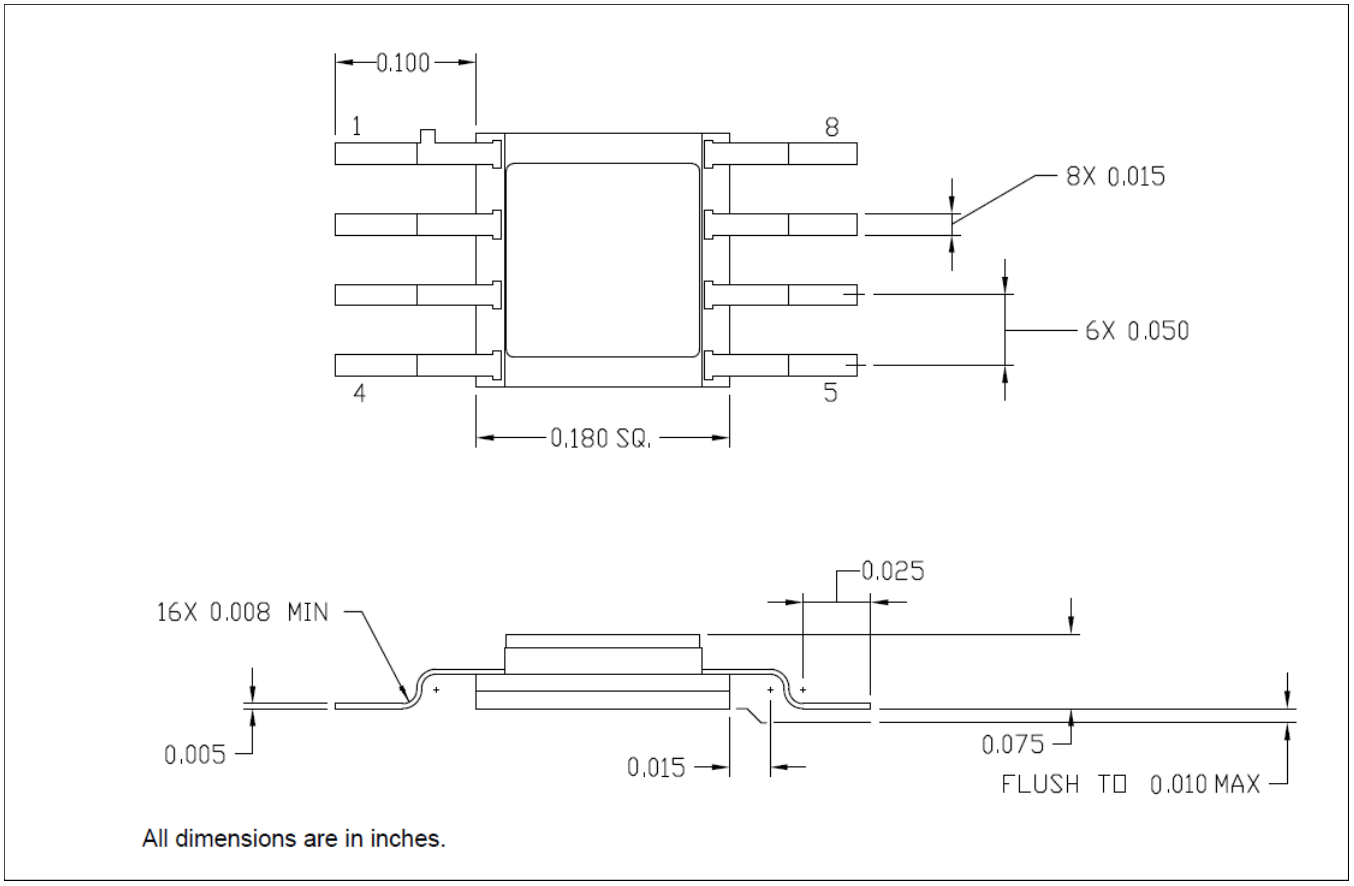
Bias Information

V_{BIAS} and V_D are separate connections on the evaluation board to give the option of varying I_D without changing R4. They can be connected together to a single voltage supply during the measurement and in the final layout implementation of the PCB. If two different voltage supplies are used then apply V_D first and then V_{BIAS} to turn on the LNA. To turn off the LNA disconnect V_{BIAS} first and then V_D. R3 is varied to obtain different levels of gain. R4 is varied to change the drain current Id.

Schematic



Lead-Free Hermetic CR10 Package†



† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 1 requirements.
Plating is Au over Ni.