M21404-13/M21414-13/M21424-13

SD, HD, and 3G Cable Equalizers

Rev V6

Applications

- SDI Routers
- SDI Switches
- SDI Distribution Amplifier
- SDI Camera

Standards Compliance

- SMPTE 259M, SMPTE 292, SMPTE 344M, SMPTE 424M (at appropriate data rates)
- DVB-ASI (270 Mbps)

Features

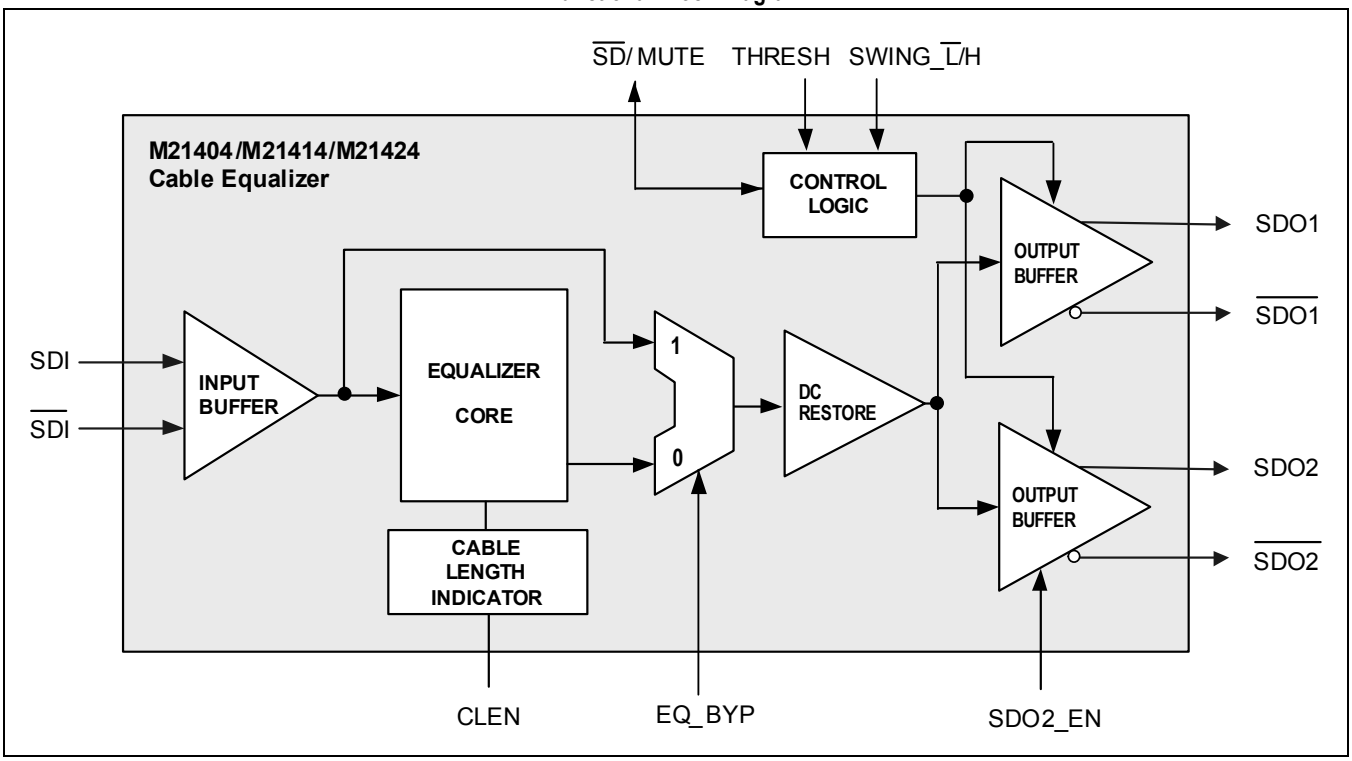
- SMPTE/DVB-ASI compliant at SD, HD and 3G (M21424)
- SMPTE/DVB-ASI compliant at SD and HD (M21414)
- SMPTE/DVB-ASI compliant at SD (M21404)
- Dual CML outputs, with selectable high amplitude
- Enable for second CML output
- Interchangeable PCB footprint for all three devices
- 3.3V Supply
- Low Power (230 mW @ 3.3V)
- Extended Temperature range: –10 to 85°C

The M21404/M21414/M21424 are high-speed, low-power, adaptive co-axial cable equalizers designed to increase the maximum low-jitter transmission distance of serial digital interface (SDI) video signals and DVB-ASI across commonly used bandwidth-limiting 75Ω coaxial cable. These devices automatically optimize their transfer function based on the bit rate and cable length to minimize the inter-symbol interference (ISI) jitter caused by the cable and to remove the DC offset components introduced with the pathological test pattern and AC coupling in systems.

The M21424 is designed to support SD, HD, and 3G data rates from 143 Mbps to 2970 Mbps. The M21414 is designed to support SD and HD data rates from 143 Mbps and 1485 Mbps. The M21404 is designed to support SD data rates between 143 Mbps and 540 Mbps.

The low-noise, high-gain equalizer allows for low jitter 3G-SDI transmissions up to 100m (Belden 1694A) and HD transmissions up to a length of 200m (Belden 1694A) and 120m (Belden 8281). For SD data rates, cable lengths up to 400m (Belden 1694A) and 300m (Belden 8281) are supported.

Functional Block Diagram



Ordering Information

Part Number	Package	Operating Data Rate	Operating Temperature
M21404G-13*	32-pin MLF (RoHS compliant)	143–540 Mbps	–10°C to 85°C
M21414G-13*	32-pin MLF (RoHS compliant)	143–1485 Mbps	–10°C to 85°C
M21424G-13*	32-pin MLF (RoHS compliant)	143–2970 Mbps	–10°C to 85°C

* Consult the price list for exact part number when ordering.

* The letter 'G' designator after the part number indicates a RoHS-compliant package.

Revision History

Revision	Level	Date	Description
V6	Release	December 2015	Updated Package Drawing, Figure 1-3. Package effective as of July 2014.
V5	Release	May 2015	Updated logos and page layout. No content changes.
F (V4)	Release	October 2013	Removed 2.5V operation
E (V3)	Release	November 2010	Updated Package Diagram (Figure 1-3).
D (V2)	Release	March 2010	Revised for -13 part.
C (V1)	Release	April 2007	Production release. Correction made to the Functional Block Diagram. Specification changes to Tables 1-3, 1-5, 1-6, and 1-7.
B (V1P)	Preliminary	February 2007	Combined data sheets for the M21404, M21214 and M21424. Removed 1.8V operation. Removed CLI and MUTE threshold specification.
A (V1A)	Advance	April 2006	Initial Release.

M21404/M21414/M21424 Marking Diagram

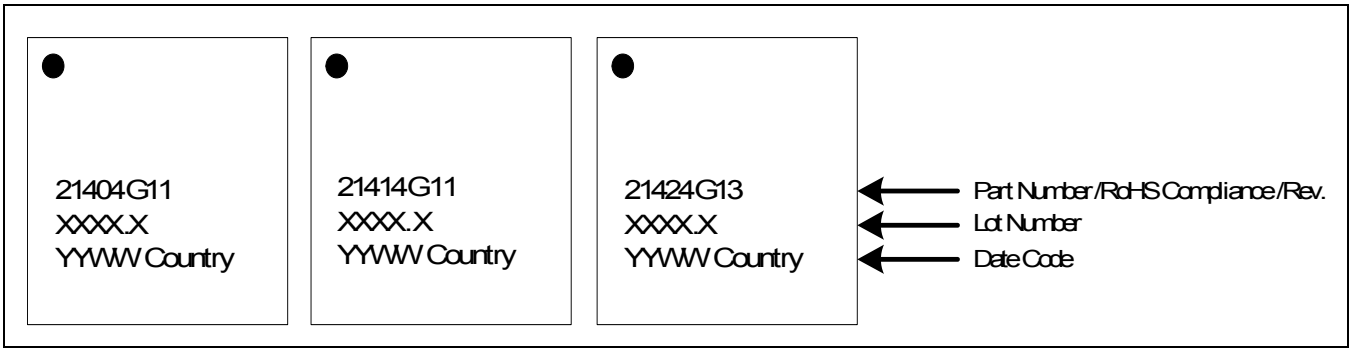


Table of Contents

List of Figures

List of Tables

1.0 Product Specification

1.1 General Specifications

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Units
AV_{DD}	Positive Supply	AV_{SS} - 0.5	AV_{SS} + 3.6	V
V_{IN}	DC Input Voltage (PCML)	AV_{SS} - 0.5	AV_{DD} + 0.5	V
T_{STORE}	Storage Temperature	–65	+150	°C
$V_{ESD, HBM}$	Human Body Model (low-speed)	2000	—	V
$V_{ESD, HBM}$	Human Body Model (high-speed)	2000	—	V
$V_{ESD, CDM}$	Charge Device Model	500	—	V

NOTE:

1. No Damage.

Table 1-2. Recommended Operating Conditions

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
AV_{DD}	Supply Voltage	—	3.135	3.3	3.465	V
T_{AMB}	Ambient Temperature	—	–10	—	+85	°C
θ_{JA}	Junction to Ambient Thermal Resistance	1, 2	—	40	—	°C/W

NOTES:

1. Mounted on multi layer board (≥ 4 layers).
2. Airflow = 0.0 m/s.

Table 1-3. Power DC Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
I_{DD}	Supply Current	1	—	70	90	mA
P_{TOTAL}	Total Power Dissipation (@3.3V)	1, 2, 3	—	230	312	mW

NOTES:

1. Specified at recommended operating conditions—See Table 1-2.
2. Includes on-chip power dissipation as well as off-chip power dissipated by termination resistors.
3. Typical calculated at nominal supply voltage, maximum calculated at nominal supply voltage + 5%.

1.2 Input/Output Level Specifications

Table 1-4. CMOS Input Electrical Specifications (Logic Signals Only)

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
V_{IH}	Input Logic High Voltage	1	0.75 x AV_{DD}	—	AV_{DD} + 0.3	V
V_{IL}	Input Logic Low Voltage	1	0	—	0.25 x AV_{DD}	V
I_{IH}	Input Current (logic high)	1	–100	—	100	µA
I_{IL}	Input Current (logic low)	1	–100	—	100	µA

NOTE:

1. Specified at recommended operating conditions—See Table 1-2. Spec is for a max load of 20 pF.

Table 1-5. High Speed Input Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DR	Input Bit Rate (M21404)	1	143	—	540	Mbps
	Input Bit Rate (M21414)	1	143	—	1485	Mbps
	Input Bit Rate (M21424)	1	143	—	2970	Mbps
V_{IN}	Input Voltage Range with 0m of cable, p-p, AV_{DD} = 3.3V	1, 5	700	800	1200	mV
V_{ICM}	Input Common-Mode Voltage (AV_{DD} = 3.3V)	1, 4	—	2.75	—	V
C_{IN}	Input capacitance	1, 4	—	0.5	—	pF
R_{IN}	Input resistance	1, 4	—	1.6	—	kΩ
S_{11}	Input Return Loss (5 MHz to 1.5 GHz)	1, 2, 3	20	30	—	dB
	Input Return Loss (1.5 GHz to 3 GHz) (M21424)	1, 2, 3	—	13	—	dB

NOTES:

1. Specified at recommended operation conditions—See Table 1-2.
2. Using the recommended input termination shown in Figure 2-1.
3. Measured single ended.
4. Guaranteed by design.
5. This is also the recommended cable launch level (far end).

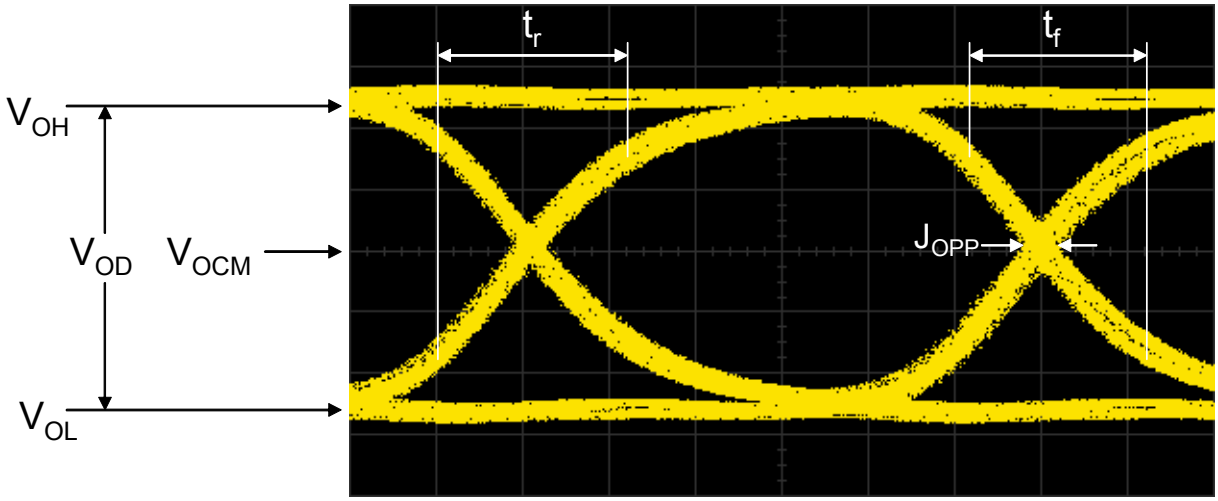
Table 1-6. High Speed Output Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
t_R/t_F	Rise/Fall Time (20%–80%), M21404	1, 2, 7	—	500	675	ps
	Rise/Fall Time (20%–80%), M21414, M21424	1, 2, 7	—	100	120	ps
t_R/t_F	Rise/Fall Time Mismatch, M21404	1, 2, 7	—	0	70	ps
	Rise/Fall Time Mismatch, M21414, M21424	1, 2, 7	—	0	30	ps
DCD_{DATA}	Duty Cycle Distortion, M21404	1, 2, 5, 6	—	0	50	ps
	Duty Cycle Distortion, M21414, M21424	1, 2, 5, 6	—	0	15	ps
V_{OD}	Differential Output Voltage p-p HiSwEn = 0 (750 mV)	1, 3	600	750	950	mV
V_{OCM}	Common mode Voltage HiSwEn = 0 (750 mV)	1, 3, 4	—	AV_{DD} – 0.205	—	V
V_{OD}	Differential Output Voltage p-p HiSwEn = 1 (1050 mV)	1, 3	850	1050	1270	mV
V_{OCM}	Common mode Voltage HiSwEn = 1 (1050 mV)	1, 3, 4	—	AV_{DD} – 0.290	—	V
R_{OUT}	Internal Output Termination Resistance to AV_{DD}	1	40	50	60	Ω

NOTES:

1. Specified at recommended operation conditions—See Table 1-2.
2. With 100Ω differential termination.
3. With 50Ω to AV_{DD} termination.
4. Outputs DC-coupled.
5. Duty Cycle Distortion is defined as the difference in the intrinsic jitter at the 50% voltage level and the intrinsic jitter at the rising/falling edge crossing point. If the rising/falling edge crossing point is at the 50% voltage level, then DCD_{DATA} = 0.
6. Measured with a 1010 pattern.
7. Measured with a PRBS23 pattern.

Figure 1-1. Output Symbols Definition



V_{OH}: Average voltage high level
V_{OL}: Average voltage low level
V_{OD}: (VOH) – (VOL)
V_{OCM}: Common Mode Voltage
J_{OPP}: Output Jitter Peak-Peak
t_r: 20-80% Rise Time
t_f: 80-20% Fall Time

NOTE: Waveform above is differential.

1.3 EQ Specifications

Table 1-7. Cable Equalizer Distance Specifications

Symbol	Parameter	Conditions	Notes	Minimum	Typical	Maximum	Units
L_{SD}	Max Cable Length	Belden 1694A	1, 4	—	400	—	m
	Max Cable Length	Belden 8281	1, 4	—	300	—	m
L_{HD}	Max Cable Length	Belden 1694A	2, 6	—	200	—	m
	Max Cable Length	Belden1694A	2, 5	—	140	—	m
	Max Cable Length	Belden 8281	2, 5	—	120	—	m
L_{3G}	Max Cable Length	Belden 1694A	3, 7	—	100	—	m

NOTES:

Entire table specified at recommended operating conditions—See Table 1-2.

1. Data Rate = 270 Mbps.
2. Data Rate = 1485 Mbps.
3. Data Rate = 2970 Mbps.
4. Error Free with timing Jitter typically = 0.2 UI, pathological pattern.
5. Error Free with alignment Jitter typically = 0.25 UI, pathological pattern.
6. Error Free with alignment jitter typically = 0.3 UI, pathological pattern.
7. Error Free with alignment Jitter typically = 0.35 UI, pathological pattern.

Table 1-8. $\overline{SD}$/MUTE Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
$V_{OUT, CMOS}$	Output voltage when input signal detected	1	—	0.16 x AV_{DD}	—	V
$V_{OUT, CMOS}$	Output voltage when input signal not detected	1	—	0.95 x AV_{DD}	—	V

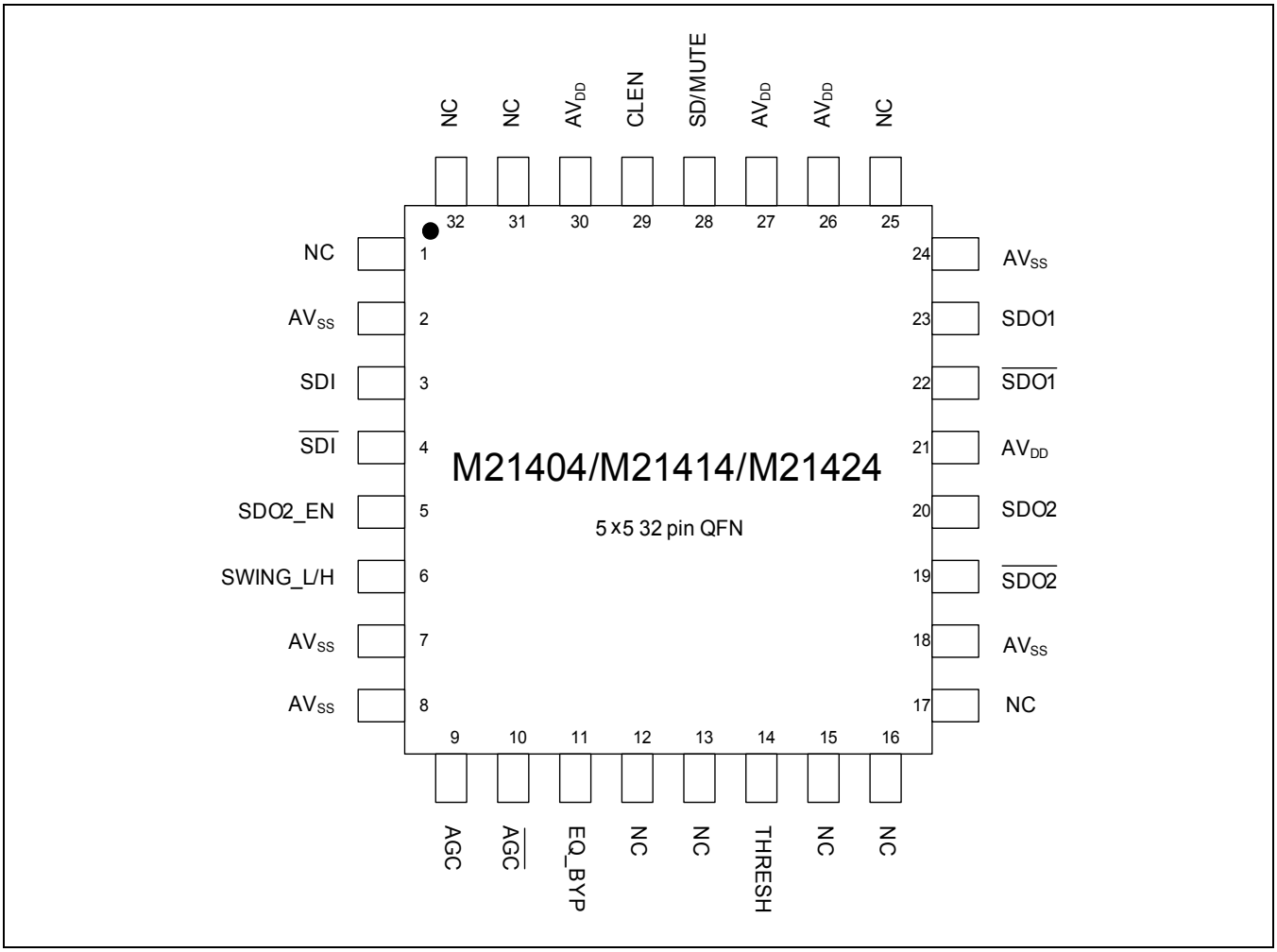
NOTE:

1. Specified at recommended operating condition—See Table 1-2.

1.4 Package Specification

The pin assignment is illustrated in Figure 1-2. The M21404/M21414/M21424 package is RoHS compliant. This package is backwards compatible with the standard soldering techniques as defined in JEDEC-STD-020C (SnPb Process).

Figure 1-2. M21404/M21414/M21424 Pin Assignments

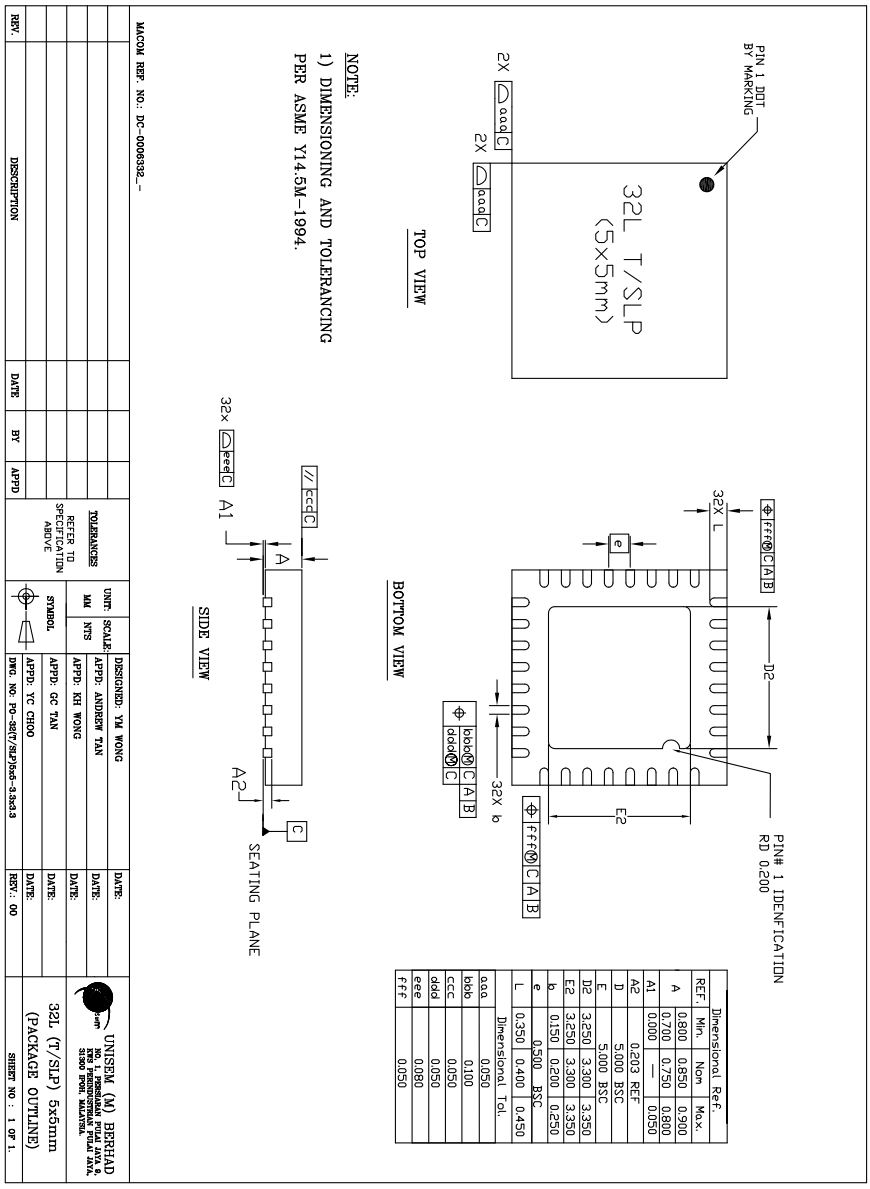


1.4.1 Mechanical Description

1.4.1.1 Package Details

The package for the M21404/M21414/M21424 is illustrated in Figure 1-3 below.

Figure 1-3. M21404/M21414/M21424 Packaging Details



Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.800	0.850	0.900
A1	0.000	0.700	0.750	0.800
A2		—	0.050
D	5.000 BSC		
E	5.000 BSC		
D2	3.250	3.300	3.350
E2	3.250	3.300	3.350
b	0.150	0.200	0.250
e	0.500 BSC		
L	0.350	0.400	0.450

Dimensional Tol.	
aaa	0.050
bbb	0.100
ccc	0.050
ddd	0.050
eee	0.080
fff	0.050

1. For dimension reference A, Min. is 0.800, Nom is 0.85 and Max. is 0.900.
2. New Unisem package and the old Amkor package have the same footprint.

1.5 Manufactureability

The values shown in this section may change; however, these are standard requirements.

1.5.1 Electrostatic Discharge

Tested per JESD22-A114. This device passes 2000V of ESD Human Body Model (HBM) testing.
Tested per JESD22-C101. This device passes 500V of ESD Charged Device Model (CDM) testing.
Tested per EIA/JESD78. This device passes 150 mA of trigger current at 85°C during Latchup testing.

1.5.2 Peak Reflow Temperature

M21404G, M21414G, and M21424G (RoHS compliant package): Peak reflow temperature is 260°C per JEDEC standards.

1.5.3 Moisture Sensitivity Level (MSL)

All versions of this device (Std Pb-type and RoHS compliant packages) are Moisture Sensitivity Level (MSL) 3 per J-STD-020B and J-STD-033.

1.6 Design Considerations

See Digital Video Interfacing Application Note (212xx-APP-001-A) for guidance on the following:

- Component Placement and Layout
- Routing Considerations

1.6.1 Thermal Considerations

The M21404/M21414/M21424 consume less power than legacy devices, therefore they will contribute less thermal energy and should result in a lower operating temperature.

2.0 Functional Description

2.1 Pin Descriptions

2.1.1 General Nomenclature

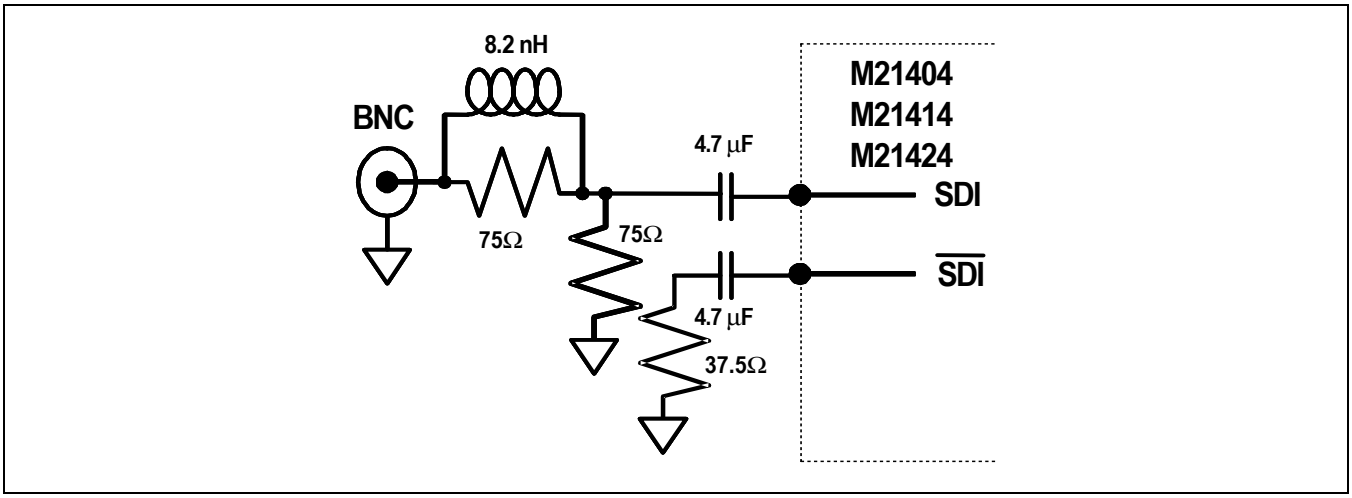
Throughout this data sheet, physical pins will be denoted in **BOLD** print. An array of pins can be called by each individual pin name (e.g. **MF0, MF1, MF2, MF3**, and **MF6**) or as an array (e.g. **MF[3...0, 6]** or **MF[3:0, 6]**).

2.1.2 High-Speed Input

Digital video coaxial cables are AC-coupled to the high-speed low-noise inputs, **SDI/$\overline{\text{SDI}}$**, which, are designed to operate in both the single-ended or differential mode. The typical application is single-ended into the non-inverting **SDI** input with the inverting **SDI** input biased to match the bias on the input used.

The M21404/M21414/M21424 do not contain any internal input terminations and require both external input termination as well as the matching circuit to exceed the SMPTE input return loss specifications. The package and IC design of the M21404/M21414/M21424 have been optimized for high-speed performance, allowing them to exceed the SD/HD SMPTE return loss spec by 5 dB to 10 dB, using the recommended external matching/termination network and commonly employed right-angle, through-hole, or vertical mount 75Ω BNC connectors. For non-inverting single-ended operation, the recommended input circuit is shown in Figure 2-1. For differential operation, the matching/termination circuit on **SDI** should be duplicated on **SDI**. The internal pull ups automatically bias **SDI/SDI** for proper AC coupled operation.

Figure 2-1. Single-ended Typical Input Matching/Termination Network



2.1.3 High-Speed Outputs

The high-speed CML differential outputs after equalization are made available on the **SDO1, $\overline{\text{SDO1}}$, SDO2, $\overline{\text{SDO2}}$** pins. By default only the **SDO1/SDO1** outputs are enabled, **SDO2/ SDO2** are enabled when **SDO2_EN** = High. Two swing levels are available; 750 mV and 1050 mV, when **SWING_L/H** = High, the 1050 mV output mode is selected, when **SDO2_EN** = High, this affects both **SDO1** and **SDO2**.

2.1.4 Adaptive Equalization Selection

In typical operation, the adaptive equalization is enabled with **EQ_BYP** = Low; however, with **EQ_BYP** = High, the adaptive equalization and DC restore circuit is bypassed and the input is fed directly to the output.

2.1.5 Cable Length Indicator

When the adaptive equalization is enabled (EQ_BYP = Low), an analog voltage inversely proportional to the cable length is made available on **CLEN**. The same transfer function applies to all bit rates. When the adaptive equalization is disabled (EQ_BYP = High), the **CLEN** voltage goes to its highest value (this indicates 0m cable length). During an LOS (Loss Of input Signal) event, the voltage falls to its lowest value.

2.1.6 Output Mute and Signal Detect

When configured as an input by forcing a voltage on **$\overline{\text{SD}}$/MUTE** = High (V_{DD}), the output of the M21404/M21414/ M21424 will be set to logic low (outputs muted). When **$\overline{\text{SD}}$/MUTE** = Low (V_{SS}), the output is never muted and the programmable cable length based mute function is disabled.

When tied to a high-impedance input or left floating, the programmable inhibit based on signal present is enabled and the pin is defined as an LOS output (logic). In the event of an LOS, the output is muted. The inhibit threshold is set with an analog voltage applied to the **THRESH** input pin, this threshold will depend on cable type (e.g. Belden 1694A or 8281).

2.1.7 Equalizer Detailed Description

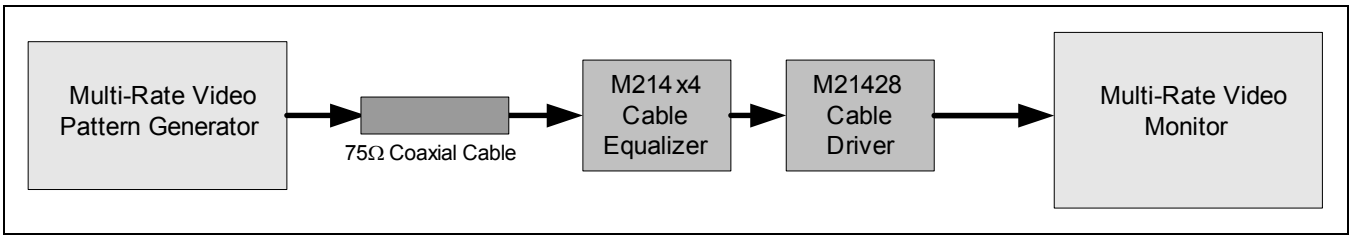
The basic equalizer design consists of interlaced stages of gain and equalization to maximize both the overall equalization gain as well as the input sensitivity for maximum performance with minimum jitter. In order to achieve maximum distance at 270 Mbps, 1485 Mbps and 2970 Mbps with Belden 1694A, the overall equalizer block has over 50 dB of broadband signal boost and maintains an input sensitivity of approximately 10 mV.

Since signals are launched with different SMPTE specified rise and fall times which can vary substantially (especially at the receive end after going though a wide dynamic range of valid cable lengths) the equalization routine determines both the bit rate and the resultant signal HF attenuation as opposed to just looking at the launch edge rates. By determining both sets of conditions, it is possible to optimize the equalizer for the different rates. For example, the M21424 maintains the same maximum cable length as optimized SD only equalizers. An SD signal through a short cable can have the same edge rate as a HD signal through a long cable; yet, both conditions require different levels of equalization as well as different optimized inverse-transfer functions. The advanced equalization technology can make the distinction between the two cases for optimal performance. This also leads to proper mute threshold (**THRESH**) and cable length indicator (**CLEN**) operation that is independent of the bit rate.

In order to accommodate both the SMPTE worst case equalizer pathological patterns as well as some customer derived worst case DC offset patterns, a high-gain slicer is included in the signal path to correct for any eye-

crossing wander due to AC coupling of the input. Figure 2-2 shows the test set used by MACOM to evaluate the performance of the M21404/M21414/M21424.

Figure 2-2. Test Setup Diagram for Cable Equalizer Evaluation



2.2 M21404/M21414/M21424 Common Signals by Interface Group

Table 2-1. Power Pins

Pin Name	Pin Number	Function	Type
AV_{SS}	2, 7, 8, 18, 24	Ground	Power
AV_{DD}	21, 26, 27, 30	Positive Supply	Power

Table 2-2. High-speed Signal Pins

Pin Name	Pin Number	Function	Type
SDI/$\overline{\text{SDI}}$	3, 4	Non-inverting and Inverting Serial Data Input to the adaptive equalizer	I—AC coupled high speed
$\overline{\text{SDO1}}$/SDO1	22, 23	Non-inverting and Inverting Differential Serial Data Output	O—High speed CML
$\overline{\text{SDO2}}$/SDO2	19, 20	Non-inverting and Inverting Differential Serial Data Output	O—High speed CML

2.2.1 M21404/M21414/M21424 Pins

Table 2-3. Control/Interface Pins

Pin Name	Pin Number	Function	Default	Type
NC	1	Do not connect to the pin.	N/A	N/A
SDO2_EN	5	Enable Input for **SDO2** Outputs: Low = SDO2 output disabled High = SDO2 output enabled	Internal pull down	I—CMOS
SWING_L/H	6	Enable Input for High Swing Output on SDO1/2: Low = 750 mV_{PP} diff. (default) High = 1050 mV_{PP} diff.	Internal pull down	I—CMOS
AGC/$\overline{\text{AGC}}$	9, 10	External AGC (Automatic Gain Control) capacitor connection points. Use 1.0 µF capacitor.	Internal pull up	Analog
EQ_BYP	11	Input control signal that when enabled (High) bypasses the inputs directly to the output stage. Low = Normal operation High = Disables EQ and bypasses input to output	Internal pull down	I—CMOS
NC	12, 13	Do not connect to the pin.	N/A	N/A
THRESH	14	Input control signal voltage. Programmable cable length forced mute threshold. This function is disabled if **$\overline{\text{SD}}$/MUTE** = Low	Internal pull down	Analog
NC	15, 16, 17, 25	Do not connect to the pin.	N/A	N/A
$\overline{\text{SD}}$/MUTE	28	Bidirectional Signal that can be used as an input control signal or as an output status indicator. When configured as an input by forcing a voltage on **$\overline{\text{SD}}$/MUTE** = High, the SDO outputs will be inhibited at logic low (outputs muted). See Table 1-4 for levels. When **$\overline{\text{SD}}$/MUTE** = Low (V_{SS}), the output is never muted and the programmable cable length based mute function is disabled. When configured as an output (tied to a high-impedance input) or left floating, the programmable inhibit based on cable length is enabled Configured as Output: Low = Input signal detect High = Loss of signal Configured as Input: Low = Never mute High = Force Mute	—	I/O
CLEN	29	Cable length Indicator output	—	Analog
NC	31, 32	Do not connect to the pin.	N/A	N/A

NOTE:

Internal pull-up/pull-down is 100 kΩ.

Appendix

A.1 Glossary of Terms/Acronyms

BER	Bit Error Rate
CD	Cable Driver
CDA	Cable Distribution Amplifier
CML	Current Mode Logic
DDI	Differential Data Inputs
DTV	Digital Television
DVB	Digital Video Broadcast
EMI	Electro Magnetic Interference
EQ	Equalizer or Equalization
ESD	Electro Static Discharge
GREEN	Environmentally friendly
HD	High Definition
HW	Hardware
ID	Identifier
I/O	Input/Output
MLF	Micro Lead Frame package (also called QFN)
RoHS	Restriction of Hazardous Substances
SD	Standard Definition
SDI	Serial Digital Input
SDO	Serial Digital Output
SE	Single Ended
SMPTE	Society of Motion Picture and Television Engineers
SW	Software

A.2 Reference Documents

A.2.1 External

The following external documents were referenced in this data sheet.

- SMPTE 292, SMPTE 259M, SMPTE 344M, SMPTE424M
- ESI t_R101 891 DVB Asynchronous Serial Interface (ASI)