M08035/M08045

SD, HD, 3G Multi-rate Reclocker

The M08035/M08045 are serial digital video reclockers with integrated trace equalization and automatic rate detect (ARD) circuitry. The M08035 operates at data rates of 270 Mbps and 1485 Mbps, while the M08045 operates at data rates of 270 Mbps, 1485 Mbps, and 2970 Mbps.

The M08035/M08045 have an input jitter tolerance (IJT) of greater than 0.6 unit intervals (UI) and can provide retimed serial outputs with very low output jitter. The reclocker requires a single, external, 27 MHz crystal, which is used as the reference clock. It includes per lane input equalization for up to 40" of FR4 trace and two connectors in addition to output de-emphasis.

These devices feature integrated supply regulators, allowing them to be powered from 1.2 V, 1.8 V, 2.5 V, or 3.3 V supply voltages. When operating at 1.2 V, they consume only 230 mW at 3G and HD. Furthermore, the power rails for the core, input, and output circuitry are electrically independent and as such may be connected to different voltage rails on the board. This feature enables the M08035/M08045 to be DC coupled to any upstream or downstream device regardless of its input/output voltage level.

These devices may be configured by setting the internal registers though standard two-wire and four-wire interfaces. Limited configuration is also possible through hardware pin settings.

The M08035/M08045 are offered in green and RoHS compliant, 6 mm x 6 mm, 40-pin QFN packages.

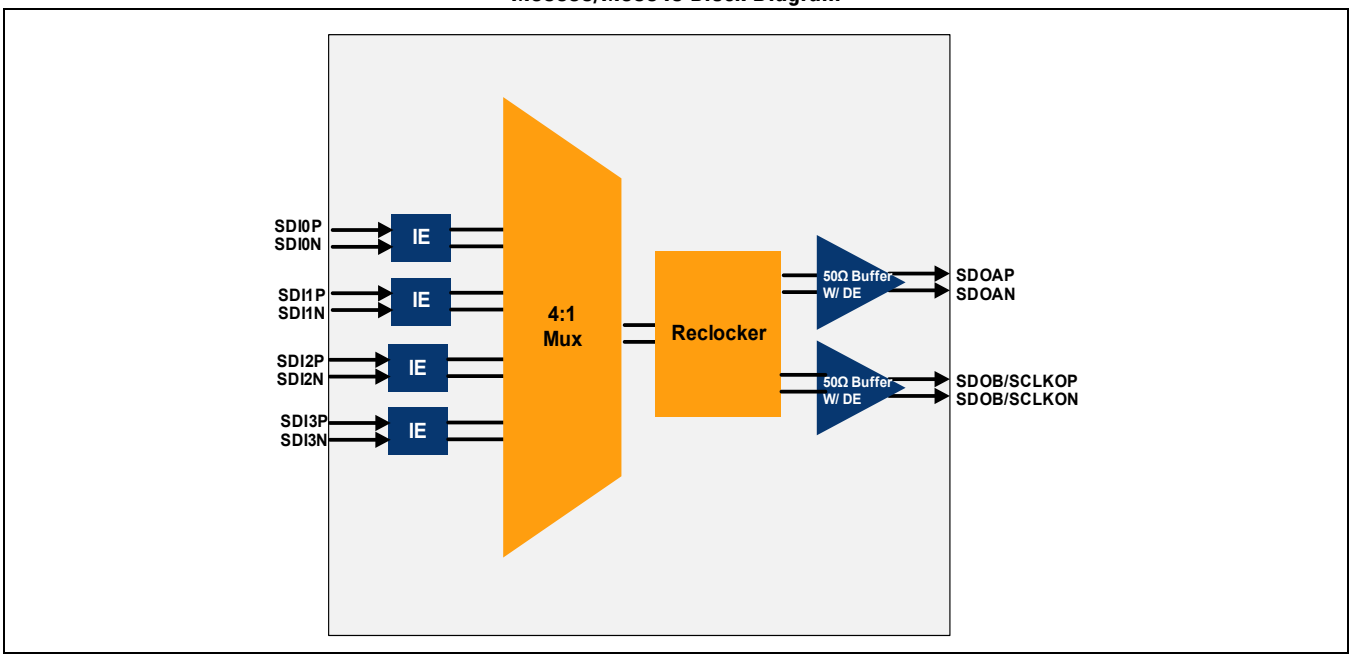
Applications

- Surveillance/CCTV Cameras
- Industrial and Professional Cameras
- Digital Video Recorders (DVR)
- Video Mixers and Switchers
- Digital Image Transmitter Devices
- Distribution Amplifiers
- Repeaters

Features

- Greater than 0.6 UI Input Jitter Tolerance
- Integrated 50 Ω input termination
- Input equalization and output de-emphasis for 40" of FR4 trace
- 230 mW power consumption (1.2 V operation)
- Integrated regulators for multi-voltage operation (1.2 V - 3.3 V)
- Electrically independent input, output, and core supply rails
- Output enable/disable and configurable auto or manual bypass mode
- Automatic and manual modes for rate indication and selection
- Loss of Lock (LOL), Loss of Signal (LOS) and data rate Indication
- Two-wire and four-wire serial interface programmability
- Industrial operating temperature range (-40 °C to +85 °C)
- Optional recovered serial clock output

M08035/M08045 Block Diagram



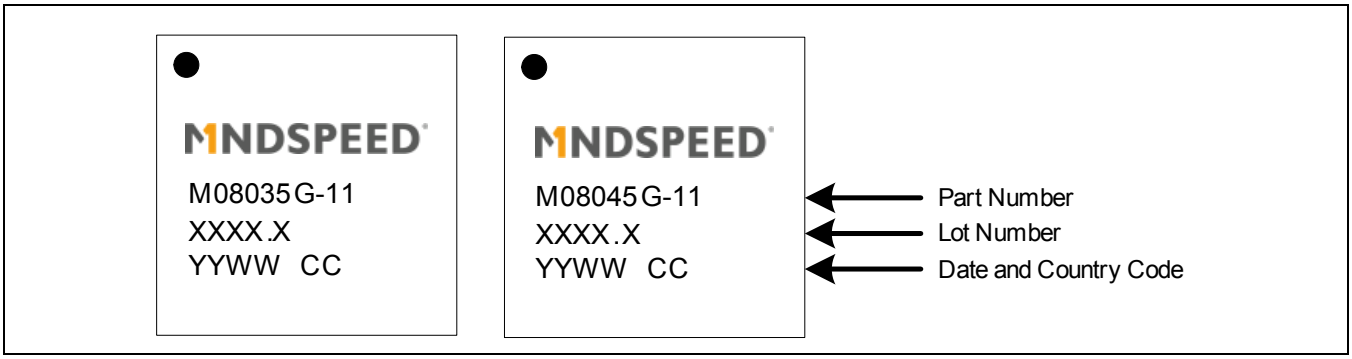
Ordering Information

Part Number	Package	Operating Temperature
M08035G-11*	6x6 mm, 40-pin QFN package	-40 °C to 85 °C
M08045G-11*	6x6 mm, 40-pin QFN package	-40 °C to 85 °C

Revision History

Revision	Level	Date	Description
V2	Release	October 2014	Updated MODE_SEL, SDOB/SCLK_EN, xREG_EN description in Table 3-1.
A (V1)	Release	May 2011	Initial release.

M08035/M08045 Marking Diagram



1.0 Electrical Characteristics

Unless noted otherwise, specifications apply for typical recommended operating conditions shown in Table 1-2, with DV_{DDO} = 1.2 V, AV_{DDCORE} = 1.2 V, DV_{DDCORE} = 1.2 V, AV_{DDI} = 1.2 V, PCML inputs/outputs at 800 mV_{PPD} (R_{LOAD} = 50 Ω), and PRBS 2^{10} – 1 test pattern at 2.97 Gbps.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Note	Minimum	Maximum	Unit
AV_{DDI}	Analog supply for input circuitry	1, 3	-0.5	3.6	V
AV_{DDO}	Analog supply for output circuitry	1, 3	-0.5	3.6	V
DV_{DDIO}	Digital supply for input/output circuitry	1, 3	-0.5	3.6	V
DV_{DDCORE}	Digital core positive supply	1, 3	-0.5	1.5	V
AV_{DDCORE}	Analog core positive supply	1, 3	-0.5	1.5	V
T_{STORE}	Storage Temperature	1, 3	-65	150	°C
$V_{MAX, IO}$	Maximum/minimum input/output voltage on any input/output pin	1, 3	-0.5	AV_{DDI}+0.5	V
$V_{ESD, HBM}$	Human Body Model (HBM)	1, 2, 3	-2	2	kV
$V_{ESD, CDM}$	Charge Device Model (CDM)	1, 2, 3	-500	500	V
LU	Latch Up @ 85 °C	1, 3	-150	150	mA

NOTES:

1. Exposure of the device beyond the minimum/maximum limits may cause permanent damage. Limits listed in the above table are stress limits only, and do not imply functional operation within these limits.
2. HBM and CDM per JEDEC Class 2 (JESD22-A114-B).
3. Limits listed in the above table are stress limits only and do not imply functional operation within these limits.

Table 1-2. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
DV_{DDIO}	Digital I/O positive supply	1.14	1.2, 1.8, 2.5, or 3.3	3.47	V
AV_{DDI}	Analog input positive supply	1.14	1.2, 1.8, 2.5, or 3.3	3.47	V
AV_{DDO}	Analog output positive supply	1.14	1.2, 1.8, 2.5, or 3.3	3.47	V
AV_{DDCORE}	Analog core positive supply	1.14	1.2	1.26	V
DV_{DDCORE}	Digital core positive supply	1.14	1.2	1.26	V
T_{CASE}	Case Temperature	-40	25	+85	°C

Table 1-3. Power Consumption Specifications

Symbol	Parameter	Conditions	Note	Typical	Maximum	Unit
P_{TOTAL}	Total power consumption	AV_{DDI} = AV_{DDO}=DV_{DDIO}=DV_{DDCORE} = AV_{DDCORE}= 1.2 V SDO Swing Level 1	1, 3	230	290	mW
			1, 4	250	350	
P_{TOTAL}	Total power consumption	AV_{DDI} = AV_{DDO}=DV_{DDIO}=DV_{DDCORE} = AV_{DDCORE}= 1.2 V SDO Swing Level 2	1, 3	240	300	mW
			1, 4	260	360	
P_{TOTAL}	Total power consumption	DV_{DDCORE} = AV_{DDCORE}= 1.2 V AV_{DDI} = DV_{DDIO} = 1.2 V AV_{DDO} = 1.8 V SDO Swing Level 3	1, 3	260	370	mW
			1, 4	270	450	
		DV_{DDCORE} = AV_{DDCORE}= 1.2 V AV_{DDI} = DV_{DDIO} = 3.3 V AV_{DDO} = 3.3 V SDO Swing Level 3	2, 3	720	1070	
θ_{JA}	Junction to ambient thermal resistance		5	35	—	°C/W
θ_{JC}	Junction to case thermal resistance		5	3	—	°C/W

NOTE:

1. Internal regulators disabled.
2. Internal regulators enabled.
3. SDOB/SCLK disabled.
4. SDOB/SCLK enabled.
5. Airflow = 0 m/s.

Table 1-4. High Speed Input Electrical Specifications

Symbol	Parameter	Conditions	Note	Minimum	Typical	Maximum	Unit
DR	Input data rate (M08035)	SD Operation		—	270	—	Mbps
		HD Operation		—	1485, 1483.5	—	Mbps
		Reclocker bypassed		18	—	3400	Mbps
DR	Input data rate (M08045)	SD Operation		—	270	—	Mbps
		HD Operation		—	1485, 1483.5	—	Mbps
		3G Operation		—	2970, 2967	—	Mbps
		Reclocker bypassed		18	—	3400	Mbps
V_{IN}	Differential input voltage	At the chip input (point blank) Input equalization disabled LOS enabled (default setting)	1, 3	300	800	1600	mV_{PPD}
V_{ICM}	Input common mode voltage	At the chip input (point blank) Input equalization disabled LOS enabled		AV_{DDI}-0.6	—	AV_{DDI}+0.1	V
R_{IN}	Input Termination to AV_{DDI}			40	50	60	Ω
IE	Input Equalization		2	—	0, 2, 4, 6	—	dB
I_{IN}	Maximum high-speed input current		4	-100		100	mA

NOTE:

1. For example, 1200 mV_{PPD} = 600 mV_{PP} for each single-ended terminal.
2. These values correspond to: off, small, medium, and large respectively. The small setting is not available in hardware mode.
3. When using long traces and input equalization enabled, MACOM recommends a minimum input swing of 400 mV_{PPD}. With video stress patterns, DC coupling produces the best results.
4. Exposure of the device beyond the minimum/maximum limits may cause permanent damage. Limits listed in the above table are stress limits only, and do not imply functional operation within these limits.

Table 1-5. High Speed Output Electrical Specifications

Symbol	Parameter	Conditions	Note	Minimum	Typical	Maximum	Unit
DR	Output data rate (M08035)	SD Operation		—	270	—	Mbps
		HD Operation		—	1485, 1483.5	—	
		Reclocker bypassed		18	—	3400	
DR	Output data rate (M08045)	SD Operation		—	270	—	Mbps
		HD Operation		—	1485, 1483.5	—	
		3G Operation		—	2970, 2967	—	
		Reclocker bypassed		18	—	3400	
F_{CLOCK}	Serial clock output frequency (M08035)	SD Operation	1, 7	—	270	—	MHz
		HD Operation		—	1485, 1483.5	—	
F_{CLOCK}	Serial clock output frequency (M08045)	SD Operation	1, 7	—	270	—	MHz
		HD Operation		—	1485, 1483.5	—	
		3G Operation		—	2970, 2967	—	
V_{OUT}	Differential Output Swing (peak to peak, differential)	Swing Level 1	2	470	600	720	mV_{PPD}
		Swing Level 2	2	600	800	970	
		Swing Level 3	2,3	960	1200	1500	
V_{OCM}	Output common mode voltage	DC coupled	2, 6	—	AV_{DDO}-V_{OUT}/4	—	
t_R/t_F	SDO output Rise/Fall Time	From 20%-80% of the swing for all levels		—	85	130	ps
$t_R/t_F \Delta$	Rise/Fall Time Mismatch	From 20%-80% of the swing for all levels	6	—	—	30	ps
DCD_{DATA}	Output duty cycle distortion	For all data rates	4	—	—	15	ps
R_{OUT}	Output Termination to AV_{DDO}			40	50	60	Ω
DE	Output De-Emphasis		5	—	0, 2, 4, 6	—	dB

NOTE:

1. Serial clock output enabled.
2. Differential swing is maximum output level (De-emphasis is disabled or max level when de-emphasis is enabled), max level includes overshoot.
3. 1200 mV_{PPD} requires AV_{DDO} to be 1.8 V or higher.
4. Measured in reclocked mode.
5. These values correspond to: off, small, medium, and large respectively. The small setting is not available in hardware mode.
6. Guaranteed by design.
7. See Section 4.7 for information on clock data alignment.

Table 1-6. Digital Input/Output Electrical Characteristics

Symbol	Parameter	Note	Minimum	Maximum	Unit
V_{OH}	Output Logic High	1	0.80 x DV_{DDIO}	—	V
V_{OL}	Output Logic Low	2	—	0.2 x DV_{DDIO}	V
V_{IH}	Input Logic High	—	0.85 x DV_{DDIO}	DV_{DDIO} + 0.5	V
V_{IF}	Input Logic Floating	—	0.25 x DV_{DDIO}	0.75 x DV_{DDIO}	V
V_{IL}	Input Logic Low	—	0	0.15 x DV_{DDIO}	V

NOTE:

1. I_{OH} = -3 mA
2. I_{OL} = 3 mA

Table 1-7. Reclocker Specifications (M08035)

Symbol	Parameter	Conditions	Note	Minimum	Typical	Maximum	Unit
t_{LOCK}	Lock time (asynchronous)	Automatic rate detection enabled	1	—	—	6	ms
$F_{LBW, PEAK}$	Loop bandwidth peaking		1	—	0.1	—	dB
F_{LBW}	Loop bandwidth (nominal setting)	HD operation (1.485 Gbps)	1	—	0.85	—	MHz
		SD operation (270 Mbps)	1	—	0.17	—	
J_{TOL}	Input jitter tolerance	HD, and SD operation	2	> 0.6	—	—	UI p-p
J_{GEN}	Total Output jitter	HD operation (1.485 Gbps)	2, 3	—	0.04	0.06	UI p-p
		SD operation (270 Mbps)	2, 3	—	0.02	0.05	

NOTE:

1. 0.2 UI input jitter applied at SDI input.
2. Measured with $PRBS2^{10}$-1.
3. Input jitter = 20 ps p-p.

Table 1-8. Reclocker Specifications (M08045)

Symbol	Parameter	Conditions	Note	Minimum	Typical	Maximum	Unit
t_{LOCK}	Lock time (asynchronous)	Automatic rate detection enabled	1	—	—	6	ms
$F_{LBW, PEAK}$	Loop bandwidth peaking		1	—	0.1	—	dB
F_{LBW}	Loop bandwidth (nominal setting)	3G operation (2.97 Gbps)	1	—	1.7	—	MHz
		HD operation (1.485 Gbps)	1	—	0.85	—	
		SD operation (270 Mbps)	1	—	0.17	—	
J_{TOL}	Input jitter tolerance	3G, HD, and SD operation	2	> 0.6	—	—	UI p-p
J_{GEN}	Total Output jitter	3G operation (2.97 Gbps)	2, 3	—	0.07	0.11	UI p-p
		HD operation (1.485 Gbps)	2, 3	—	0.04	0.06	
		SD operation (270 Mbps)	2, 3	—	0.02	0.05	

NOTE:

1. 0.2 UI input jitter applied at SDI input.
2. Measured with $PRBS2^{10}$-1.
3. Input jitter = 20 ps p-p.

Table 1-9. XTALP/N and Reference Clock Electrical Specifications

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
F_{REF}	XTAL/Ref clock frequency	3	—	27	—	MHz
$F_{REF, ppm}$	XTAL/Ref clock frequency accuracy	—	-100	0	100	ppm
C_{LOAD}	XTAL load capacitance	1	—	20	—	pF
$CLOCK_{JITT}$	Jitter (RMS)	2, 4	—	—	1	ps
$CLOCK_{DCT}$	Reference clock duty cycle tolerance	2	40	—	60	%
R_{IN}	Input impedance	2, 5	200	750	1500	Ω
V_{IN}	Input amplitude	2	0.8	—	1.2	V
t_R/t_F	Rise/Fall time	2, 6	—	2	6	ns

NOTE:

1. This capacitance is supplied internally (no external cap is required).
2. When using an external reference clock source, this should be AC coupled through a 0.1 µF capacitor.
3. When using an external clock a small increase in jitter may be seen. For best performance a crystal is recommended.
4. Jitter bandwidth is from 12 kHz to 20 MHz.
5. Measured with TDR module.
6. 10% to 90% rise and fall times.

2.0 Typical Performance Characteristics

Figure 2-1. M08035 Eye Diagram at Reclocker Input PRBS15 @ 1.485 Gbps

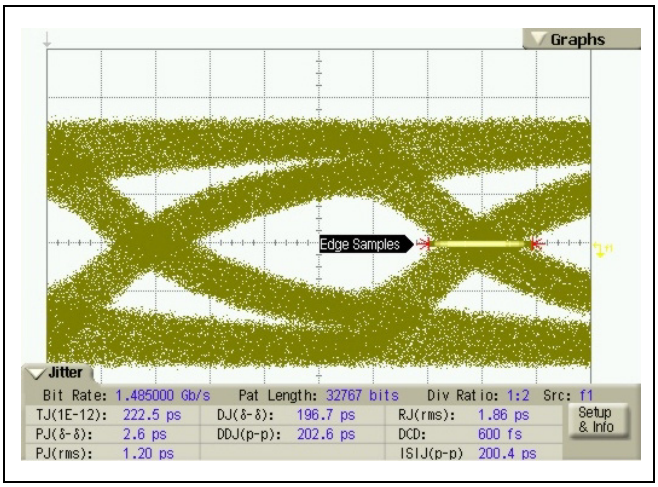


Figure 2-2. M08035 Eye Diagram at Reclocker Output PRBS15 @ 1.485 Gbps

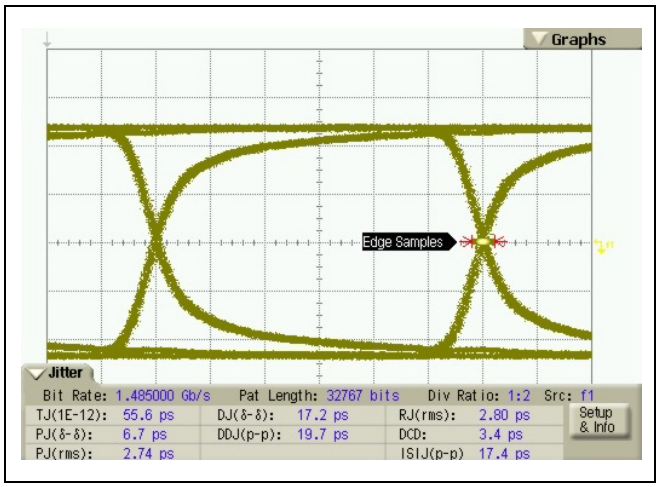


Figure 2-3. M08045 Eye Diagram at Reclocker Input PRBS15 @ 3 Gbps

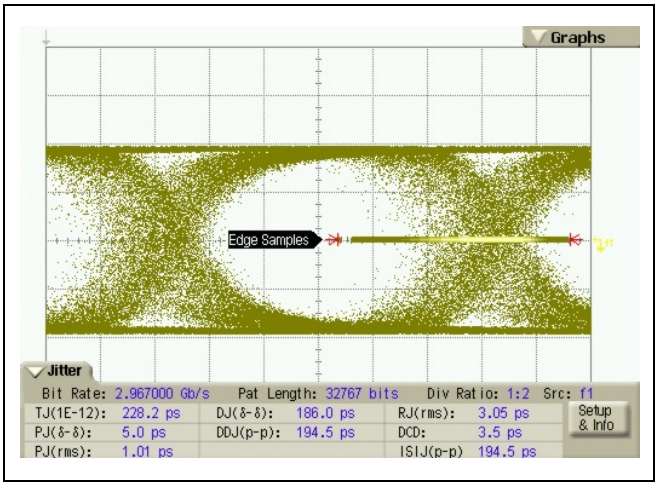
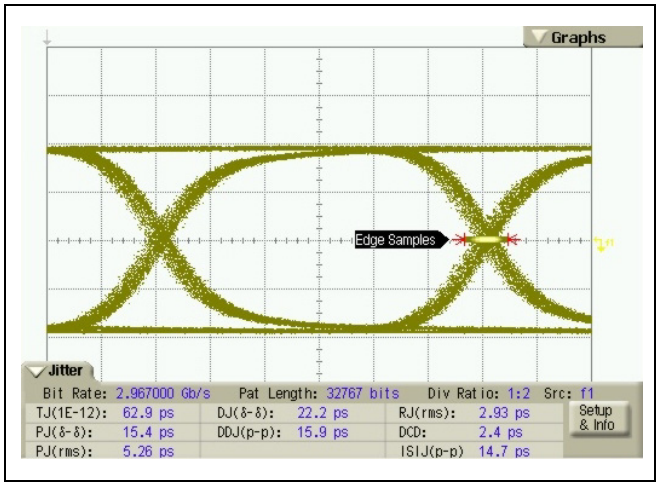


Figure 2-4. M08045 Eye Diagram at Reclocker Output PRBS15 @ 3 Gbps



3.0 Pinout Diagram, Pin Description, and Package Drawing

Figure 3-1. M08035/M08045 Pinout Diagram

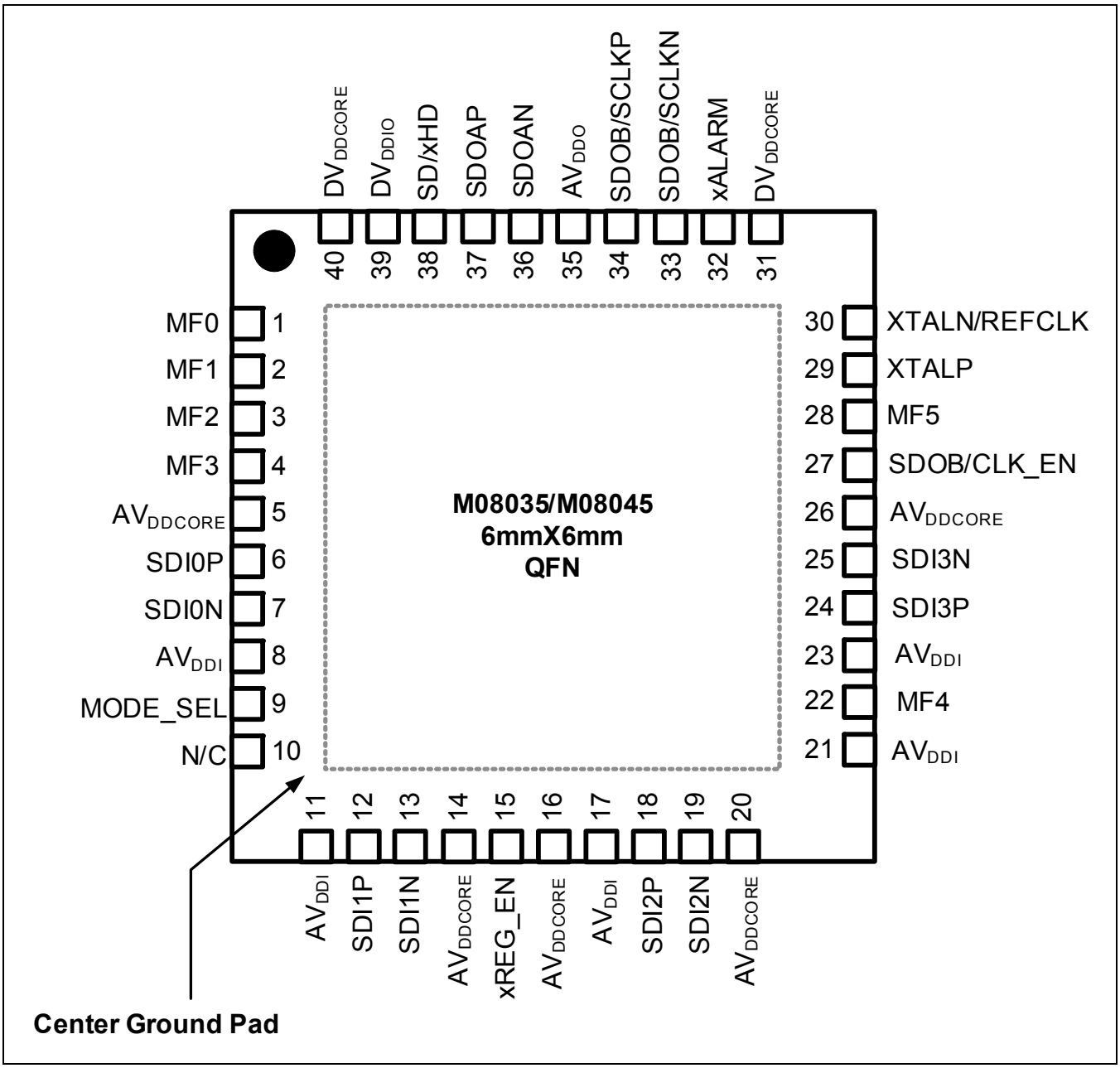


Table 3-1. M08035/M08045 Pin Description (1 of 2)

Pin Name	Pin Number(s)	Type	Description
AV_{DDCORE}	5, 14, 16, 20, 26	Power	Analog positive supply
AV_{DDI}	8, 11, 17, 21, 23	Power	Analog positive supply
AV_{DDO}	35	Power	Analog positive supply
DV_{DDCORE}	31, 40	Power	Digital Core Positive Supply
DV_{DDIO}	39	Power	Digital Core Positive Supply
AVSS	Center Ground Pad	Power	Ground
SDI0P, SDI0N	6, 7	PCML Input	Data Input Lane0; true/complement
SDI1P, SDI1N	12, 13	PCML Input	Data Input Lane1; true/complement
SDI2P, SDI2N	18, 19	PCML Input	Data Input Lane2; true/complement
SDI3P, SDI3N	24, 25	PCML Input	Data Input Lane3; true/complement
SDOAP, SDOAN	37, 36	PCML Output	Data Output Lane A; true/complement
SDOBP/SCLKP, SDOBN/SCLKN	34, 33	PCML Output	Data Output Lane B; true/complement
XTALP	29	Reference Clock	27 MHz reference XTAL connection
XTALN/REFCLK	30	Reference Clock	27 MHz reference XTAL connection or 27 MHz reference clock input
MODE_SEL	9	CMOS Input	Sets the device control/configuration mode: L = Device is in register access mode with two-wire serial control (SIC2) F = Device is in hardware control mode (Hardware Mode) H = Device is in register access mode with four-wire serial control (SIC4)
SDOB/SCLK_EN	27	CMOS Input	SDOB/SCLK output enable: L = SDOB/SCLK output disabled F = Serial data output enabled H = Serial clock output enabled
xREG_EN	15	CMOS Input	Regulator enable control, as in Figure 3-6, but pull up resistor is to AV_{DDI}. L = Integrated regulators enabled F = Integrated regulators disabled
SD/xHD	38	CMOS Output	CMOS SD/xHD rate indicator: L = HD/3G Data rate H = SD Rate
xALARM	32	Output (Open Drain)	Alarm indicator for all channels (Logical OR of all individual channel alarms). Termination - Open L = Alarm asserted H = Normal operation Serial Control Mode (two-wire/four-wire): xALARM in interrupt mode Hardware Mode: Not supported

Table 3-1. M08035/M08045 Pin Description (2 of 2)

Pin Name	Pin Number(s)	Type	Description
MF0	1	CMOS Input	Four-wire serial control Mode: Serial clock input (SCLK) Two-wire serial control Mode: Clock input from master host (SCL) Hardware Mode: Unused
MF1	2	CMOS Input	Four-wire serial control Mode: Serial data output (SO) Two-wire serial control Mode: Serial data I/O (SDA) Hardware Mode: Unused
MF2	3	CMOS Input	Four-wire serial control Mode: Serial data in (SI) Two-wire serial control Mode: Address bit 0 (ADD0) Hardware Mode: Input trace equalization control for all SDI inputs (IE_CTRL) H = Large Input EQ F = Medium Input EQ L = Input EQ disabled
MF3	4	CMOS Input	Four-wire serial control Mode: Active low chip select (xCS) Two-wire serial control Mode: Address bit 1 (ADD1) Hardware Mode: Output de-emphasis (DE) control for SDO outputs (DE_CTRL) H = Large Output DE F = Medium Output DE L = DE disabled
MF4	22	CMOS Input	Four-wire serial control Mode: Not used. Tie to DV_{DDIO} or leave floating Two-wire serial control Mode: Address bit 2 (ADD2) Hardware Mode: Reclocker bypass control (RC_BYPASS) L/F = Normal operation, Reclocker not bypassed H = Reclocker bypassed
MF5	28	CMOS Input	Four-wire serial control Mode: Not used. Tie to AVSS or leave floating Two-wire serial control Mode: Address bit 3 (ADD3) Hardware Mode: SDO disable control for all outputs (SDO_DIS) H = SDO disabled output logic high L/F = SDO enabled
NC	10	Reserved	Do not connect

Figure 3-2. I-Analog

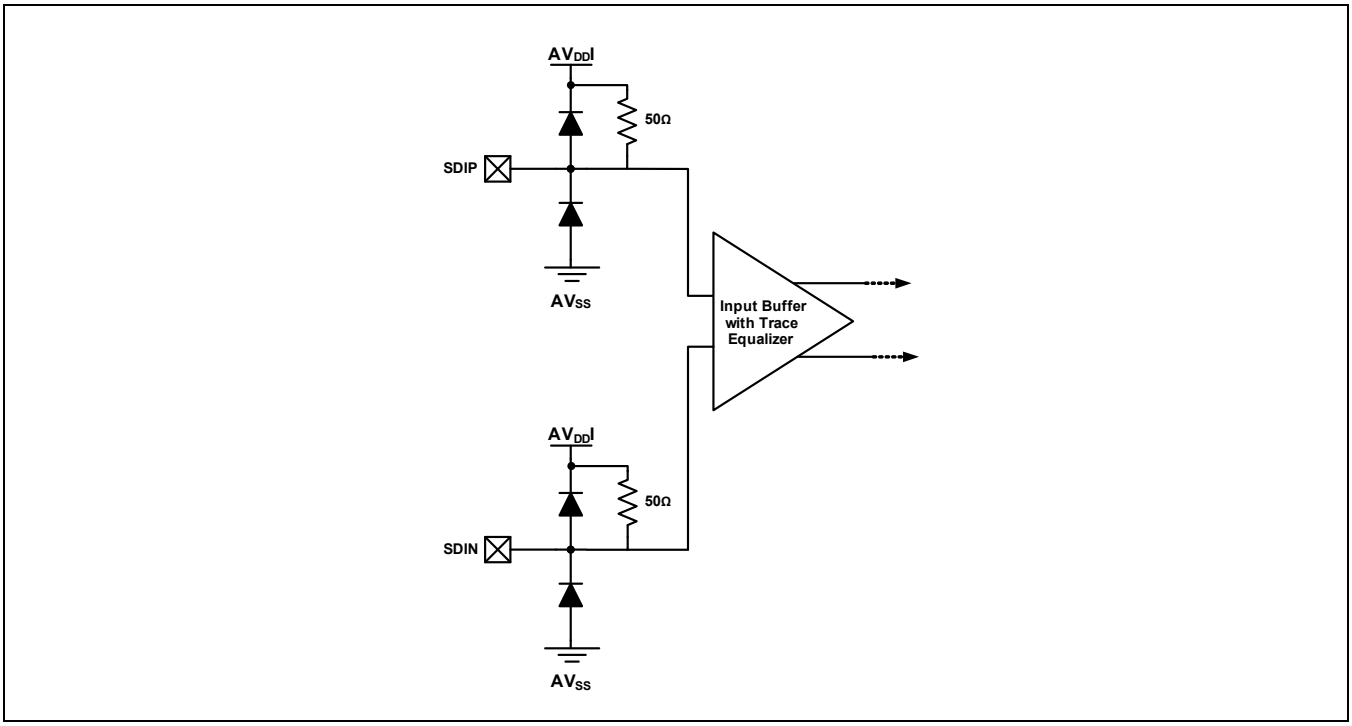


Figure 3-3. O-Analog

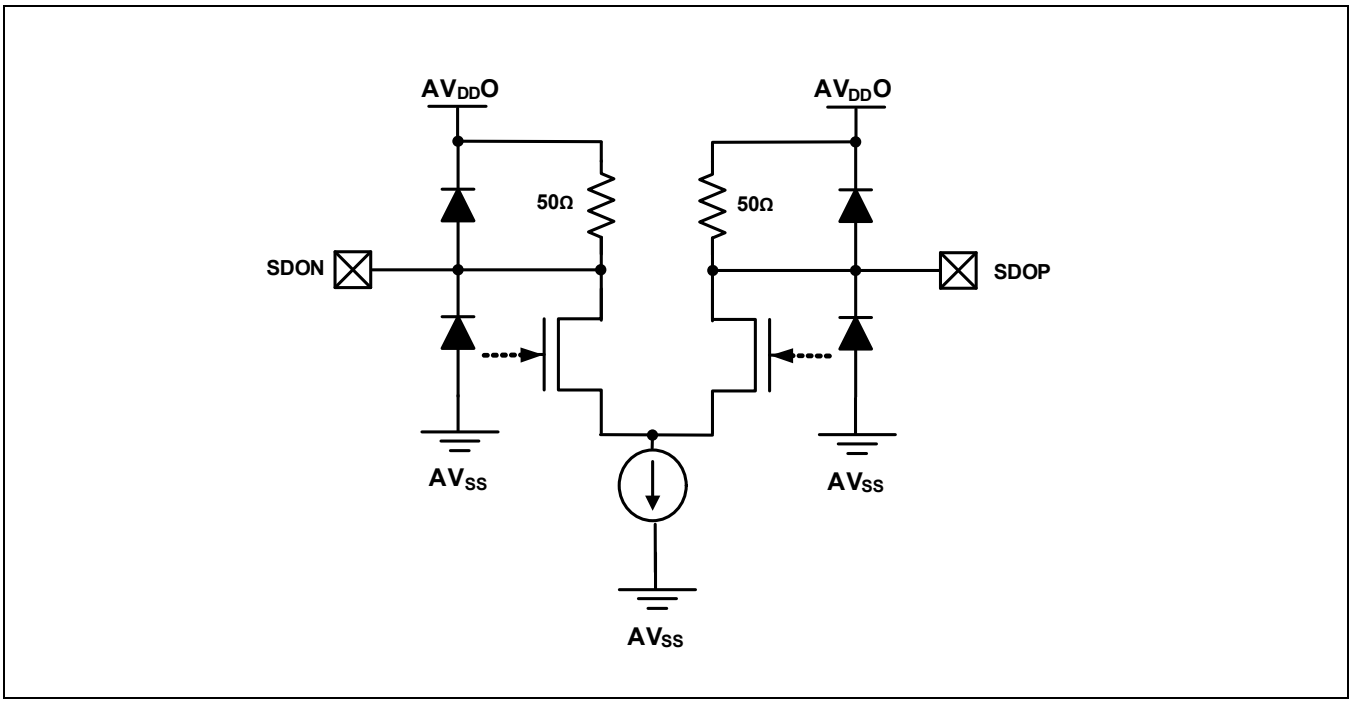


Figure 3-4. Ref Clock

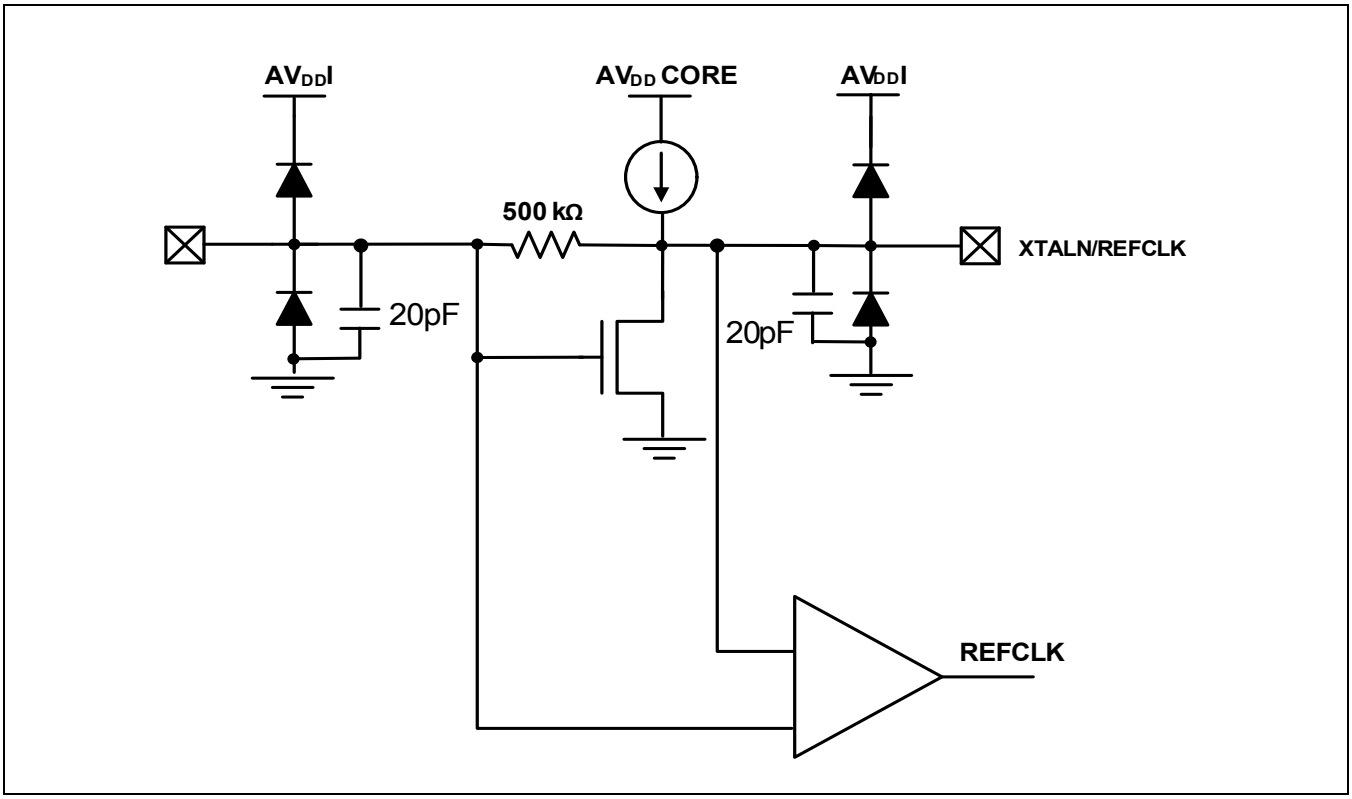


Figure 3-5. I-Digital With No Pull-up

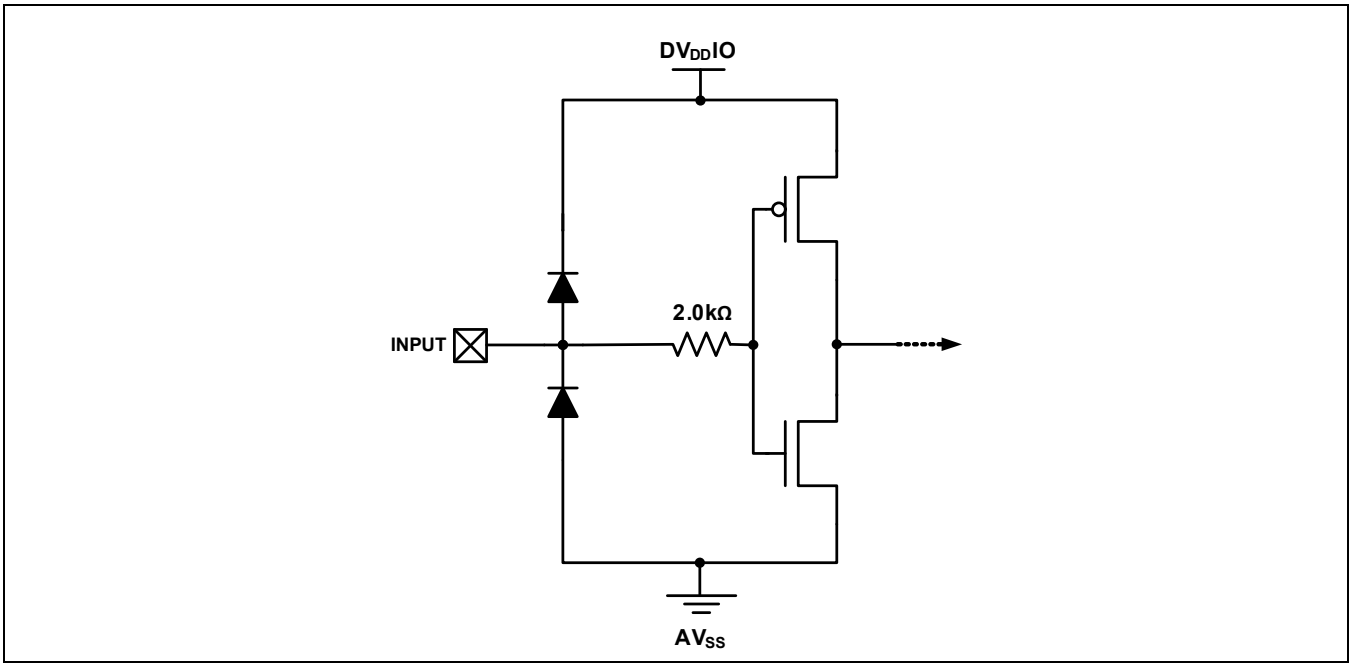


Figure 3-6. I-Digital With Pull-up

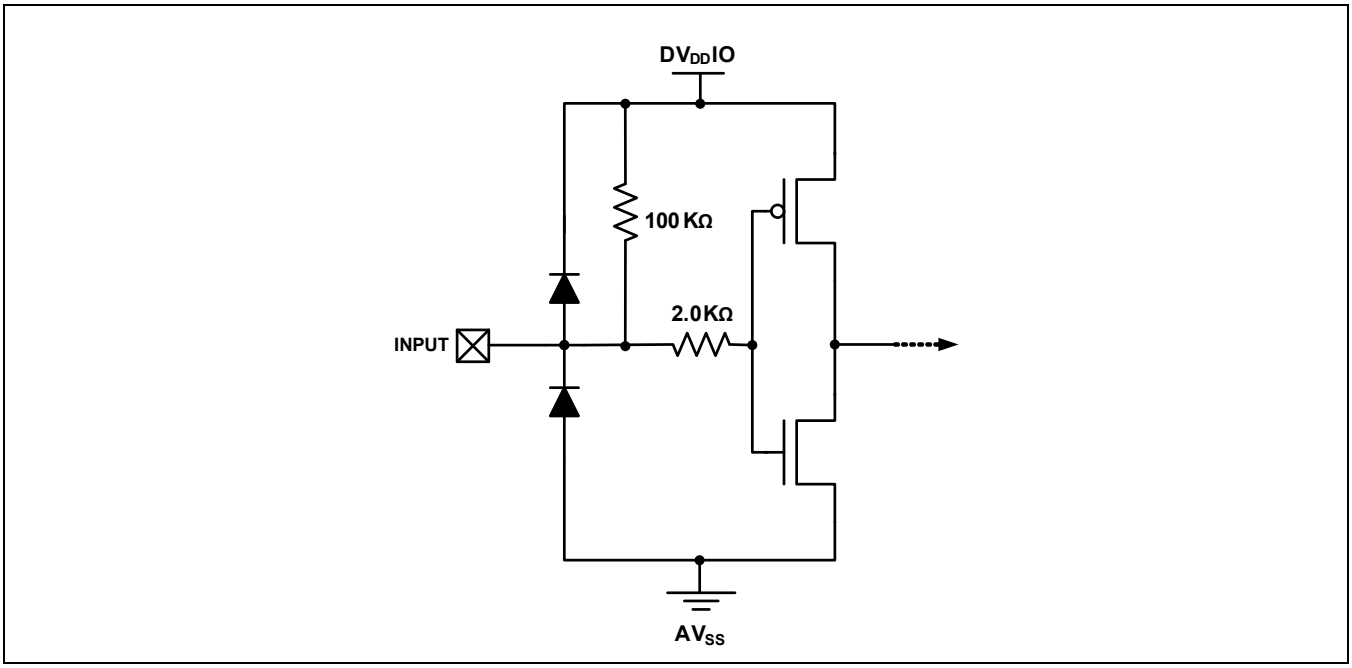


Figure 3-7. I-Digital With Pull-down

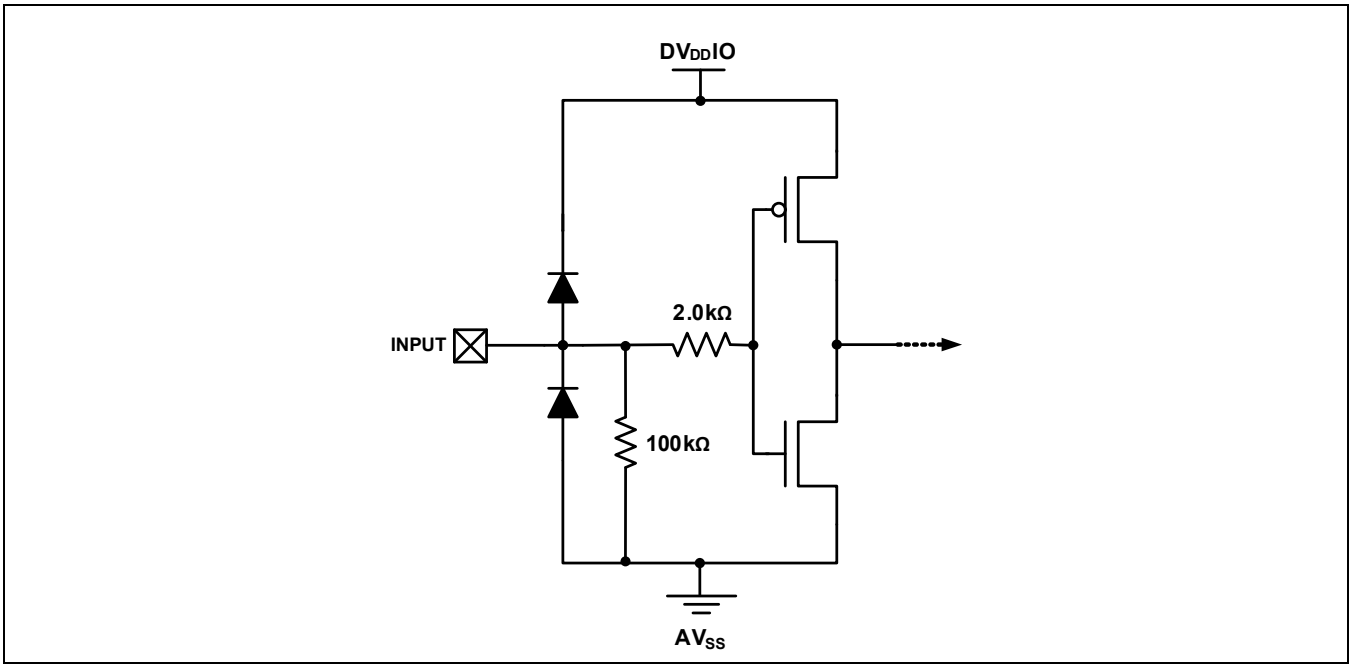


Figure 3-8. 3-State/I-Digital

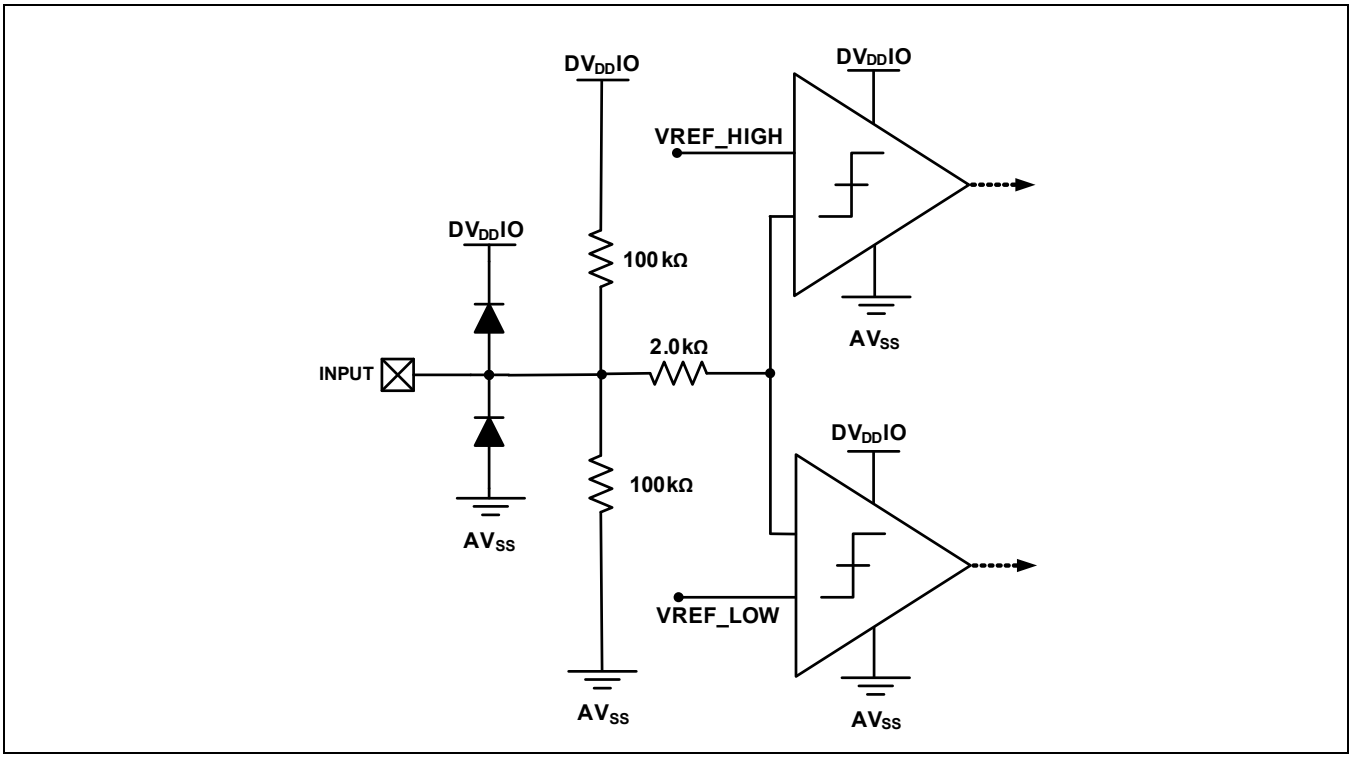


Figure 3-9. O-Digital

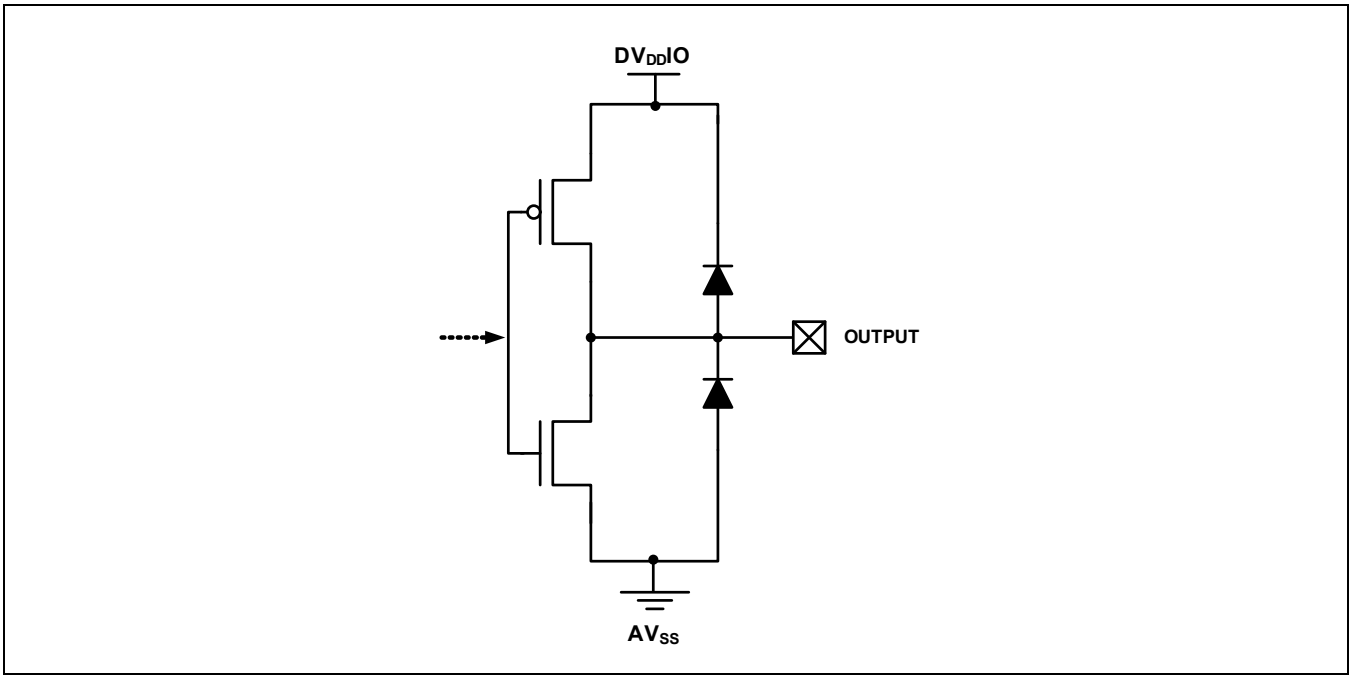
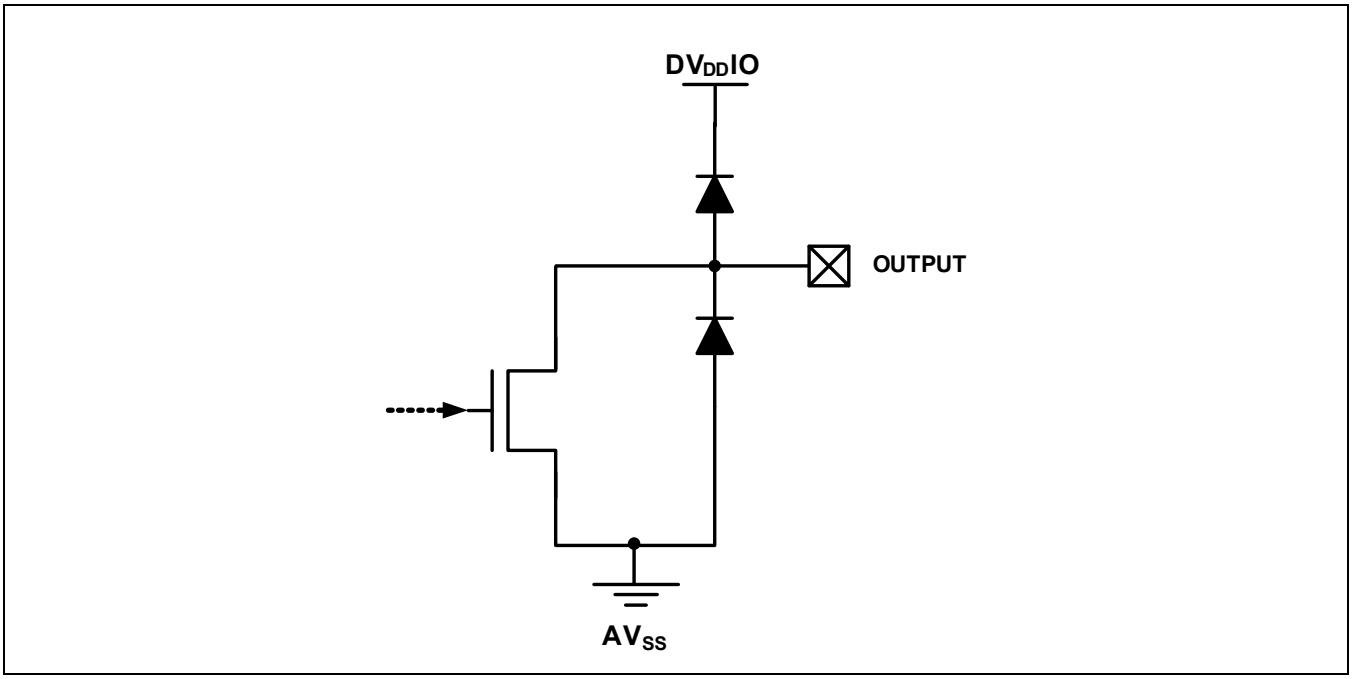


Figure 3-10. O-Open Drain



The M08035/M08045 are assembled in 40-pin, 6 mm x 6 mm Quad Flat No-Lead (QFN) packages. The exposed die paddle serves as the IC ground (AV_{SS}), and the primary means of thermal dissipation. This die paddle should be soldered to the PCB. A cross-section of the QFN package is shown below.

Figure 3-11. QFN Package Cross Section

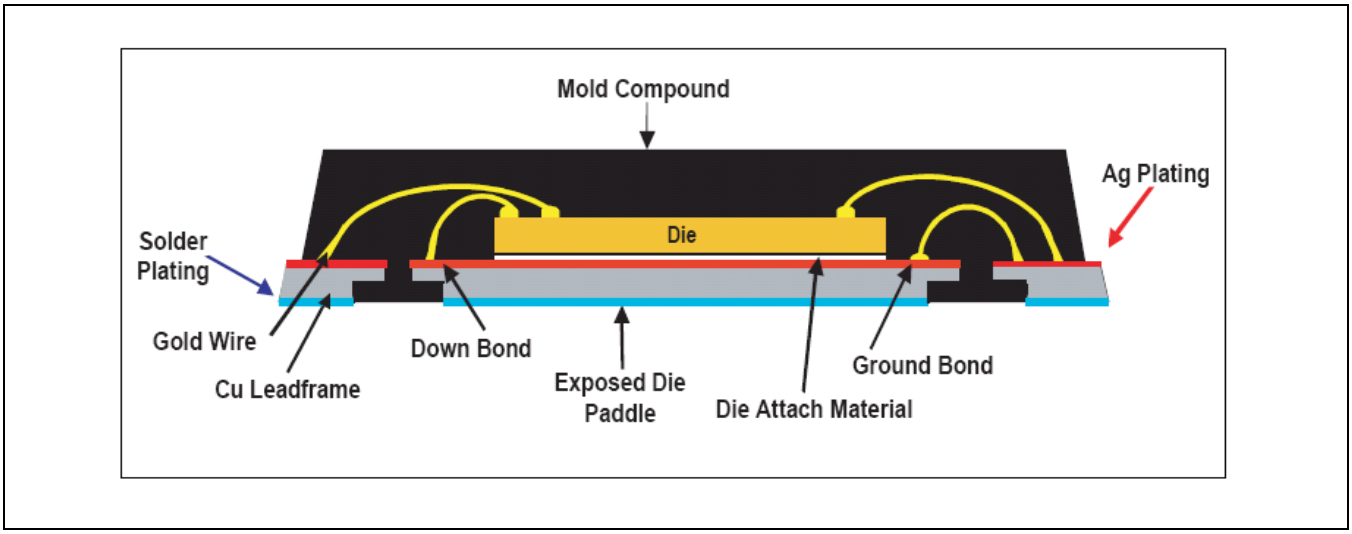
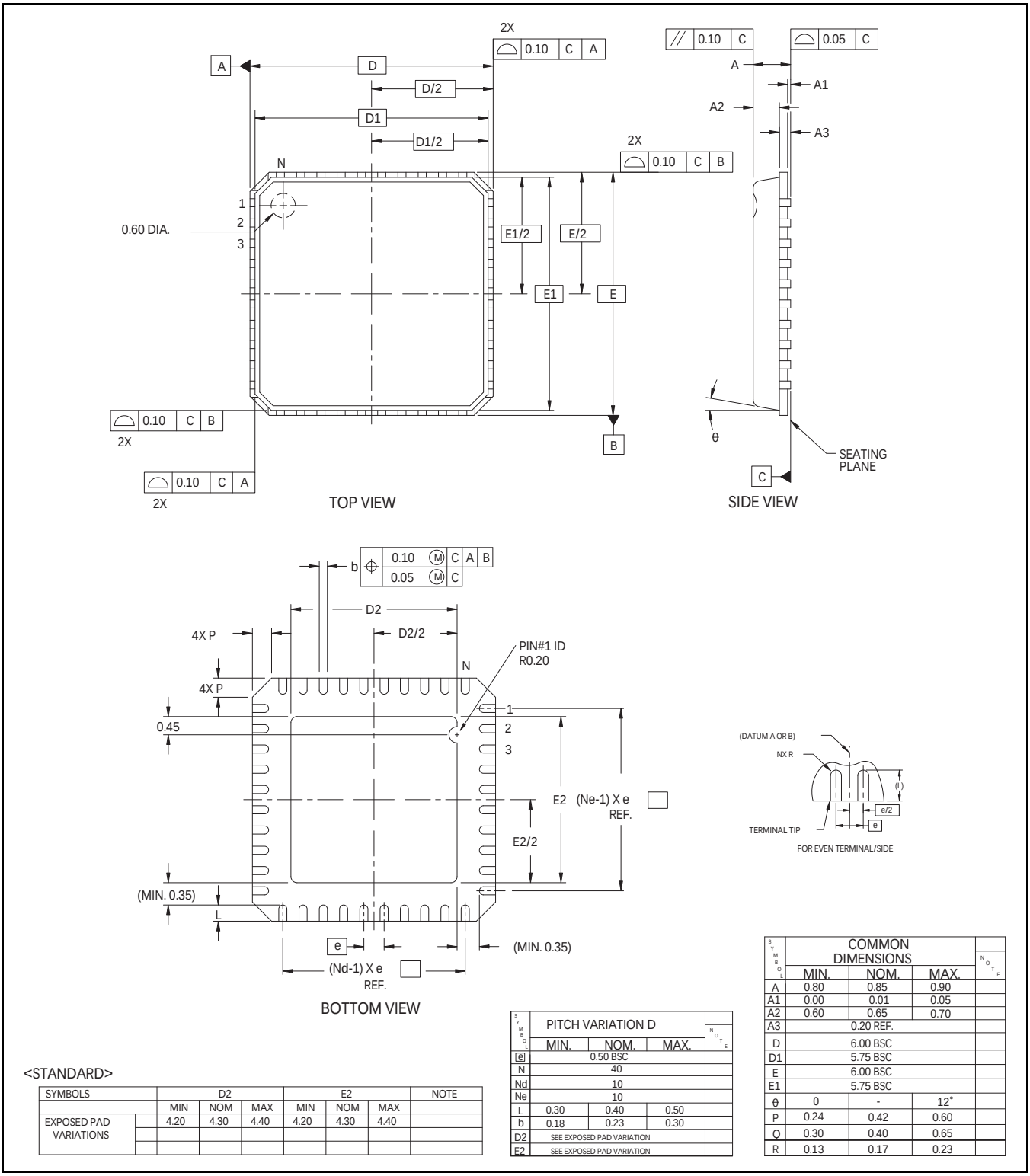


Figure 3-12. Package Outline Drawing (Amkor)



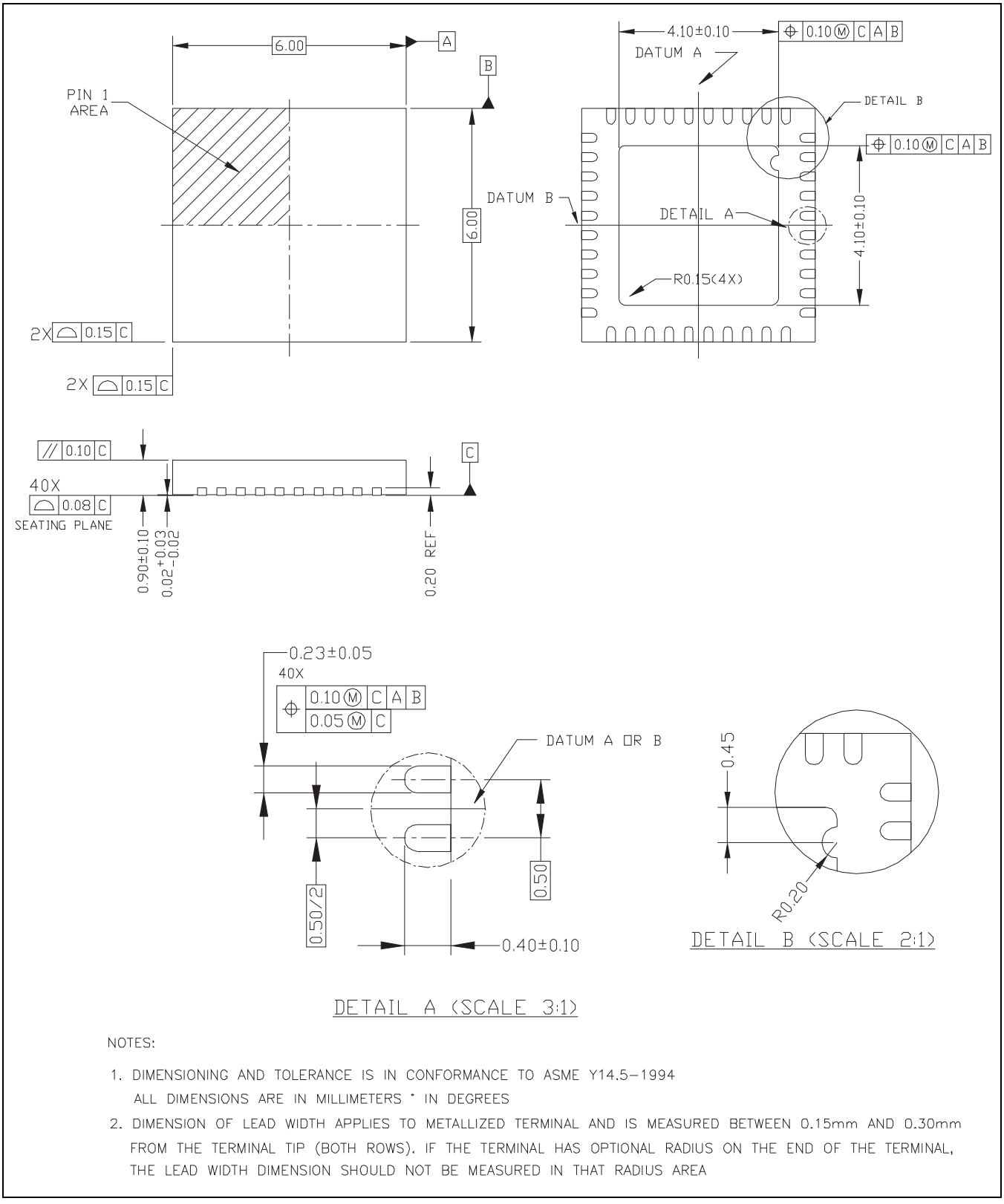
<STANDARD>

SYMBOLS		D2			E2			NOTE
		MIN	NOM	MAX	MIN	NOM	MAX	
EXPOSED PAD VARIATIONS		4.20	4.30	4.40	4.20	4.30	4.40	

SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		40		
Nd		10		
Ne		10		
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	
D2	SEE EXPOSED PAD VARIATION			
E2	SEE EXPOSED PAD VARIATION			

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.85	0.90	
A1	0.00	0.01	0.05	
A2	0.60	0.65	0.70	
A3		0.20 REF.		
D		6.00 BSC		
D1		5.75 BSC		
E		6.00 BSC		
E1		5.75 BSC		
θ	0	-	12°	
P	0.24	0.42	0.60	
Q	0.30	0.40	0.65	
R	0.13	0.17	0.23	

Figure 3-13. Package Outline Drawing (ASE)



NOTES:

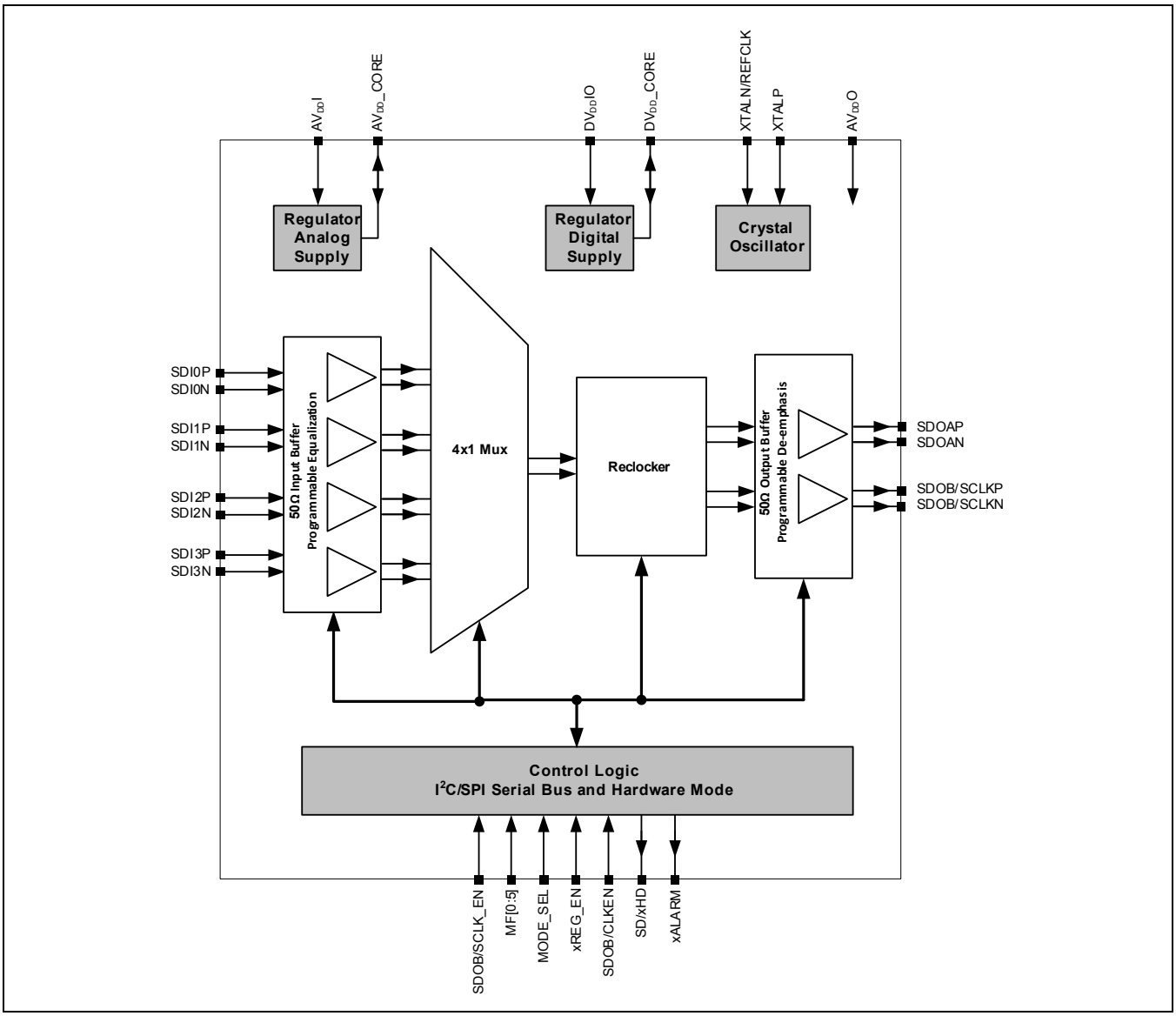
1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5–1994
   ALL DIMENSIONS ARE IN MILLIMETERS ° IN DEGREES
2. DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP (BOTH ROWS). IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA

4.0 Functional Description

4.1 Functional Block Diagram

Figure 4-1 illustrates the M08035/M08045 block diagram. The subsequent sections provide additional detail on the operation of the devices.

Figure 4-1. M08035/M08045 Block Diagram



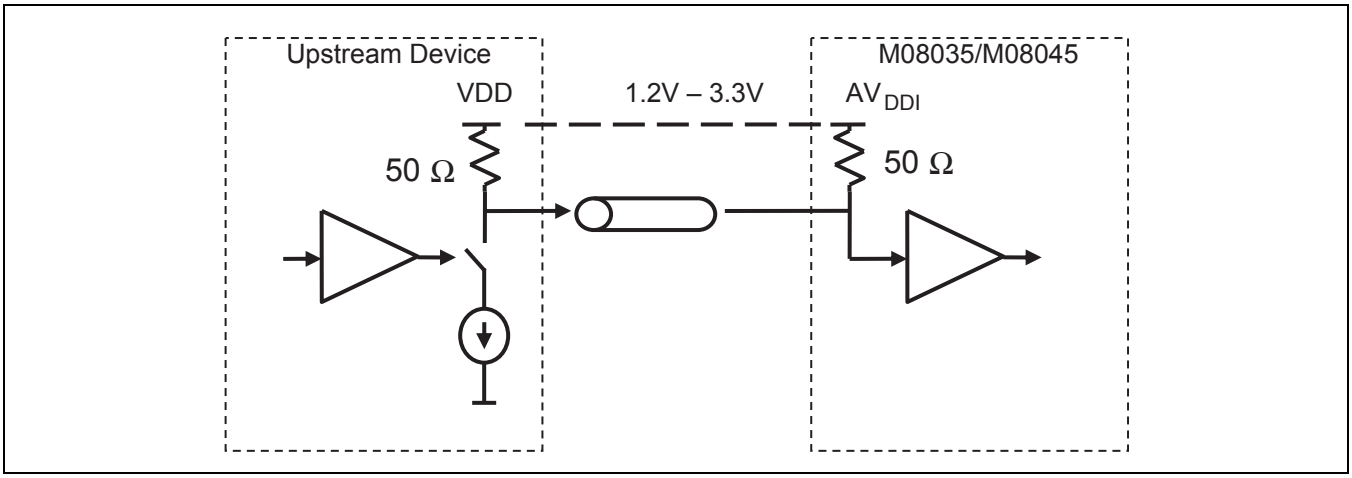
4.2 High-Speed Differential Inputs

The M08035/M08045 feature four differential inputs compatible with PCML. LVDS and LVPECL signal levels are also accommodated. Serial data to be retimed is presented to these four inputs. Each input is terminated with a 50 Ω termination to AV_{DDI}. AV_{DDI} can be supplied from any voltage ranging from 1.2 V to 3.3 V.

In order to improve signal integrity when used in large systems, each input also comes equipped with programmable input equalization (IE) for FR4 trace. There are four settings for input equalization: 0 dB (or no equalization), 2 dB, 4 dB, and 6 dB. In serial control mode, the input equalization level for each input may be set by programming the desired value to reg00h-reg03h. Alternatively, in hardware mode, the input equalization for all of the inputs may be set globally through the IE_CTRL (MF2) pin. In hardware mode only the three settings of 0 dB, 4 dB, and 6 dB are available.

In most video applications, it is important to avoid AC coupled data interfaces between devices wherever possible. In addition to reducing the number of components, DC coupling will result in more system jitter margin. In order to accommodate DC coupling with the upstream device, the AV_{DDI} power domain of the M08035/M08045 is electrically independent from all other power domains, allowing it to be tied to the V_{DD} of the upstream device. This is demonstrated in Figure 4-2 below.

Figure 4-2. M08035/M08045 AV_{DDI} Connected to the V_{DD} of the Upstream Device

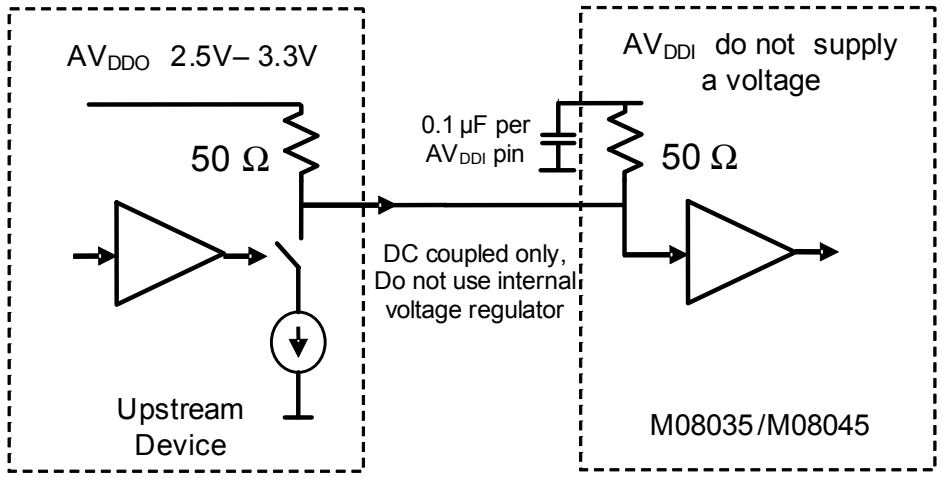


Alternatively and under certain conditions, the M08035/M08045 allow for the inputs to be self biased eliminating the need for an electrical connection between the supply voltages of the upstream device and the M08035/M08045. This configuration offers the benefit of keeping the supply of the previous device and the power domain(s) of the M08035/M08045 completely isolated, while using DC coupling. AC coupling should not be used with the self bias interface. This self biasing scheme is demonstrated in Figure 4-3 below.

When using the M08035/M08045 in self biased mode, specific conditions must be met:

1. The self biased inputs must be DC coupled. No AC coupling is supported in self biased mode.
2. The AV_{DDO} of the upstream device must be 2.5 V or greater. AV_{DDO} levels 1.2 V and 1.8 V are not supported in this mode.
3. The common mode of the upstream signals must be greater than 600 mV.
4. Internal voltage regulators are disabled.
5. All inputs are configured in self biased mode. Combination of self biased and non-self biased is not supported.

Figure 4-3. Self Biasing the Input of M08035/M08045



NOTE:

1. For self bias applications, no voltage must be applied to the AV_{DDI} pin. Every AV_{DDI} pin should be decoupled to GND with a 0.1 µF capacitor as shown in Figure 4-3.

A Loss of Signal (LOS) detector monitors each input and issues an alarm when the input signal level dips below the detection threshold set in register 06h. See Section 4.3 for more information on the LOS circuit.

In order to correct any duty cycle distortion (DCD) in the input signal, or any DC offset buildup in the internal signal path, a DC correction loop has been added. Programming register 0Dh bit 1 to a '1' will disable the DC correction loop for all inputs.

The M08035/M08045 include a 4:1 multiplexer. This allows any one of the four input signals to be routed to the reclocker. By default SDI0 is selected to be routed to SDO0. The selected input can be set using MUX control register 07h.

By default, only the selected input is powered up, with all other inputs powered down. When an input is powered down, its associated LOS circuitry is disabled. If required, all the other inputs can also be powered up by setting bit[3] in register 0Dh. This will allow a faster response if rapid input switching is required as there is no delay waiting for the circuitry to power-up and adjust to the input signal, but has the disadvantage of consuming more power.

With all inputs enabled, the power consumption increases by 100 mW.

4.3 LOS (Loss of Signal)

The M08035/M08045 have integrated LOS circuits on each of their four high-speed inputs. This circuit monitors the input amplitude and if it falls below the detection threshold it asserts the LOS alarm bit by setting this to a logic high. These alarm bits are latched and will need to be reset with the CLR_ALARMS, register 85h, by setting bit 0 to a high and back to a low. Hysteresis is built into the LOS circuit to avoid chattering. The LOS threshold can be set to a different level by using the bits[7:5] in register 06h, this changes the level on all four inputs.

By default, the LOS alarm mutes the signal from that particular input. Setting register 06h bit[3] to a high will disable this feature.

4.4 High-Speed Output Description

There are two high-speed outputs available on the M08035/M08045. By default, only SDOA is powered up, setting bit 2 of register 0Ch high will enable SDOB. The output signal will be a copy of SDOA. In hardware mode, SDOB is enabled with the SDOB/SCLK_EN input pin in a floating (F) or high (H) (see Table 3-1).

A further function of this output is a serial clock source. By setting register 06h, bit 0 to high, the reclockers recovered clock is output to the SDOB/SCLK pins. In hardware mode this function is selected by setting SDOB/SCLK_EN high (see Table 3-1).

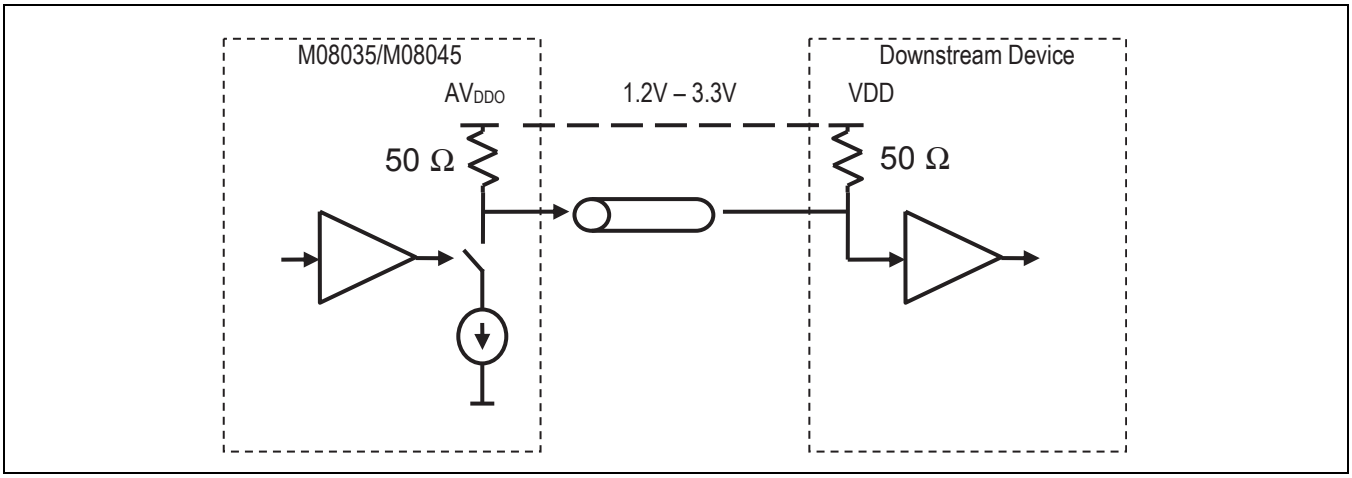
The M08035/M08045 feature differential current mode logic (CML) drivers with integrated 50 Ω pull ups to AV_{DDO} for the output of each reclocker channel. AV_{DDO} may be supplied from any voltage ranging from 1.2 V to 3.3 V.

The differential, peak-to-peak, output swing for each CML driver is programmable and may be set to 600 mV_{PPD}, 800 mV_{PPD}, or 1200 mV_{PPD}. Please note that the 1200 mV_{PPD} output swing setting is only available when AV_{DDO} is supplied from a voltage of 1.8 V or greater. The swing setting may be programmed by writing to register 09h for SDOA, and register 0Bh for SDOB.

In order to improve signal integrity when used in large systems, each output also comes equipped with programmable de-emphasis (DE) for FR4 trace. There are four settings for output de-emphasis: 0 dB (or no DE), 2 dB, 4 dB, and 6 dB. In serial control mode, the output de-emphasis level for each input may be set by programming the desired value to register 09h for SDOA and register 0Ah for SDOB. Alternatively, in hardware mode, the de-emphasis level for all of the outputs may be globally set through pin DE_CTRL (MF3). In hardware mode only the three settings of 0 dB, 4 dB, and 6 dB are available.

In most video applications, it is important to avoid AC coupled data interfaces between devices wherever possible. In addition to reducing the number of components, DC coupling will result in more system jitter margin. In order to accommodate DC coupling with the upstream device, the AV_{DDO} power domain of the M08035/M08045 is electrically independent from all other power domains therefore allowing it to be tied to the V_{DD} of the downstream device. This is demonstrated in Figure 4-4 below.

Figure 4-4. M08035/M08045 AV_{DDO} Connected to the V_{DD} of the Downstream Device



If AC coupling is desired or necessary, then the capacitor should be at least 10 µF.

4.5 Logic Signals

To allow interfacing to logic levels other than the 1.2 V core voltage, or any of the analog input and output supplies, the digital interface signals are referenced to DV_{DDIO} which is an isolated power domain. DV_{DDIO} may be supplied from any voltage ranging from 1.2 V to 3.3 V. Many digital control pins have three states, high (H), low (L), or floating (F). In order to assert the F or floating state, the pin must be left unconnected or undriven.

4.6 Control Modes

The M08035/M08045 may be configured in four separate control modes. The control mode is determined by the setting of the MODE_SEL pin as shown in Table 4-1 below.

Table 4-1. Control Mode Setting

MODE_SEL	Control Mode
MODE_SEL = F	Hardware Control Mode (HIC)
MODE_SEL = H	Four-wire Serial Interface Control Mode (SIC4 or SPI)
MODE_SEL = L	Two-wire Serial Interface control Mode (SIC2 or I^2C)
	Memory Interface Configuration Mode (MIC) When the reclocker is configured through an external EEPROM

The MIC mode is a subset of the two-wire Interface mode and is initiated by writing to special reserved address when the device is set in two-wire Interface mode.

4.6.1 HIC Mode

Configuring the M08035/M08045 in hardware mode avoids the complication of adding a microcontroller, but offers limited control options. When in hardware mode, the MF (Multi Function IO) pins are configured as shown in Table 4-2 below.

Table 4-2. MF Pin Configuration in Hardware Mode

MF	HIC Mode Pin Name	Function
MF2	IE_CTRL	Input trace equalization control for all SDI inputs H = 6 dB Input EQ F = 2 dB Input EQ L = 0 dB Input EQ
MF3	DE_CTRL	Output de-emphasis (DE) control for all SDO outputs H = 6 dB of output DE F = 4 dB of output DE L = 0 dB output DE
MF4	RC_BYPASS	Reclockers bypass control for all outputs L/H = Normal operation, Reclocker not bypassed H = Reclocker bypassed
MF5	SDO_DIS	SDO disable control for all outputs H = SDO disabled output logic high L/F = SDO enabled

NOTE: In this mode, xALARM is not supported.

4.6.2 Four-wire Interface Mode (SIC4)

In this mode, a four-wire serial interface is used to program the device's internal registers, configuring the operation of the M08035/M08045. When in SIC4 mode, MF[0:3] pins comprise the four-wire bus as shown in Table 4-3 below.

Table 4-3. MF Pin Configuration in Four-wire Interface Mode

MF	SIC4 Mode Pin Name	Function
MF0	SCLK	Serial clock input
MF1	SO	Serial data output
MF2	SI	Serial Data input
MF3	xCS	Chip Select (active low)

The interface shifts data in from the external controller on the rising edge of SCLK. The serial I/O operation is gated by xCS. Data is shifted in to the M08035/M08045 from the Host (Master) to SI on the falling edge of SCLK, and shifted out through SO on the rising edge of SCLK. To address a register, a 10-bit input needs to be shifted, consisting of the first bit (Start Bit, SB = 1), the second bit (Operation Bit, OP = 1 for read, = 0 for write), and the 8-bit address (MSB first).

Figure 4-5. Four-wire Interface Word Format

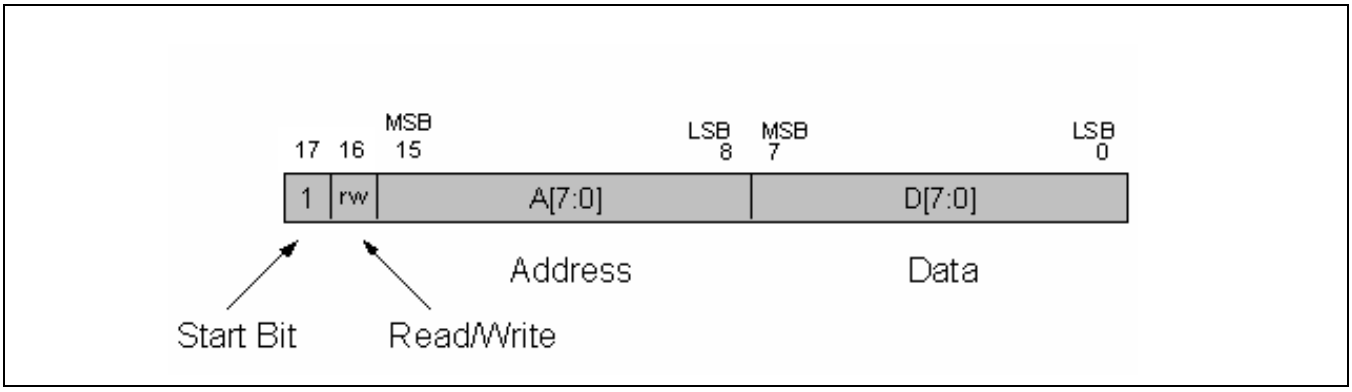
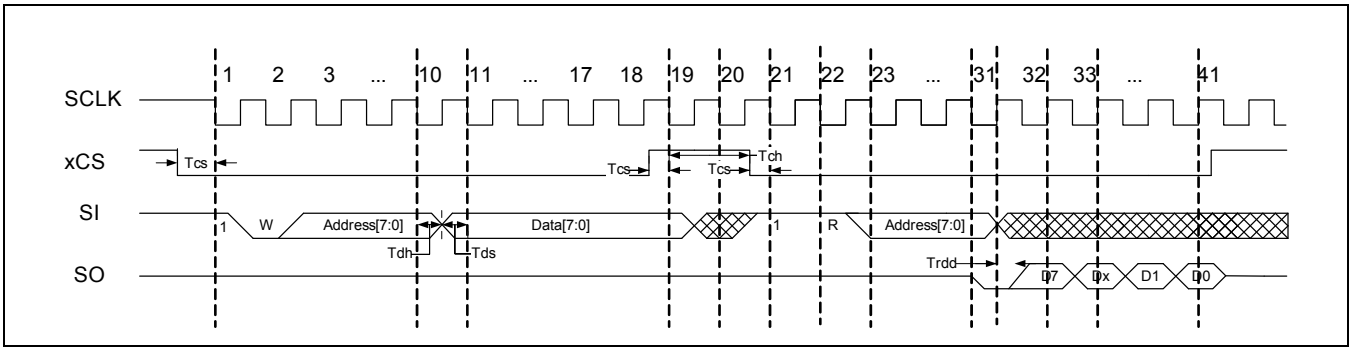


Figure 4-6 illustrates a Serial Write Mode followed by a Serial Read mode. To initiate a Write sequence, xCS goes low before the falling edge of SCLK. On each falling edge of the clock, the 18 bits consisting of the SB = 1, OP = 0, ADDR, and DATA, are latched into the input shift register through SI. The rising edge of xCS may occur before or after the falling edge of SCLK for the last bit. Upon receipt of the last bit, one additional cycle of SCLK is necessary before DATA transfers from the input shift register to the addressed register.

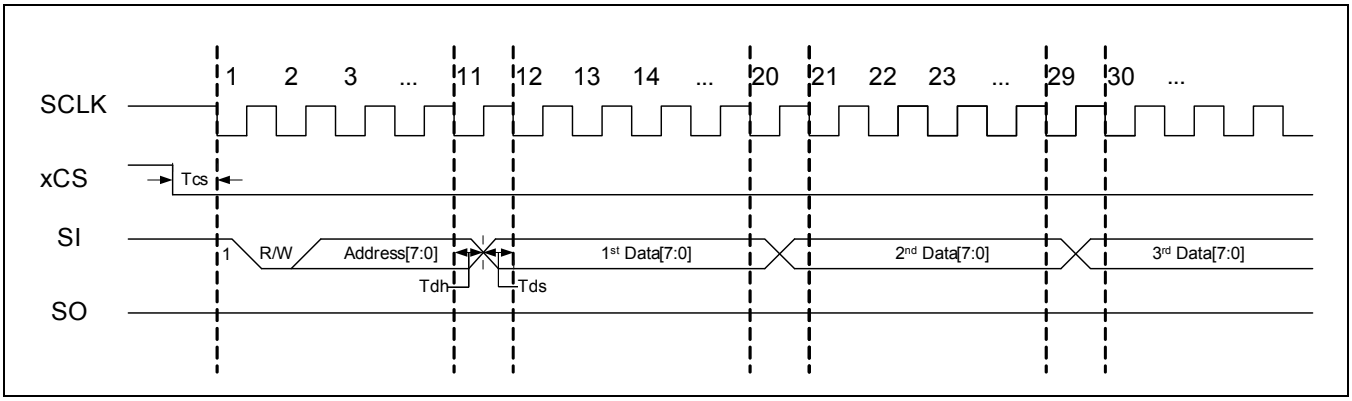
To initiate a read sequence, xCS goes low before the falling edge of SCLK. On each falling edge of SCLK, the 10 bits consisting of SB = 1, OP = 1, and the 8-bit ADDR are written to the serial input shift register and copied to the serial output shift register. On the next rising edge after the address LSB, the SB and 8 bits of the DATA are shifted out. The SB for a Read is always 1.

Figure 4-6. Four-Wire Write Followed by a Read Sequence



The 4-wire interface supports multiple consecutive writes. In this case, the address header is not needed and each additional 8 bits of data will be written into consecutive addresses. If consecutive read/write cycles are being performed, it is not necessary to insert an extra clock cycle between read/write cycles, however one extra clock cycle is needed after the last data bit of the last read/write cycle.

Figure 4-7. Four-Wire Sequential WRITE



On a Write cycle, any bits that follow the expected number of bits are ignored, and only the first 15 bits following SB and OP are used. On a Read cycle, any extra clock cycles will result in the repeat of the data LSB. An invalid SB or OP renders the operation undefined. The falling edge of xCS always resets the serial operation for a new Read or Write cycle.

Detailed timing information is shown below.

Table 4-4. Four-wire Interface Timing

Timing Symbol	Description	Min	Max	Unit
Tds	Data set-up time	5	—	ns
Tdh	Data hold time	5	—	ns
Tcs	xCS set-up time	5	—	ns
Tch	xCS hold time	5	—	ns
Tfreq, write	Four-wire interface write clock frequency	—	40	MHz
Tfreq, read	Four-wire interface clock read frequency, DV_{DDIO}=2.5 V or 3.3 V	—	40	MHz
	Four-wire interface read clock frequency, DV_{DDIO}=1.8 V	—	20	MHz
	Four-wire interface read clock frequency, DV_{DDIO}=1.2 V	—	5	MHz
T_{DUTY}	SCLK duty cycle	40	60	%
Tdd	Read data output delay (measured with max 30 pF loading, DV_{DDIO}=3.3 V)	1	8	ns

4.6.3 Two-wire Interface Mode (SIC2)

In this mode a two-wire serial interface is used to program the device's internal registers, configuring the operation of the M08035/M08045. When in SIC2 mode, MF[0:5] pins are configured as shown below.

Table 4-5. MF Pin Configuration in Two-wire Interface Mode

MF	SIC4 Mode Pin Name	Function
MF0	SCL	Clock input from master host
MF1	SDA	Serial data input/output
MF2	ADD0	Address bit 0
MF3	ADD1	Address bit 1
MF4	ADD2	Address bit 2
MF5	ADD3	Address bit 3

Each device has an individual address and is addressed using an address byte, which is latched upon Power-On-Reset (POR). In this mode, the M08035/M08045 are I^2C-compatible slave devices that can operate at 100 kHz and 400 kHz for all allowed voltages seen at the DV_{DDIO} pin.

The M08035/M08045 allow for forty different addresses to be programmed using the inputs ADD[3:0]; these inputs have three states, low (L), high (H) and floating (F). The slave addresses are from 21h to 48h.

Table 4-6. M08035/M08045 2-Wire Interface Address Map (1 of 2)

Dec Add	Hex Add	Bin Add	Pin Setting				Function
			ADD3	ADD2	ADD1	ADD0	
32	20	010 0000b	L	L	L	L	EEPROM only, Address 50h
32	20	010 0000b	L	L	L	H	EEPROM only, Address 51h
32	20	010 0000b	L	L	H	L	EEPROM only, Address 52h
32	20	010 0000b	L	L	H	H	EEPROM only, Address 53h
33	21	010 0001b	L	H	L	L	Slave 1
34	22	010 0010b	L	H	L	H	Slave 2
35	23	010 0011b	L	H	L	F	Slave 3
36	24	010 0100 b	L	H	H	L	Slave 4
37	25	010 0101b	L	H	H	H	Slave 5
38	26	010 0110b	L	H	H	F	Slave 6
39	27	010 0111b	L	H	F	L	Slave 7
40	28	010 1000 b	L	H	F	H	Slave 8
41	29	010 1001b	L	H	F	F	Slave 9
42	2A	010 1010b	L	F	L	L	Slave 10
43	2B	010 1011b	L	F	L	H	Slave 11
44	2C	010 1100b	L	F	L	F	Slave 12
45	2D	010 1101b	L	F	H	L	Slave 13

Table 4-6. M08035/M08045 2-Wire Interface Address Map (2 of 2)

Dec Add	Hex Add	Bin Add	Pin Setting				Function
			ADD3	ADD2	ADD1	ADD0	
46	2E	010 1110b	L	F	H	H	Slave 14
47	2F	010 1111b	L	F	H	F	Slave 15
48	30	011 0000 b	L	F	F	L	Slave 16
49	31	011 0001 b	L	F	F	H	Slave 17
50	32	011 0010 b	L	F	F	F	Slave 18
51	33	011 0011 b	F	L	L	L	Slave 19
52	34	011 0100 b	F	L	L	H	Slave 20
53	35	011 0101 b	F	L	L	F	Slave 21
54	36	011 0110 b	F	L	H	L	Slave 22
55	37	011 0111 b	F	L	H	H	Slave 23
56	38	011 1000 b	F	L	H	F	Slave 24
57	39	011 1001b	F	L	F	L	Slave 25
58	3A	011 1010b	F	L	F	H	Slave 26
59	3B	011 1011b	F	L	F	F	Slave 27
60	3C	011 1100b	F	H	L	L	Slave 28
61	3D	011 1101b	F	H	L	H	Slave 29
62	3E	011 1110b	F	H	L	F	Slave 30
63	3F	011 1111b	F	H	H	L	Slave 31
64	40	100 0000b	F	H	H	H	Slave 32
65	41	100 0001b	F	H	H	F	Slave 33
66	42	100 0010b	F	H	F	L	Slave 34
67	43	100 0011b	F	H	F	H	Slave 35
68	44	100 0100 b	F	H	F	F	Slave 36
69	45	100 0101b	F	F	L	L	Slave 37
70	46	100 0110b	F	F	L	H	Slave 38
71	47	100 0111b	F	F	L	F	Slave 39
72	48	100 1000 b	F	F	H	L	Slave 40

Table 4-7. Supported AT24C01 EEPROM Addresses

Dec Add	Hex Add	Bin Add	Fixed by EEPROM				Address Pin Setting		
			ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
80	50	010 0000b	H	L	H	L	L	L	L
81	51	010 0001b	H	L	H	L	L	L	H
82	52	010 0010b	H	L	H	L	L	H	L
83	53	010 0011b	H	L	H	L	L	H	H

Figure 4-8 illustrates typical waveforms and timing seen at SCL and SDA for a read and write operation.

Figure 4-8. Two-wire Interface Timing Diagram

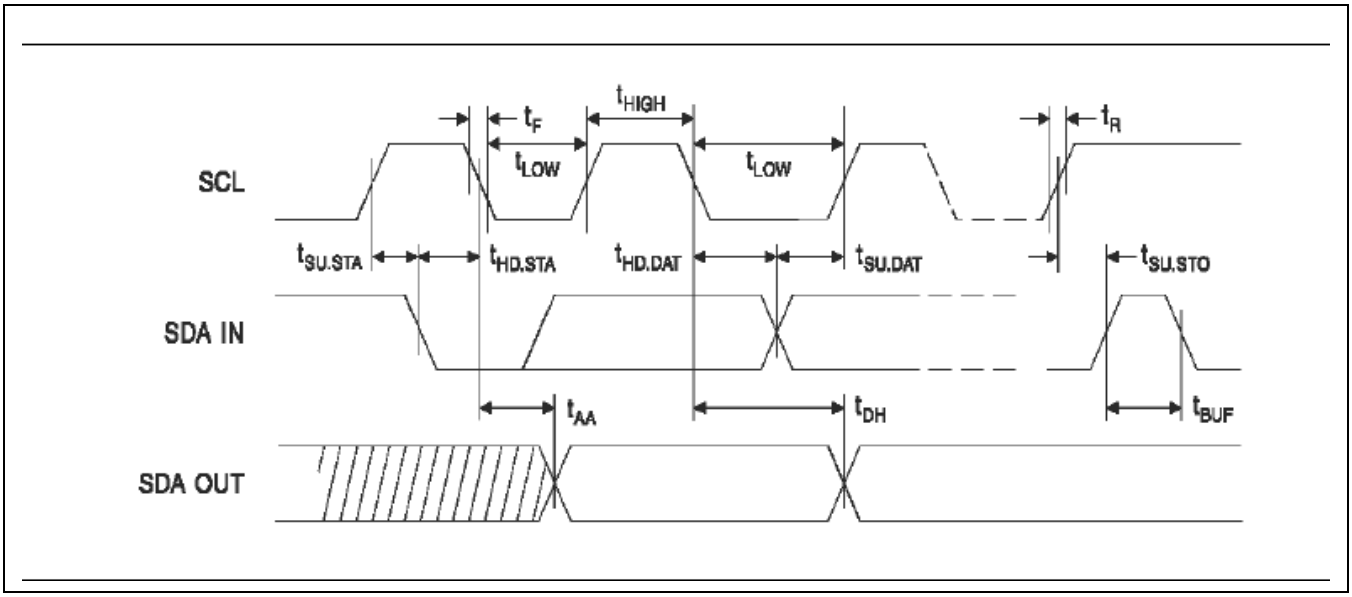


Table 4-8. Two-wire Interface Timing Specifications (Standard Mode or Fast Mode)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
f_{SCL}	Clock Frequency, SCL	—	—	400	kHz
t_{LOW}	Clock Pulse Width Low	1.3	—	—	µs
t_{HIGH}	Clock Pulse Width High	1	—	—	µs
t_{AA}	Clock Low to Data Out Valid	0.05	—	0.9	µs
t_{HDSTA}	Start Hold Time	200	—	—	ns
t_{SUSTA}	Start Set-up Time	200	—	—	ns
t_{HDDAT}	Data In Hold Time	0	—	—	ns
t_{SUDAT}	Data In Set-up Time	100	—	—	ns
t_{SUSTO}	Stop Set-up Time	200	—	—	ns
t_{DH}	Data Out Hold Time	50	—	—	ns

Notes:
500 pF @ 100 kHz and 250 pF @ 400 kHz with 1k Ω pull-up.

4.6.4 MIC Mode Operation

In this mode, the reclocker is initialized with an EEPROM. To use this mode, the EEPROM must be programmed with the register data required. The I^2C address of the memory can be 50h, 51h, 52h or 53h; the reclocker loads its register contents from this address.

This mode is enabled when the I^2C mode is set and address 20h has been hardwired on the address pins. When the reclocker locates the memory at one of the above addresses, it sets itself into I^2C quasi-master mode. It will then load its registers from the EEPROM. Addresses 00h to 19h should be used when only one reclocker is used. Register 0Fh contains the number of slave reclockers; if there are none this is set to 0.

Once the master has finished the task of downloading the registers, it will revert to slave mode at address 20h and can be accessed for debugging purposes.

Note that when using MIC power mode supply, ramp time is important. The EEPROM should be powered from the same supply as DV_{DDIO} and the ramp up of the supply should be < 100 ms. If the ramp time is not met, the reclocker I^2C will time-out before the EEPROM is ready to receive serial data.

The target EEPROM is the AT24C01 or equivalent.

If there is more than one reclocker to be programmed, a checksum is used to confirm that the data is correct. This works as follows:

1. The slave reclocker sums all registers from 00h to 1Ah, then truncates this to leave the 8 LSB bits. This is then compared with the value 2Eh. If it is not equal, then the registers are not loaded and it returns to the default value. It will then try up to 512 times before timing out. When the checksum is equal to 2Eh, the registers are loaded with the EEPROM settings.
2. To make the checksum = 2Eh, register 1Ah must be programmed with the 8 LSBs from the following calculation:

   Register 1Ah = 2Eh - (sum of registers 00h to 19h)

4.7 Reclocker Operation

4.7.1 Clock Recovery

This block generates a serial clock signal at a frequency close to the data rate. The clock signal is generated by a phased locked loop (PLL) which uses the 27 MHz input clock as a reference.

The presence of the reference clock is monitored by the device. An alarm bit (NOREF) in register 88h is set to '1' when a suitable reference clock is not present. Once the PLL has locked to the reference clock, the REFLOL bit in the same register will be set to '0'. A value of '1' in this bit indicates that the PLL has not locked to the input reference clock.

The frequency locked clock signal is supplied to the phase lock block. In this block, a bang-bang phase comparator is used to make fine adjustments to the phase and frequency of the clock, aligning it with the incoming serial data.

Once the clock signal is phase and frequency aligned with the serial data stream, it is used to re-time the data, producing a clean data signal that is provided at the output of the device. The phase lock block uses an integrated, programmable loop filter. The bandwidth of the phase lock block may be programmed using the BW[2:0] bits in register 16h. A wide bandwidth increases the jitter tolerance and reduces the lock time of the loop. However, a wide bandwidth also allows more jitter from the input serial data stream to be transferred to the output. Alternatively, a low bandwidth setting causes the loop to reject more of the incoming data stream's jitter, while increasing lock time, and reducing input jitter tolerance. The bandwidth setting can be optimized for each system.

Furthermore, since the phase lock block uses a non-linear, bang-bang loop, the bandwidth of the system is inversely proportional to the incoming data stream's jitter. This offers several advantages over linear PLLs. It achieves higher jitter attenuation with large input jitter, while it corrects for small variations quickly with low input jitter. With higher input jitter, the loop automatically reduces the bandwidth, causing more of the jitter to be rejected. Conversely, a data stream with lower jitter will cause the loop bandwidth to be widened. Note that bandwidth settings greater than 2x will increase output jitter.

When the recovered serial clock output is enabled, the clock alignment to the SDOA data output will be typically 60 ps, where the falling edge of the clock lags the transition edge of the SDOA signal.

4.7.2 Automatic Rate Detection

The reclocker features an Automatic Rate Detector (ARD) circuit that monitors the input signal rate and automatically sets the reclocker to the correct video rate. The data rate determined by the ARD block may be read from bits 1:0 in register 89h as shown in Table 4-9.

Table 4-9. Reclocker Rate Detection

Reg89h (Bits 1:0)	Function
00b	Reclocker unlocked
01b	SD rate detected
10b	HD rate detected
11b	3G rate detected (M08045)

As an alternative to the ARD, the user may manually set the reclocker to the desired data rate by programming bits[3:2] in register 12h to the desired values as shown in Table 4-10.

Table 4-10. Reclocker Data Rate Selection

Reg12h (Bits 3:2)	Function
00b	ARD Enabled
01b	Manual SD rate programmed
10b	Manual HD rate programmed
11b	Manual 3G rate programmed (M08045)

Please note that when configured in manual ARD mode, the reclocker is guaranteed to lock to the program data rate. However, it may also lock to the harmonics of that program data rate as well. For example, if the reclocker is programmed to lock to HD data, it will also try to lock to 3G data as 2.97 Gbps is exactly twice 1.485 Gbps.

When in auto-bypass mode, if the ARD cannot determine the rate of the input data stream, it will switch the reclocker into bypass mode. This allows a data rate other than those specified to be passed through the reclocker. The auto-bypass mode may be disabled through Register 14h.

4.7.3 Lock Detection

Several circuits monitor each reclocker for Loss of Lock. One in particular compares the recovered serial clock to one derived from the reference clock. If the clock frequency is within ±2000 ppm of the serial data frequency, the Loss of Lock (LOL) alarm will be set to '0'. If the clock is outside of this window, then the LOL alarm will be asserted to '1'.

The LOL bit can be read from bit[0] in register 88h.

4.7.4 Reference Clock

The M08035/M08045 can operate from a crystal or an external reference clock, but better jitter results are obtained with a crystal. If using an external reference clock, this should be a 27 MHz clock with a frequency accuracy of ±100 ppm or better. Reference clock jitter is important and care must be taken to supply a low jitter reference clock to the reclocker of 1 ps RMS or less. The reference clock may either be from an external CMOS clock oscillator or an external parallel resonance crystal. If a low jitter 27 MHz signal is already available on the board then it may be used. Due to the higher jitter, a genlocked 27 MHz clock is likely not suitable for this device. When supplying an external clock signal, it is recommended to use AC coupling through a 0.1 µF capacitor. Refer to Table 1-7 for recommended input levels.

4.8 SD/xHD Output

When the reclocker is locked to the input data, the SD/xHD output indicates whether an SD or HD rate is detected. When a 3G rate is being received, the output will indicate HD. This output is designed to be connected to the slew rate control on a downstream cable driver.

The SD/xHD pin has two available modes as shown in Table 4-11. These are controlled by the SDALG bit, reg 18h[5], by default this is a 0 and only goes high when the reclocker is locked to a 270 Mbps input signal. This mode sets the fast edge on the cable driver and allows for any signal in the reclockers data range to be bypassed. If the slow edge is set, any signal above 540 Mbps would be distorted by the slow edge on the cable driver.

When SDALG is high it also sets the SD/xHD pin high when the reclocker is unlocked. This is used when the user requires other SD rates such as 143 Mbps and 360 Mbps to be output from the cable driver with the slow SD edge when the reclocker is not locked.

Table 4-11. SD/xHD Output Algorithm

Rate (Gbps)	SD/xHD Pin	
	SDALG Bit = 0	SDALG Bit = 1
0.270	H	H
1.485/1.4835	L	L
2.97/2.967	L	L
unlocked	L	H

4.9 xALARM

The xALARM output pin is provided so the user can monitor alarm activity on the reclocker. The output is open drain as shown in Figure 3-10. Table 4-12 shows the reclocker alarms and their function. The assertion of any of the alarms in Table 4-12 will trigger xALARM.

NOTE: Please note that xAlarm is not supported in hardware control mode (HIC).

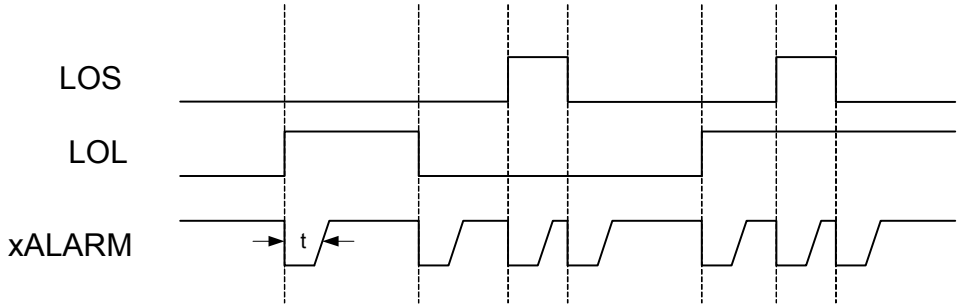
Table 4-12. Reclocker Alarm Function

Alarm	Function
LOS	Asserted when input signal goes below LOS threshold as set in register 06h.
LOL	Asserted when reclocker cannot lock to the incoming data.
NOREF	Asserted when no input reference is present at the reference clock inputs.
REFLOL	Asserted when frequency lock block cannot lock to the reference clock input.

The xAlarm pin may be used when the device is controlled using standard four-wire or two-wire serial interfaces (SIC4 and SIC2). The xAlarm pin operates in an interrupt mode. It goes low on the assertion of any of the internal alarm flags and stays low for a fixed period of time before returning to high (see Figure 4-9). This period is set by the Interrupt Control register (0Eh). By default this is 0 and that corresponds to 20 ns. The maximum period is 2.560 µs, when INT[3:0] is set to Fh.

The xAlarm pin is designed to be connected to a microprocessor's interrupt pin. After the interrupt occurs, the microprocessor can read the reclocker's alarm registers to determine which alarm was asserted.

Figure 4-9. xALARM-Output Interrupt Mode



Interrupt occurs when LOS or LOL changes state.
xALARM pulse width is programmable.

4.9.1 Reading Register Alarm Bits

The LOS and LOL alarm bits are latched when asserted. After reading they should be cleared using the CLRALRM bit in register 88h. This bit needs to be set to '1' to reset the alarms. It should then be reset to a '0' to re-enable normal alarm operation.

4.10 Internal Regulator

Both digital and analog cores of the M08035/M08045 are designed to run from a 1.2 V supply. If a 1.2 V supply is not available locally, then the internal regulator can be used to create this domain from AV_{DDI}/AV_{DDO} and DV_{DDIO}. Setting the xREG_EN pin LOW, enables the internal regulator. This regulator generates a 1.2 V domain at pins AV_{DD} and DV_{DD}. See Figure 4-10 through Figure 4-12 for the three different supply configurations. Note that the decoupling capacitors should be at least 100 nF.

When the internal regulator is used, all the current for the device is taken through the AV_{DDI}/AV_{DDO} and DV_{DDIO} pins. Because of this, care should be taken to ensure that the supplies to these pins are sufficient to handle the total current.

Figure 4-10. All Power Pins Connected to 1.2 V, Internal Regulators Not Used

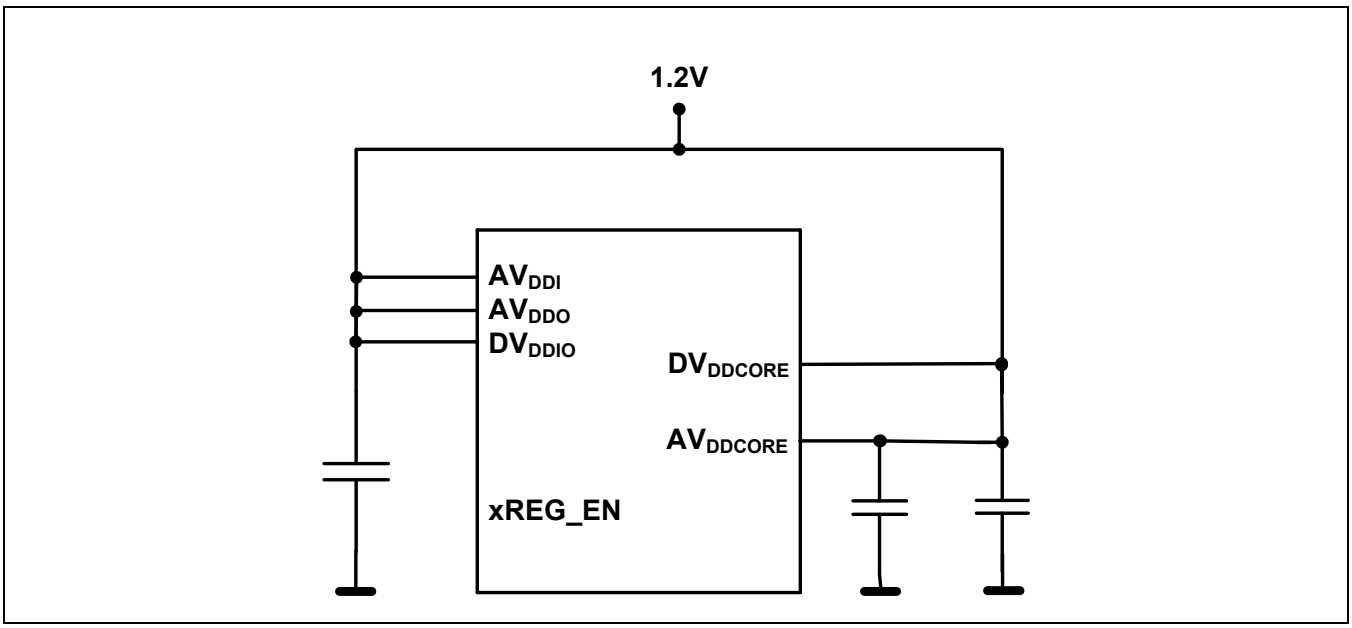


Figure 4-11. AV_{DDI}, AV_{DDO}, and DV_{DDIO} Connected to a Supply at 1.8 V or 3.3 V, 1.2 V is Supplied to AV_{DD} and DV_{DD}, Internal Regulator not Used

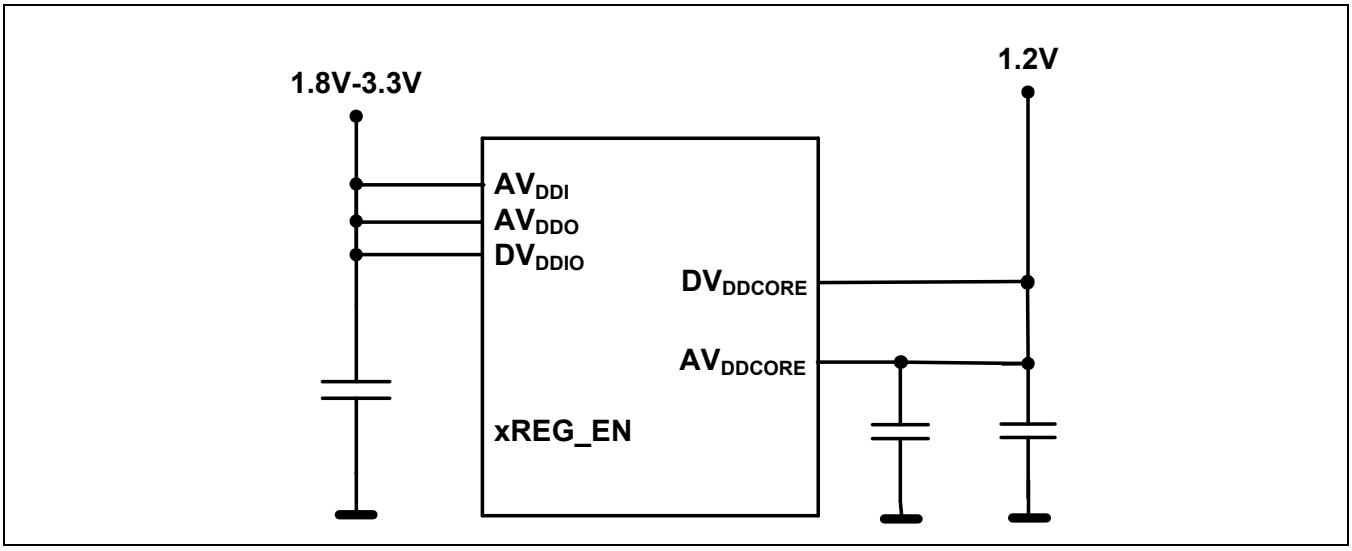
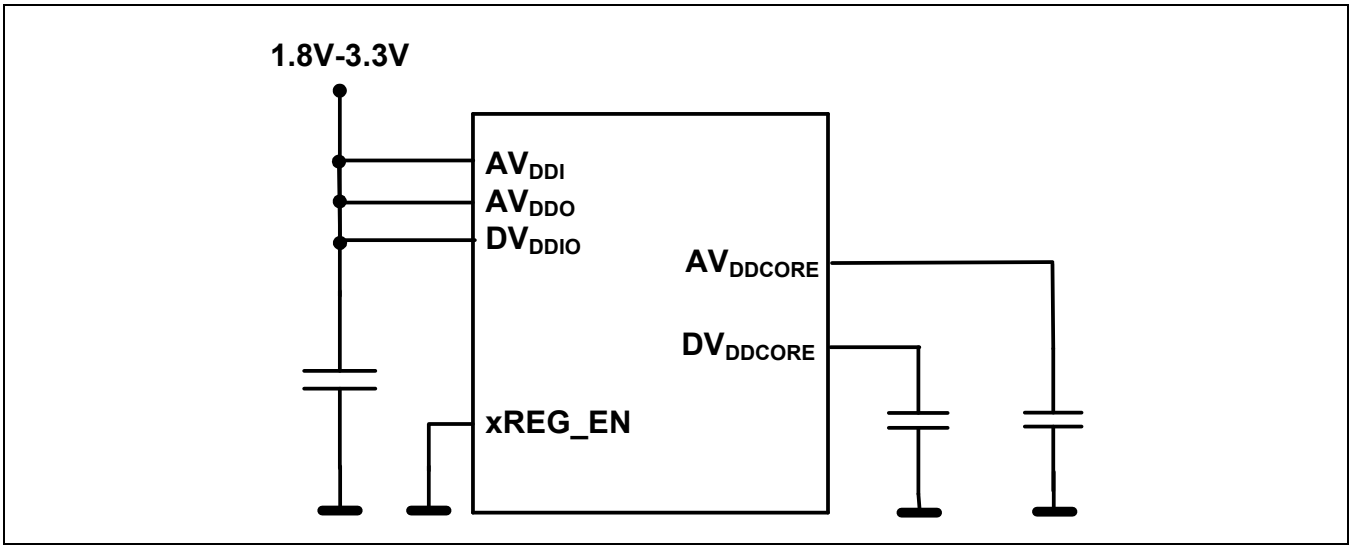


Figure 4-12. AV_{DDI}, AV_{DDO}, and DV_{DDIO} Connected to a Supply at 1.8 V or 3.3 V. Internal Regulator Generates On-Chip 1.2 V



Note: In order to simplify the diagrams, AV_{DDI}, AV_{DDO}, and DV_{DDIO} are shown to be shorted together. In practice, they may all be separated and connected to different supply domains if desired.

AV_{DDO} is sensitive to noise and therefore should be filtered through a ferrite bead, with a 10 nF ceramic capacitor adjacent to each AV_{DDO} pin. Since this core can take a current in the order of 500 mA, the ferrite bead should be very low resistance to ensure the drop across it is minimal.

5.0 Control Registers Map and Descriptions

Table 5-1. M08035/M08045 Register Map (1 of 2)

Addr	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
Input/Output Configuration											
00h	Input EQ Config 0	*RSVD*	*RSVD*	IE0[1]	IE0[0]	*RSVD*	*RSVD*	*RSVD*	*RSVD*	00h	R/W
01h	Input EQ Config 1	*RSVD*	*RSVD*	*RSVD*	*RSVD*	IE1[1]	IE1[0]	*RSVD*	*RSVD*	00h	R/W
02h	Input EQ Config 2	*RSVD*	*RSVD*	*RSVD*	*RSVD*	IE2[1]	IE2[0]	*RSVD*	*RSVD*	00h	R/W
03h	Input EQ Config 3	*RSVD*	*RSVD*	*RSVD*	*RSVD*	IE3[1]	IE3[0]	*RSVD*	*RSVD*	00h	R/W
04h	Input Polarity Flip 0	*RSVD*	*RSVD*	POL1	*RSVD*	*RSVD*	POL0	*RSVD*	*RSVD*	00h	R/W
05h	Input Polarity Flip 1	*RSVD*	*RSVD*	POL3	*RSVD*	*RSVD*	*RSVD*	POL2	*RSVD*	00h	R/W
06h	LOS Config/CLK EN	LVL[2]	LVL[1]	LVL[0]	F_LOS	NVRSQ	SQPOL	RSVD	SCLK_EN	20h	R/W
07h	Input MUX CTRL	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	IN[1]	IN[0]	40h	R/W
08h	RSVD	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	C8h	R/W
09h	SDOA CTRL	*RSVD*	*RSVD*	*RSVD*	*RSVD*	LVL_A[1]	LVL_A[0]	DE_A[1]	DE_A[0]	88h	R/W
0Ah	SDOB CTRL DE	*RSVD*	*RSVD*	DE_B[1]	DE_B[0]	*RSVD*	*RSVD*	*RSVD*	*RSVD*	00h	R/W
0Bh	Output CTRL	*RSVD*	*RSVD*	*RSVD*	SDOA_MUTE	SCLK_LVL[1]	SCLK_LVL[0]	*RSVD*	*RSVD*	08h	R/W
0Ch	SDOB CTRL	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	SDOB_EN	*RSVD*	*RSVD*	02h	R/W
0Dh	GBL CTRL1	*RSVD*	*RSVD*	*RSVD*	*RSVD*	FORCESDION	*RSVD*	OFFLOOP	PDALL	00h	R/W
0Eh	Interrupt CTRL	*RSVD*	*RSVD*	*RSVD*	*RSVD*	INT[3]	INT[2]	INT[1]	INT[0]	00h	R/W
0Fh	MicReg	*RSVD*	*RSVD*	MICDEV	MICDEV	MICDEV	MICDEV	MICDEV	MICDEV	00h	R/W
Reclocker Configuration											
10h	RSVD	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	30h	R/W
11h	RSVD	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	00h	R/W
12h	RCLK CTRL 0	*RSVD*	*RSVD*	*RSVD*	*RSVD*	RATE[1]	RATE[0]	BYPASS	PDOWN	00h	R/W
13h	RSVD	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	00h	R/W
14h	RCLK CTRL 1	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	BYPDIS	00h	R/W
15h	RSVD	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	00h	R/W
16h	RCLK BW CTRL	*RSVD*	BW[2]	BW[1]	BW[0]	*RSVD*	*RSVD*	*RSVD*	*RSVD*	20h	R/W
17h	RSVD	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	C0h	R/W
18h	RSVD	*RSVD*	*RSVD*	SDALG	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	C8h	R/W
19h	RSVD	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	03h	R/W

Table 5-1. M08035/M08045 Register Map (2 of 2)

Addr	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
Checksum for Memory Interface Configuration											
1Ah	CHECKSUM	CHKSUM	CHKSUM	CHKSUM	CHKSUM	CHKSUM	CHKSUM	CHKSUM	CHKSUM	55h	R/W
Status/Monitoring Registers											
80h	MASTER RESET	RST	RST	RST	RST	RST	RST	RST	RST	00h	R/W
81h	CHIP ID	ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]	0Bh	R
82h	CHIP REV	REV[7]	REV [6]	REV [5]	REV [4]	REV [3]	REV [2]	REV [1]	REV [0]	04h	R
83h	LOS STATUS 0	*RSVD*	*RSVD*	LOS1	*RSVD*	*RSVD*	LOS0	*RSVD*	*RSVD*	00h	R
84h	LOS STATUS 1	*RSVD*	*RSVD*	LOS3	*RSVD*	*RSVD*	*RSVD*	LOS2	*RSVD*	00h	R
85h	CLEAR ALARMS	*RSVD*	*RSVD*	RSVD	RSVD	*RSVD*	*RSVD*	SOFTRST	CLRALARMS	00h	R/W
87h	CHECKSUM RESULT	CHKRES	CHKRES	CHKRES	CHKRES	CHKRES	CHKRES	CHKRES	CHKRES	00h	R/W
88h	RCLK ALARMS	*RSVD*	*RSVD*	NOREF	REFLOL	*RSVD*	*RSVD*	*RSVD*	LOL	00h	R
89h	RCLK RATE DETECT	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	*RSVD*	RATE[1]	RATE[0]	00h	R
96h	LOL CONFIG	*RSVD*	MASK[0]	RSVD	RSVD	*RSVD*	*RSVD*	*RSVD*	*RSVD*	00h	R/W

NOTE:

1. *RSVD* are reserved bits that should never be changed from the default level.

5.1 Registers Description

5.1.1 Input/Output Configuration

Register Address: 00h
Default: 00h
Register Name: Input EQ Config 0
Description: Select input equalization level, input 0

Bit	Bit Description	Default	R/W
7:6	*Reserved*	00b	R/W
5:4	00b: SDI0, Input equalization disabled 01b: SDI0, Small input equalization level 10b: SDI0, Medium input equalization level 11b: SDI0, Large input equalization level	00b	R/W
3:2	*Reserved*	00b	R/W
1:0	*Reserved*	00b	R/W

Register Address: 01h
Default: 00h
Register Name: Input EQ Config 1
Description: Select input equalization level, input 1

Bit	Bit Description	Default	R/W
7:6	*Reserved*	00b	R/W
5:4	*Reserved*	00b	R/W
3:2	00b: SDI1, Input equalization disabled 01b: SDI1, Small input equalization level 10b: SDI1, Medium input equalization level 11b: SDI1, Large input equalization level	00b	R/W
1:0	*Reserved*	00b	R/W

Register Address: 02h
Default: 00h
Register Name: Input EQ Config 2
Description: Select input equalization level, input 2

Bit	Bit Description	Default	R/W
7:6	*Reserved*	00b	R/W
5:4	*Reserved*	00b	R/W
3:2	00b: SDI2, input equalization disabled 01b: SDI2, Small input equalization level 10b: SDI2, Medium input equalization level 11b: SDI2, Large input equalization level	00b	R/W
1:0	*Reserved*	00b	R/W

Register Address: 03h
Default: 00h
Register Name: Input EQ Config 3
Description: Select input equalization level, input 3

Bit	Bit Description	Default	R/W
7:6	*Reserved*	00b	R/W
5:4	*Reserved*	00b	R/W
3:2	00b: SDI3, input equalization disabled 01b: SDI3, Small input equalization level 10b: SDI3, Medium input equalization level 11b: SDI3, Large input equalization level	00b	R/W
1:0	*Reserved*	00b	R/W

Register Address: 04h
Default: 00h
Register Name: Input Polarity Flip 0
Description: Setting to a '1' inverts associated input, inputs 0 to 1

Bit	Bit Description	Default	R/W
7	*Reserved*	0b	R/W
6	*Reserved*	0b	R/W
5	0b: SDI1, Input normal 1b: SDI1, Input inverted	0b	R/W
4	*Reserved*	0b	R/W
3	*Reserved*	0b	R/W
2	0b: SDI0, Input normal 1b: SDI0, Input inverted	0b	R/W
1	*Reserved*	0b	R/W
0	*Reserved*	0b	R/W

Register Address: 05h
Default: 00h
Register Name: Input Polarity Flip 1
Description: Setting to a '1' inverts associated input, inputs 2 to 3

Bit	Bit Description	Default	R/W
7	*Reserved*	0b	R/W
6	*Reserved*	0b	R/W
5	0b: SDI3, Input normal 1b: SDI3, Input inverted	0b	R/W
4	*Reserved*	0b	R/W
3	*Reserved*	0b	R/W
2	*Reserved*	0b	R/W
1	0b: SDI2, Input normal 1b: SDI2, Input inverted	0b	R/W
0	*Reserved*	0b	R/W

Register Address: 06h
Default: 20h
Register Name: LOS Config/CLK EN
Description: Sets configuration for Loss of Signal alarm/Enables serial clock output buffer

Bit	Bit Description	Default	R/W
7:5	000b: 70 mV_{PPD} assert, 80 mV_{PPD} de-assert 001b: 80 mV_{PPD} assert, 90 mV_{PPD} de-assert [default] 010b: 90 mV_{PPD} assert, 100 mV_{PPD} de-assert 011b: 100 mV_{PPD} assert, 110 mV_{PPD} de-assert 100b: 110 mV_{PPD} assert, 120 mV_{PPD} de-assert 101b: 120 mV_{PPD} assert, 130 mV_{PPD} de-assert 110b: 130 mV_{PPD} assert, 140 mV_{PPD} de-assert 111b: LOS power down (globally applied for all input channels)	001b	R/W
4	0b: Normal LOS operation 1b: Force LOS to asserted	0b	R/W
3	0b: Squelch input upon LOS assertion 1b: Never squelch input upon LOS assertion	0b	R/W
2	0b: Squelch to logic high state 1b: Squelch to logic low state	0b	R/W
1	*Reserved*	0b	R/W
0	0b: Serial clock output is disabled 1b: Serial clock output is enabled (output level controlled by reg0Bh[3:2])	0b	R/W

Register Address: 07h
Default: 40h
Register Name: Input Mux Control
Description: Selects the input that is selected for the serial data output

Bit	Bit Description	Default	R/W
7:2	*Reserved*	010000b	R/W
1:0	00b: select input 0 to SDO 01b: select input 1 to SDO 10b: select input 2 to SDO 11b: select input 3 to SDO	00b	R/W

Register Address: 09h
Default: 88h
Register Name: SDOA CTRL
Description: Sets output level and De-emphasis for SDO0

Bit	Bit Description	Default	R/W
7:4	*Reserved*	1000b	R/W
3:2	00b: SDO powered down 01b: SDO output swing = 600 mV_{PPD} 10b: SDO output swing = 800 mV_{PPD} 11b: SDO output swing = 1200 mV_{PPD}	10b	R/W
1:0	00b: SDO De-emphasis off 01b: SDO De-emphasis = small 10b: SDO De-emphasis = medium 11b: SDO De-emphasis = large	00b	R/W

Register Address: 0Ah
Default: 00h
Register Name: Data Output De-Emphasis Control
Description: Sets output level and de-emphasis for SDOB.

Bit	Bit Description	Default	R/W
7:6	*Reserved*	000b	R/W
5:4	00b: SDOB de-emphasis off 01b: SDOB de-emphasis = small 10b: SDOB de-emphasis = medium 11b: SDOB de-emphasis = large	00b	R/W
3:0	*Reserved*	00b	R/W

Register Address: 0Bh
Default: 08h
Register Name: Output Control
Description: SDOA Mute and SDOB/SCLK swing control.

Bit	Bit Description	Default	R/W
7:5	*Reserved*	000b	R/W
4	0b: SDOA output in normal operation 1b: SDOA output muted	0b	R/W
3:2	00b: SDOB/SCLK output powered down 01b: SDOB/SCLK output swing = 600 mV_{PPD} 10b: SDOB/SCLK output swing = 800 mV_{PPD} 11b: SDOB/SCLK output swing = 1200 mV_{PPD}	10b	R/W
1:0	*Reserved*	00b	R/W

Register Address: 0Ch
Default: 02h
Register Name: SDOB Control
Description: Enable for second data output.

Bit	Bit Description	Default	R/W
7:3	*Reserved*	00000b	R/W
2	0b: SDOB output disabled 1b: SDOB output enabled	0b	R/W
1:0	*Reserved*	10b	R/W

Register Address: 0Dh
Default: 00h
Register Name: Global Control1
Description: Controls Global Configuration

Bit	Bit Description	Default	R/W
7:4	*Reserved*	0000b	R/W
3	0b: Inputs that are not used are powered down 1b: All inputs are forced on	0b	R/W
2	*Reserved*	0b	R/W
1	0b: Input offset correction loop On (all inputs) 1b: Input offset correction loop Off (all inputs)	0b	R/W
0	0b: Normal Operation 1b: Global Power Down	0b	R/W

Register Address: 0Eh
Default: 00h
Register Name: Interrupt Control
Description: Sets configuration for xALARM Output pin

Bit	Bit Description	Default	R/W
7:4	*Reserved*	00000b	R/W
3	0b: xALARM output is used in Interrupt mode 1b: Not supported	0b	R/W
2:0	000b: xALARM pulse width = 140 ns 001b: xALARM pulse width = 180 ns 010b: xALARM pulse width = 200 ns 011b: xALARM pulse width = 300 ns 100b: xALARM pulse width = 450 ns 101b: xALARM pulse width = 800 ns 110b: xALARM pulse width = 1.5 µs 111b: xALARM pulse width = 2.8 µs Measured with a 10 kΩ pull up resistor. Actual pulse width varies with the value of the pull-up resistor.	000b	R/W

Register Address: 0Fh
Default: 00h
Register Name: Memory Interface Configuration Control
Description: Defines the number of slave RCLK devices, controlled by quasi master/EEPROM

Bit	Bit Description	Default	R/W
7:6	*Reserved*	00b	R/W
5:0	000000b: no slave RCLKs 000001b: 1 slave RCLK 000010b: 2 slave RCLKs	000000b	R/W

5.1.2 Reclocker Configuration

Register Address: 12h
Default: 00h
Register Name: Reclocker Control 0
Description: Controls Reclocker

Bit	Bit Description	Default	R/W
7:4	*Reserved*	0000b	R/W
3:2	00b: ARD enabled 01b: SD data rate selected for reclocker 10b: HD data rate selected for reclocker 11b: 3G data rate selected for reclocker (M08045)	00b	R/W
1	0b: Normal operation (reclocker not bypassed) 1b: Reclocker bypassed	0b	R/W
0	0b: Normal operation 1b: Reclocker powered down	0b	R/W

Register Address: 14h
Default: 00h
Register Name: Reclocker Control 1
Description: Controls Reclocker

Bit	Bit Description	Default	R/W
7:1	*Reserved*	0000b	R/W
0	0b: Normal operation 1b: Reclocker auto-bypass feature disabled	0b	R/W

Register Address: 16h
Default: 20h
Register Name: Reclocker BW Control
Description: Controls bandwidth of Reclocker

Bit	Bit Description	Default	R/W
7	*Reserved*	0b	R/W
6:4	000b: Reserved (do not use) 001b: 0.5 x Nominal LBW 010b: 1 x Nominal LBW 011b: 4 x Nominal LBW 100b: 2 x Nominal LBW 101b: 3 x Nominal LBW 110b: 1.5 x Nominal LBW 111b: 0.875 x Nominal LBW	010b	R/W
3:0	*Reserved*	0000b	R/W

Register Address: 18h
Default: 00h
Register Name: SD/xHD Algorithm Control
Description: Controls SD/xHD output of Reclocker

Bit	Bit Description	Default	R/W
7:6	*Reserved*	00b	R/W
5	0b: SD/xHD output conforms to case 1, Table 4-11 1b SD/xHD output conforms to case 2, Table 4-11	0b	R/W
4:0	*Reserved*	00000b	R/W

5.1.3 Checksum for Memory Interface Configuration

Register Address: 1Ah
Default: 55h
Register Name: Checksum
Description: Checksum value to be added to sum of reg 00h to 19h contents

Bit	Bit Description	Default	R/W
7:0	Checksum value	01010101b	R/W

5.1.4 Status/Monitoring

Register Address: 80h
Default: 00h
Register Name: Reset
Description: Does Master Reset on Device

Bit	Bit Description	Default	R/W
7:0	00h: Normal Operation AAh: Master Reset	00000000b	R/W

Register Address: 81h
Default: 0Bh
Register Name: Chip ID
Description: Chip Identification Number

Bit	Bit Description	Default	R/W
7:0	M08035/M08045	N/A	R

Register Address: 82h
Default: 04h
Register Name: Chip Rev
Description: Chip Revision

Bit	Bit Description	Default	R/W
7:0	Chip revision	00000100b	R

Register Address: 83h
Default: 00h
Register Name: LOS Status 0
Description: Inputs 0-1, Set to a '1' when LOS asserted (single-event latched operation). Proper status is obtained after clearing all latched alarms by using Register 85h bit 0.

Bit	Bit Description	Default	R/W
7:6	*Reserved*	00b	R
5	0b: SDI1, Input present 1b: SDI1, LOS Asserted	0b	R
4:3	*Reserved*	00b	R
2	0b: SDI0, Input present 1b: SDI0, LOS Asserted	0b	R
1:0	*Reserved*	00b	R

Register Address: 84h
Default: 00h
Register Name: LOS Status 1
Description: Inputs 2-3, Set to a '1' when LOS asserted (single-event latched operation). Proper status is obtained after clearing all latched alarms by using Register 85h bit 0.

Bit	Bit Description	Default	R/W
7:6	*Reserved*	00b	R
5	0b: SDI3, Input present 1b: SDI3, LOS Asserted	0b	R
4:2	*Reserved*	000b	R
1	0b: SDI2, Input present 1b: SDI2, LOS Asserted	0b	R
0	*Reserved*	0b	R

Register Address: 85h
Default: 00h
Register Name: Alarm Clear
Description: Clears Latched Alarms. To properly clear all alarm bits, write "1" followed by a "0" to bit 0.

Bit	Bit Description	Default	R/W
7:2	*Reserved*	000000b	R/W
1	0b: Normal operation 1b: Soft reset for Reclocker (for master reset use reg 80h)	0b	R/W
0	0b: Normal operation 1b: Clears all alarm bits in registers 83h, 84h and 88h	0b	R/W

Register Address: 87h
Default: 00h
Register Name: Checksum result
Description: Shows the result of the checksum calculation

Bit	Bit Description	Default	R/W
7:0	Checksum result	00000000b	R/W

Register Address: 88h
Default: 00h
Register Name: Reclocker Status Register
Description: Reads status of the Reclocker

Bit	Bit Description	Default	R/W
7:6	*Reserved*	00b	R
5	0b: Reference clock is present 1b: Reference clock is not present	0b	R
4	0b: PLL locked 1b: PLL unlocked	0b	R
3:1	*Reserved*	XXXb	R
0	0b: Reclocker, locked 1b: Reclocker, un-locked	0b	R

Register Address: 89h
Default: 00h
Register Name: Reclocker Rate Detect
Description: Reads data rate for Reclocker

Bit	Bit Description	Default	R/W
7:2	*Reserved*	XXXXXXb	R
1:0	00b: Reclocker: un-locked 01b: Reclocker: SD data rate detected 10b: Reclocker: HD data rate detected 11b: Reclocker: 3G data rate detected (M08045)	00b	R

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