M02046-15

3.3/5V Limiting Amplifier for Applications from 100 Mbps to 1.25 Gbps

Rev V4

Applications

- 1.06 Gbps Fibre Channel
- 1.25 Gbps Ethernet
- 1.25 Gbps SDH/SONET
- SDH/SONET 155 Mbps Transceivers
- FTTx and Media Converters
- Fast Ethernet Receivers
- FDDI 125 Mbps Receivers
- ESCON Receivers

Features

- Pin compatible with the MC2046-2
- Operates with a 3.3V or 5V supply
- 2.8 mV typical input sensitivity at 1.25 Gbps
- Programmable input-signal level detect
- On-chip DC offset cancellation circuit
- CMOS and PECL Signal Detect output variants
- Output Jam Function
- Low power (< 200 mW (M02046-15) at 3.3V including PECL load)

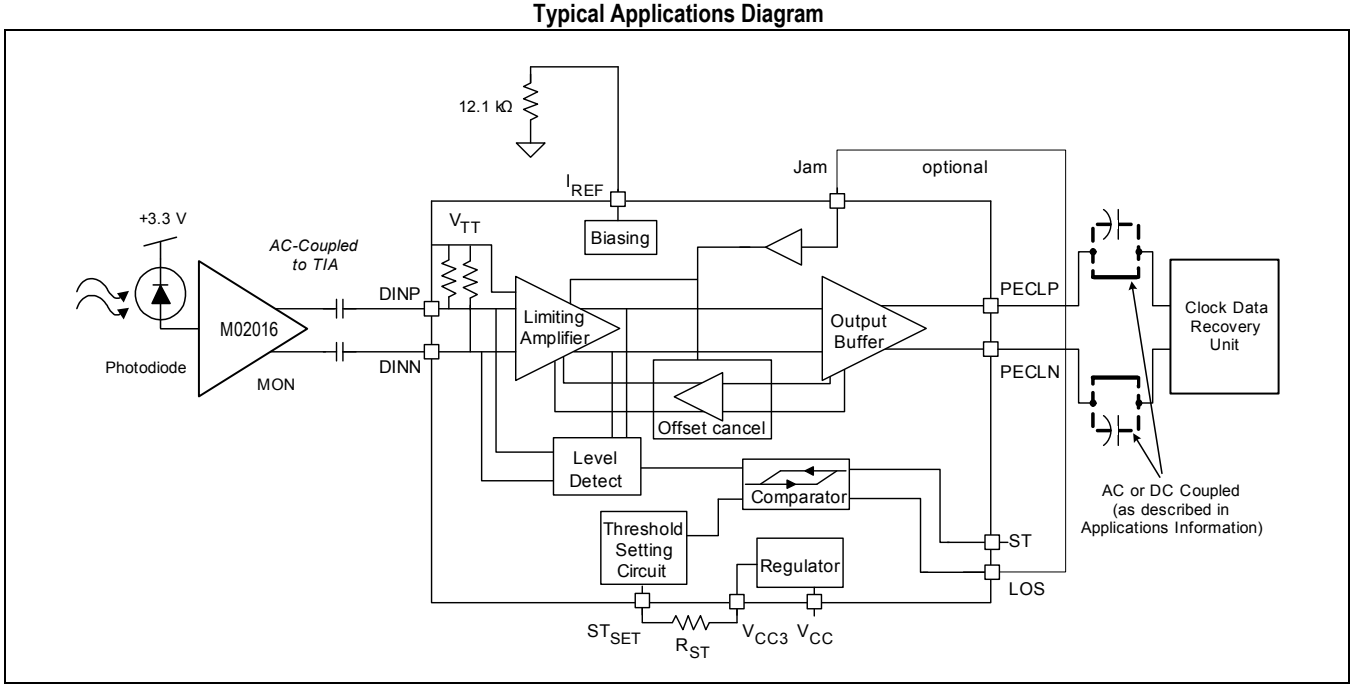
The M02046 is a highly integrated high-gain limiting amplifier that can be used with the same board layout and footprint as the MC2046-2 (refer to 02046-APP-004-X where X is the revision which will change if the application note is revised). Featuring PECL outputs, the M02046 is intended for use in applications from 100 Mbps to 1.25 Gbps. Full output swing is achieved even at minimum input sensitivity. The M02046 can operate with a 3.3V or 5V supply.

Included in the M02046 is a programmable signal-level detector, allowing the user to set thresholds at which the logic outputs are enabled. The signal detect function has typically 2 dB (optical) of hysteresis which prevents chatter at low input levels. A squelch function, which turns off the output when no signal is present, is provided by externally connecting the LOS Status output to the JAM input.

The M02046-15 has a CMOS Status output and the M02046-25 has a PECL Status output. Both versions have a CMOS LOS output.

Other available solutions: M02040-15 3.3/5V Limiting Amplifier for Applications to 2.125 Gbps (PECL outputs)
M02050-15 3.3/5V Limiting Amplifier for Applications to 2.5 Gbps (PECL outputs)
M02049-15 3.3/5V Limiting Amplifier for Applications to 4.3 Gbps (CML outputs)
M02043-15 3.3/5V Limiting Amplifier for Applications to 4.3 Gbps (CML outputs)

Typical Applications Diagram



Ordering Information

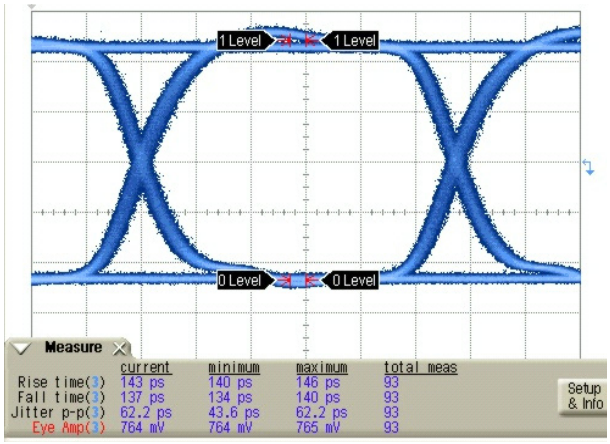
Part Number	Package	Operating Temperature
M02046-15*	CMOS Status Output (CMOS LOS Output) in QSOP16 package	–40 °C to 85 °C
M02046-25*	PECL Status Output (CMOS LOS Output) in QSOP16 package	–40 °C to 85 °C
M02046-15EVM	Evaluation board with M02046-15 (CMOS Status Output)	–40 °C to 85 °C
M02046-25EVM	Evaluation board with M02046-25 (PECL Status Output)	–40 °C to 85 °C

* The letter “G” designator after the part number indicates that the device is RoHS-compliant.

Revision History

Revision	Level	Date	Description
V4	Final	May 2015	Updated logos and page layout. No content changes.
G (V3)	Final	October 2007	Updated front page description to make it clear the part supports data rates down to 100 Mbps. Update Section 4.1.3 describing input ac-coupling capacitor selection.
F (V2)	Final	July 2005	Correct Jam connection in block diagram and typical applications figures. Correct I_{REF} figure (reference current generation).
E (V1)	Final	June 2005	In the DC specifications, update R_{IN}DIFF and added note 4. In the ac specifi-cations update V_{LOS} and DJ. Updated R_{ST} values and the typical LOS curve (Figure 4-2 - Figure 4-4). Added typical hysteresis curve (Figure 4-5).
D	Preliminary	April 2005	Corrected the ASIC revision number in this table. Update the Absolute Maximum specification for I(LOS) and I(ST_{CMOS}). Add the following DC specification: I_{OL_CMOS}.

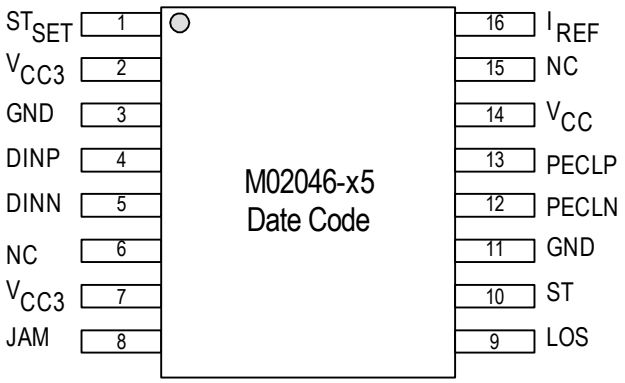
Typical Eye Diagram



10 mV_{PP} differential input
1.25 Gbps

160 mV/div
140 ps/div

Pin Configuration



Note: x is either a 1 or 2 as explained in the ordering information above

1.0 Product Specification

1.1 Absolute Maximum Ratings

These are the absolute maximum ratings at or beyond which the IC can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{CC}	Power supply voltage (V_{CC}-GND)	-0.5 to +5.75	V
T_{STG}	Storage temperature	-65 to +150	°C
PECLP, PECLN, ST_{PECL}	PECL Output pins voltage	V_{CC} - 2 to V_{CC} + 0.4	V
I(PECLP), I(PECLN), I(ST_{PECL})	PECL Output pins maximum continuous current (delivered to load)	30	mA
|DINP - DINN|	Data input pins differential voltage	0.80	V
DINP, DINN	Data input pins voltage meeting |DINP - DINN| requirement	GND to V_{CC3} + 0.4	V
ST_{SET}	Signal detect threshold setting pin voltage	GND to V_{CC3} + 0.4	V
JAM	Output enable pin voltage	GND to V_{CC} + 0.4	V
ST_{CMOS}, LOS	CMOS Status Output pins voltage	GND to V_{CC} + 0.4	V
I_{REF}	Current into Reference input	+0 to -120	µA
I(LOS), I(ST_{CMOS})	Current into CMOS Status Output pins	+3000 to -100	µA

1.2 Recommended Operating Conditions

Table 1-2. Recommended Operating Conditions

Parameter	Rating	Units
Power supply: (V_{CC}-GND) (apply no potential to V_{CC3}) or (V_{CC3}-GND) (connect V_{CC} to same potential as V_{CC3})	+5V ± 7.5% or +3.3V ± 7.5%	V
Junction temperature	-40 to +110	°C
Operating ambient	-40 to +85	°C

1.3 DC Characteristics

V_{CC} = +3.3V ± 7.5% or +5V ± 7.5%, T_A = -40°C to +85°C, unless otherwise noted.
Typical specifications are for V_{CC} = 3.3V, T_A = 25°C, unless otherwise noted.

Table 1-3. DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Supply Current	PECL outputs un-loaded	–	26	38	mA
$V_{OUTHpecl}$	PECL Output High Voltage (1) (PECLP, PECLN)	Single ended; 50Ω load to V_{CC} - 2V	V_{CC}-1.025	V_{CC}-0.952	V_{CC}-0.88	V
$V_{OUTLpecl}$	PECL Output Low Voltage (1) (PECLP, PECLN)	Single ended; 50Ω load to V_{CC} - 2V	V_{CC}-1.81	V_{CC}-1.71	V_{CC}-1.62	V
R_{IN}DIFF	Differential Input Resistance	Measured between DINP and DINN	90	110	130	Ω
V_{OH_CMOS}	CMOS ST (2), LOS (2, 3) Output High Voltage	External 4.7-10 kΩ pull up to V_{CC}	2.75	V_{CC}	–	V
V_{OL_CMOS}	CMOS ST (2), LOS (2, 3) Output Low Voltage	External 4.7-10 kΩ pull up to V_{CC}	0	–	0.4	V
I_{OL_CMOS}	CMOS ST (2), LOS (2, 3) Output Low Current (into device)	V_{OL} determined by external pull up to V_{CC}	–	–	2.0	mA
V_{OH_PECL}	PECL ST Output High Voltage (1, 3, 4)	ST terminated 50Ω to V_{CC} - 2V	V_{CC}-1.115	V_{CC}-1.042	V_{CC}-0.97	V
V_{OL_PECL}	PECL ST Output Low Voltage (1, 3, 4)	ST terminated 50Ω to V_{CC} - 2V	V_{CC}-1.88	V_{CC}-1.78	V_{CC}-1.69	V
V_{IH}	JAM Input High Voltage		2.7	–	V_{CC}	V
V_{IL}	JAM Input Low Voltage		–	–	0.8	V

Notes:

1. Limits apply between 0°C to +85°C. Below 0°C the minimum decreases by up to 40 mV.
2. M02046-15
3. M02046-25
4. When ST is terminated with a 510Ω resistor to ground, the ST output voltages are approximately the same as for $V_{OUTHpecl}$ and $V_{OUTLpecl}$

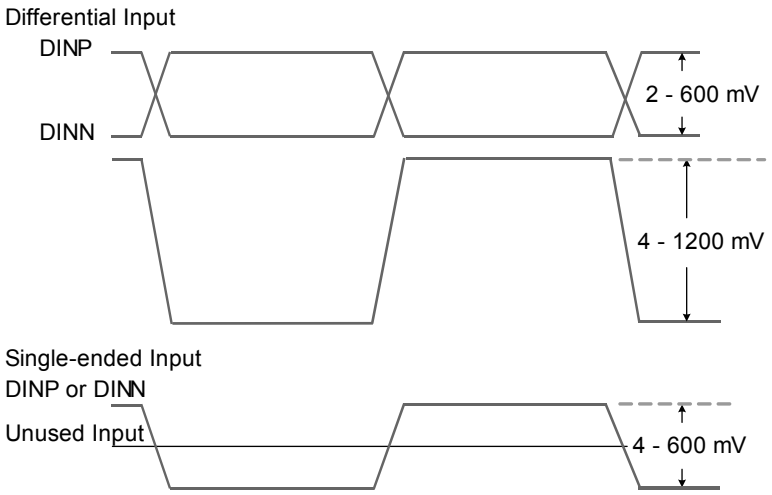
1.4 AC Characteristics

V_{CC} = +3.3V ± 7.5% or +5V ± 7.5%, T_A = -40°C to +85°C, input bit rate = 1.25 Gbps 2^{23}-1 PRBS unless otherwise noted. Typical specifications are for V_{CC} = 3.3V, T_A = 25°C, unless otherwise noted.

Table 1-4. AC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{IN(MIN)}$	Differential Input Sensitivity	1.25 Gbps, BER < 10^{-12}	–	2.8	5	mV
$V_{I(MAX)}$	Input Overload	BER < 10^{-12}, differential input 1.25 Gbps	1200	–	–	mV
		BER < 10^{-12}, single-ended input, 1.25 Gbps	600	–	–	mV
v_n	RMS Input Referred Noise		–	200	–	μV_{RMS}
V_{LOS}	LOS Programmable Range	Differential inputs	5	–	55	mV
HYS	Signal Detect/LOS Hysteresis	(electrical); across LOS programmable range	2	3.5	5.5	dB
BW_{LF}	Small-Signal –3dB Low Frequency Cutoff	Excluding AC coupling capacitors	–	25	–	kHz
DJ	Deterministic Jitter (includes DCD)	K28.5 pattern at 1.25 Gbps, 10 mVPP input	–	18	70	ps
RJ	Random Jitter	10 mV_{PP} input	–	5	–	ps_{RMS}
t_r / t_f	Data Output Rise and Fall Times	20% to 80%; outputs terminated into 50Ω; 10 mV_{PP} input	–	150	230	ps
T_{LOS_ON}	Time from LOS state until LOS output is asserted	LOS assert time after 1 V_{PP} input signal is turned off; signal detect level set to 10 mV	2.3	–	80	µs
T_{LOS_OFF}	Time from non-LOS state until LOS is deasserted	LOS deassert time after input crosses signal detect level; signal detect set to 10 mV with applied input signal of 20 mV_{PP}	2.3	–	80	µs

Figure 1-1. Data Input Requirements

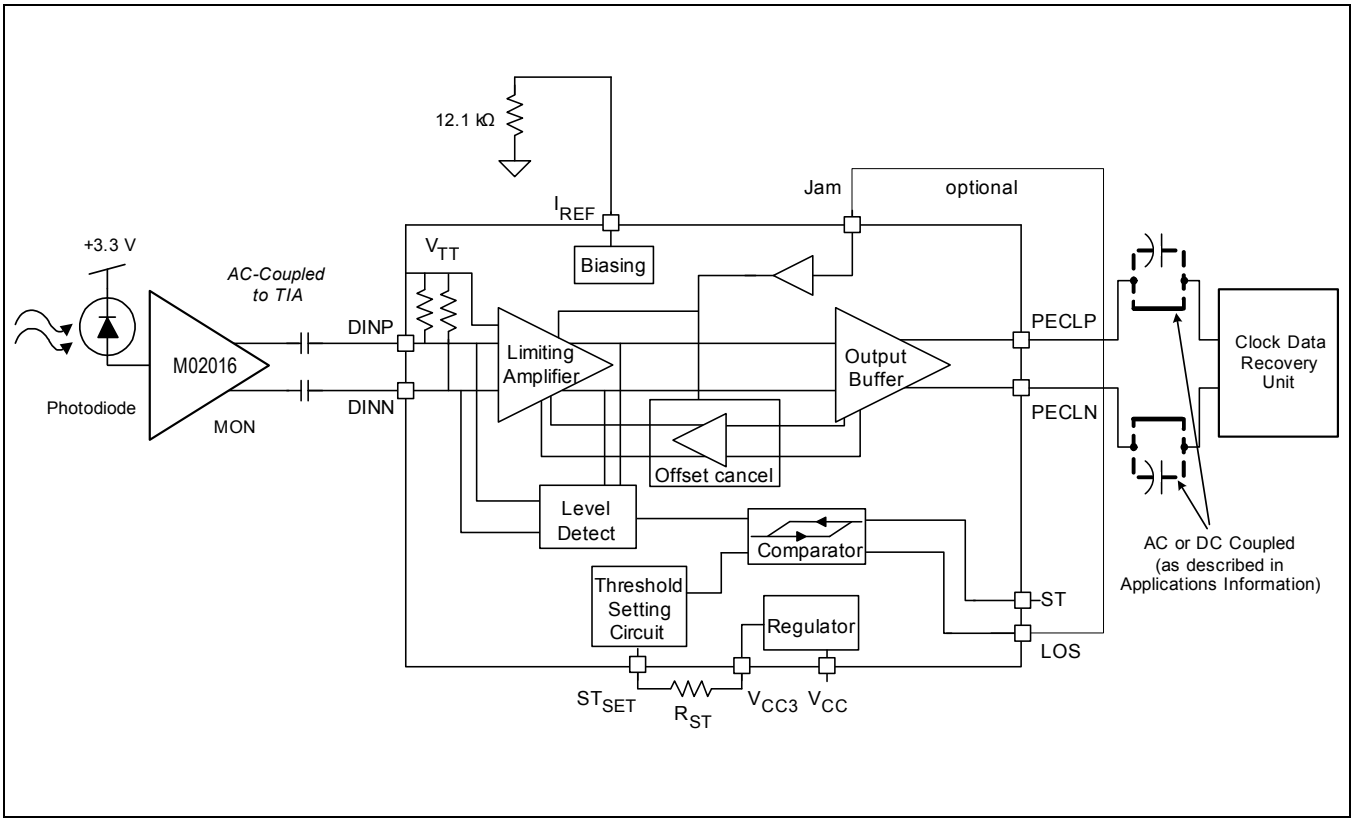


NOTE:

For single-ended input connections.
When connecting to the used input with AC-coupling, the unused input should be AC-coupled through 50Ω to the supply voltage of the TIA;

When connecting to the used input with DC-coupling, the unused input should be DC-coupled through 50Ω to a voltage equal to the common mode level of the used input.

Figure 1-2. Typical Applications Circuit



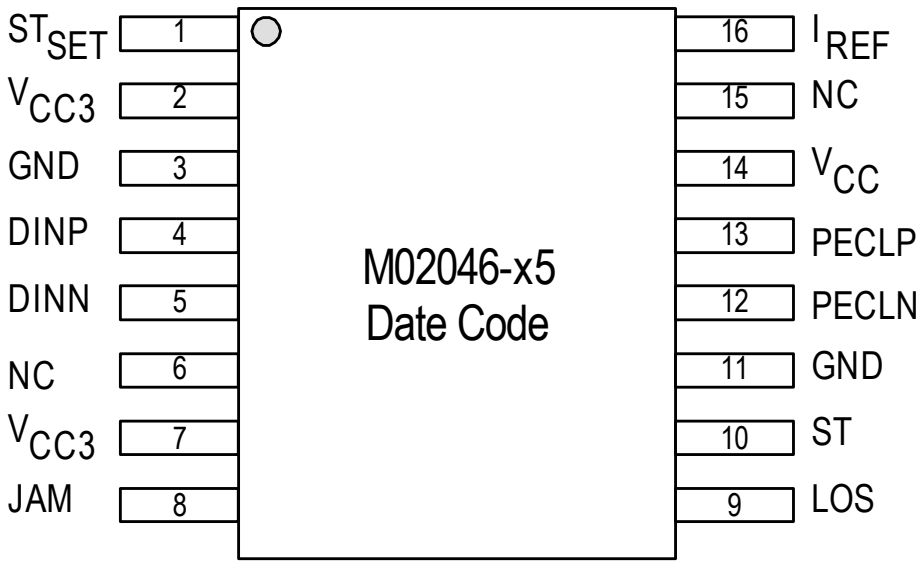
NOTE: AC-coupled inputs shown.

2.0 Pin Definitions

Table 2-1. Pin Descriptions

QSOP Pin#	Name	Function
1	ST_{SET}	Loss of signal threshold setting input. Connect a 1% resistor between this pin and V_{CC3} (pin 2) to set loss of signal threshold.
2	V_{CC3}	Power supply input for 3.3V applications or the output of the internally regulated 3.3V voltage when V_{CC} = 5V. Connect directly to supply for 3.3V applications (internal regulator not in use). Do not connect to power supply if V_{CC} = 5V.
3	GND	Ground.
4	DINP	Non-inverting data input. Internally terminated with 50Ω to V_{TT} (see Figure 3-2).
5	DINN	Inverting data input. Internally terminated with 50Ω to V_{TT} (see Figure 3-2).
6	NC	No Connect. Leave Floating.
7	V_{CC3}	Power supply input for 3.3V applications or the output of the internally regulated 3.3V voltage when V_{CC} = 5V. Connect directly to supply for 3.3V applications (internal regulator not in use). Do not connect to power supply if V_{CC} = 5V.
8	JAM	Output disable. When high, data outputs are disabled (with non-inverting output held high and inverting output held low). Connect to LOS output to disable outputs with loss of signal. Outputs are enabled when JAM is low or floating. Internal 150 kΩ resistor to ground.
9	LOS	Loss of signal output. Goes high when input signal falls below threshold set by ST_{SET}. This output is an open collector TTL with internal 80 kΩ pull-up resistor to V_{CC}. Leave floating if not used.
10	ST	Signal detect output. Goes high when input signal amplitude is above threshold set by ST_{SET}. In M02046-15, this output is an open collector TTL with internal 80 kΩ pull-up resistor to V_{CC}; In M02046-25, this output is PECL. Leave floating if not used.
11	GND	Ground.
12	PECLN	Inverting data output (PECL).
13	PECLP	Non-inverting data output (PECL).
14	V_{CC}	Power supply. Connect to either +5V or +3.3V.
15	NC	No Connect. Leave Floating.
16	I_{REF}	Internal reference current for the LOS threshold. Must be connected to ground through a 12.1 kΩ 1% resistor.

Figure 2-1. M02046-x5 Pinout



Note: x is either a 1 or 2 as explained in the ordering information

3.0 Functional Description

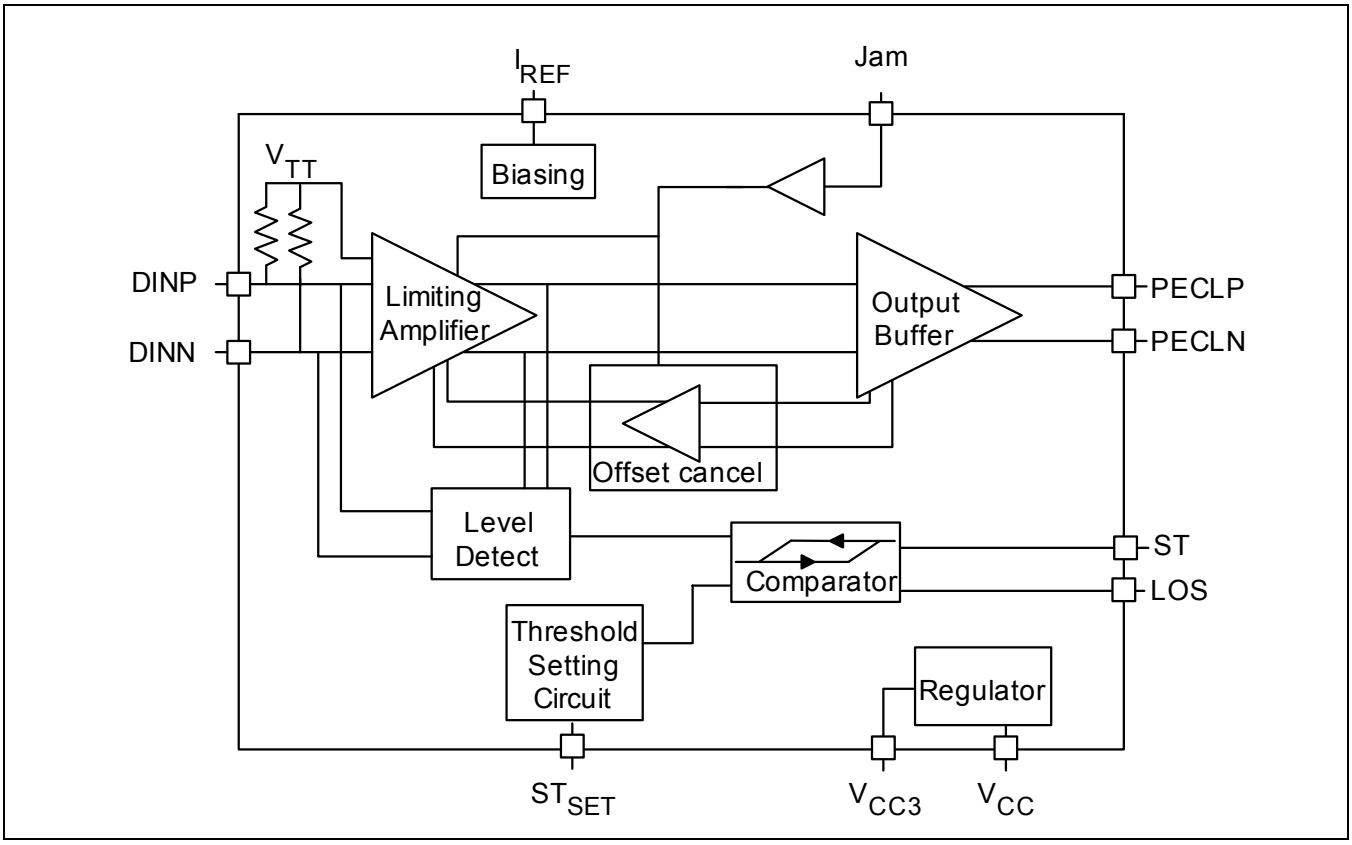
3.1 Overview

The M02046 is a highly integrated high-gain limiting amplifier that can be used with the same board layout and footprint as the MC2046-2. Featuring PECL outputs, the M02046 is intended for use in applications from 100 Mbps to 1.25 Gbps. Full output swing is achieved even at minimum input sensitivity. The M02046 can operate with a 3.3V or 5V supply.

Included in the M02046 is a programmable signal-level detector, allowing the user to set thresholds at which the logic outputs are enabled. The signal detect function has typically 2 dB (optical) of hysteresis which prevents chatter at low input levels. A squelch function, which turns off the output when no signal is present, is provided by externally connecting the LOS Status output to the JAM input.

The M02046-15 has a CMOS Status output and the M02046-25 has a PECL Status output. Both versions have a CMOS LOS output.

Figure 3-1. Block Diagram Example



3.2 Features

- Pin compatible with the MC2046-2
- Operates with a 3.3V or 5V supply
- 2.8 mV typical input sensitivity at 1.25 Gbps
- Programmable input-signal level detect
- On-chip DC offset cancellation circuit
- CMOS and PECL Signal Detect output variants
- Output Jam Function
- Low power (< 200 mW (M02046-15) including PECL outputs)

3.3 General Description

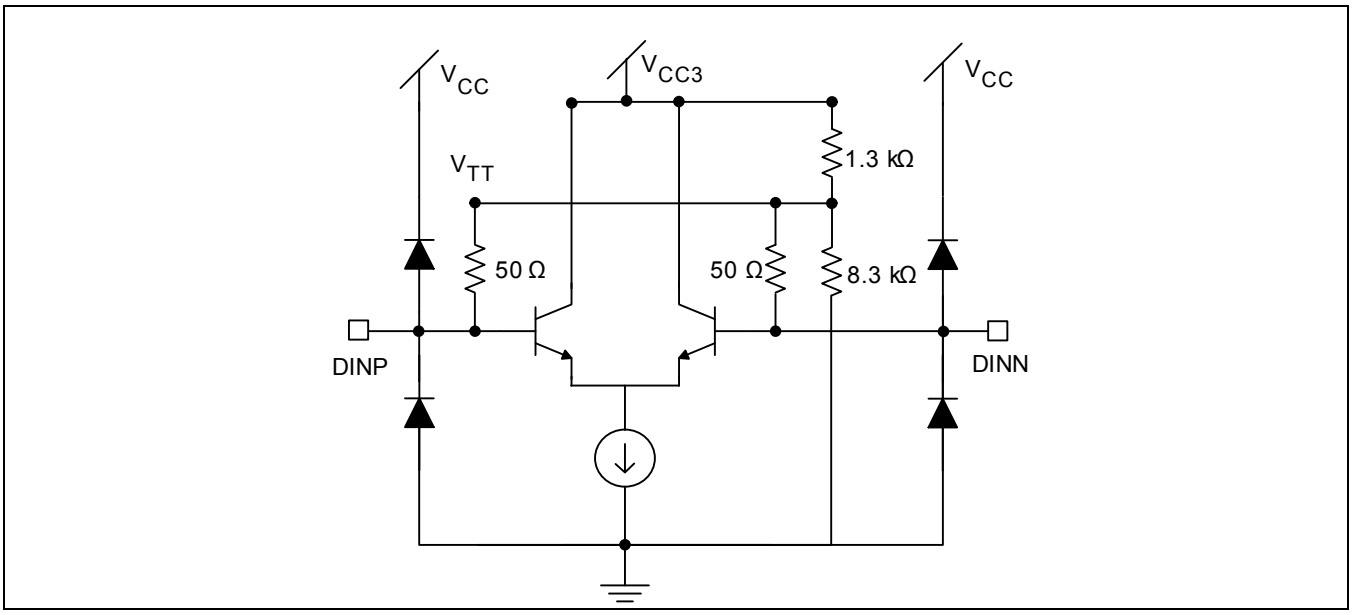
The M02046 is a high-gain limiting amplifier for applications up to 1.25 Gbps, and incorporates a limiting amplifier, an input signal level detection circuit and also a fully integrated DC-offset cancellation loop that does not require any external components. The M02046 features a PECL high-speed data outputs.

The M02046 provides the user with the flexibility to set the signal detect threshold and features either a CMOS status output (M02046-15) or a PECL status output (M02046-25). Optional output buffer disable (squelch/jam) can be implemented using the JAM input.

3.3.1 Inputs

The data inputs are internally connected to V_{TT} via 50Ω resistors, and generally need to be AC coupled. Referring to Figure 3-2, the nominal V_{TT} voltage is 2.85V because of the internal resistor divider to V_{CC3}, which means this is the DC potential on the data inputs. See the applications information section for further details on choosing the AC-coupling capacitor.

Figure 3-2. CML Data Inputs



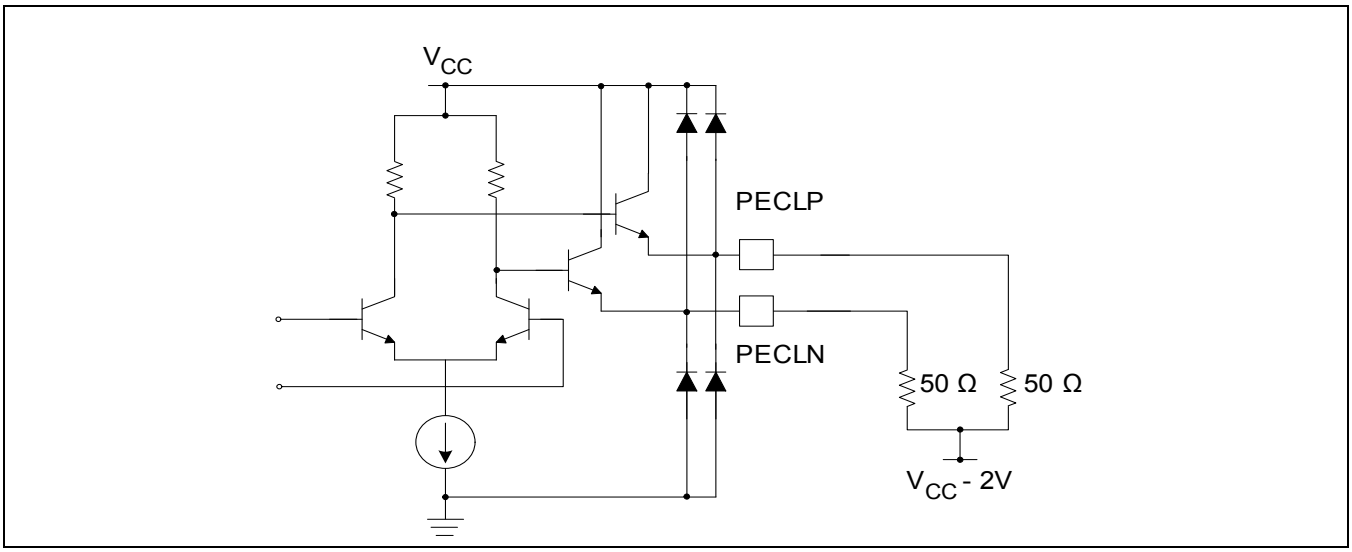
3.3.2 DC Offset Compensation

The M02046 contain an internal DC autozero circuit that can remove the effect of DC offsets without using external components. This circuit is configured such that the feedback is effective only at frequencies well below the lowest frequency of interest. The low frequency cut off is typically 25 kHz.

3.3.3 Data Outputs

The M02046 features 100k/300k PECL compliant outputs as shown in Figure 3-3. The outputs may be terminated using any standard AC or DC-coupling PECL termination technique. AC-coupling is used in applications where the average DC content of the data is zero e.g. SONET. The advantage of this approach is lower power consumption, no susceptibility to DC drive and compatibility with non-PECL interfaces.

Figure 3-3. PECL Data Outputs



3.3.4 Signal Detect (ST) and Loss of Signal (LOS)

The M02046 features input signal level detection over an extended range. Using an external resistor, R_{ST}, between pin ST_{SET} and V_{CC3} (Figure 3-6) the user can program the input signal threshold. The signal detect status is indicated on the both the Signal Detect (ST) and LOS output pins. The Status output is either CMOS (M02046-15) or PECL (M02046-25). The PECL version is shown in Figure 3-4 while Figure 3-5 shows the ST output for the CMOS version of the device (and the LOS output for both versions of the device).

The ST (LOS) signal is active (not asserted) when the signal is above the threshold value. The signal detection circuitry has the equivalent of 3.5 dB (typical) electrical hysteresis.

Figure 3-4. PECL ST Output (M02046-25)

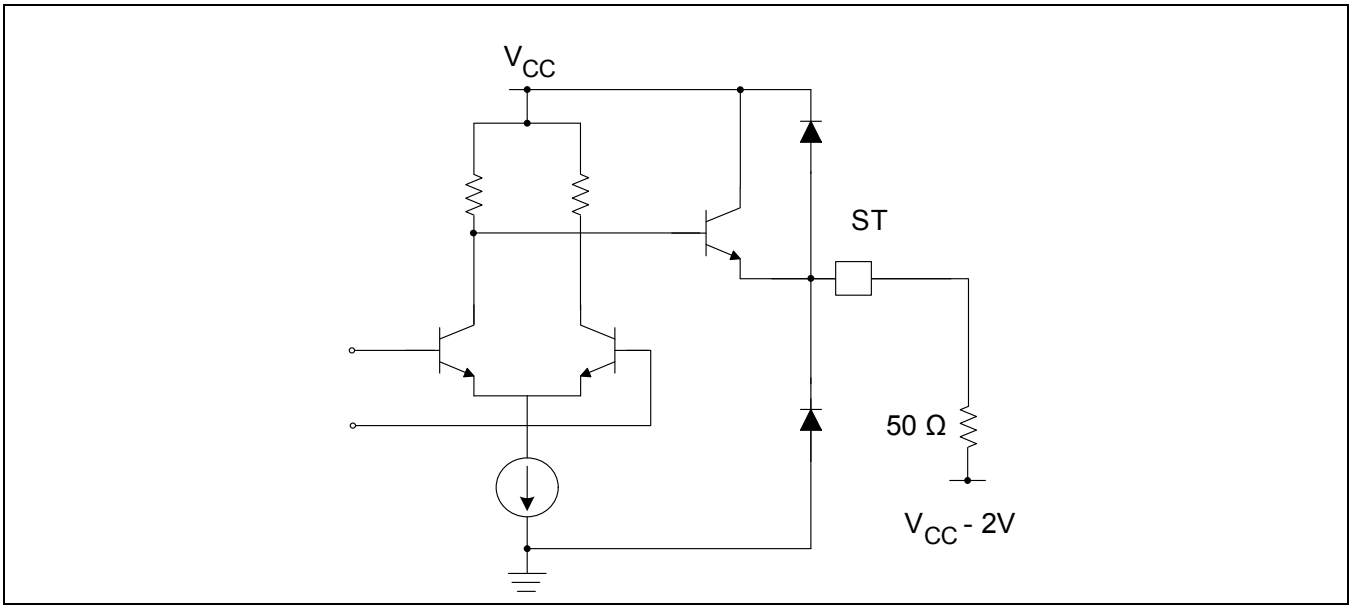
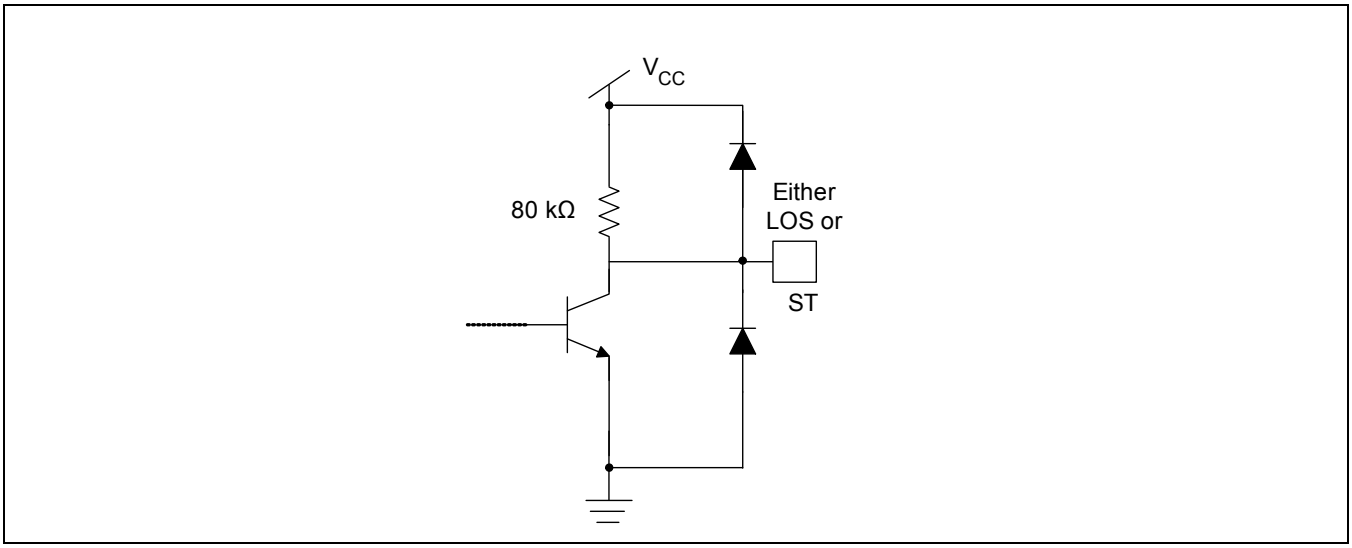


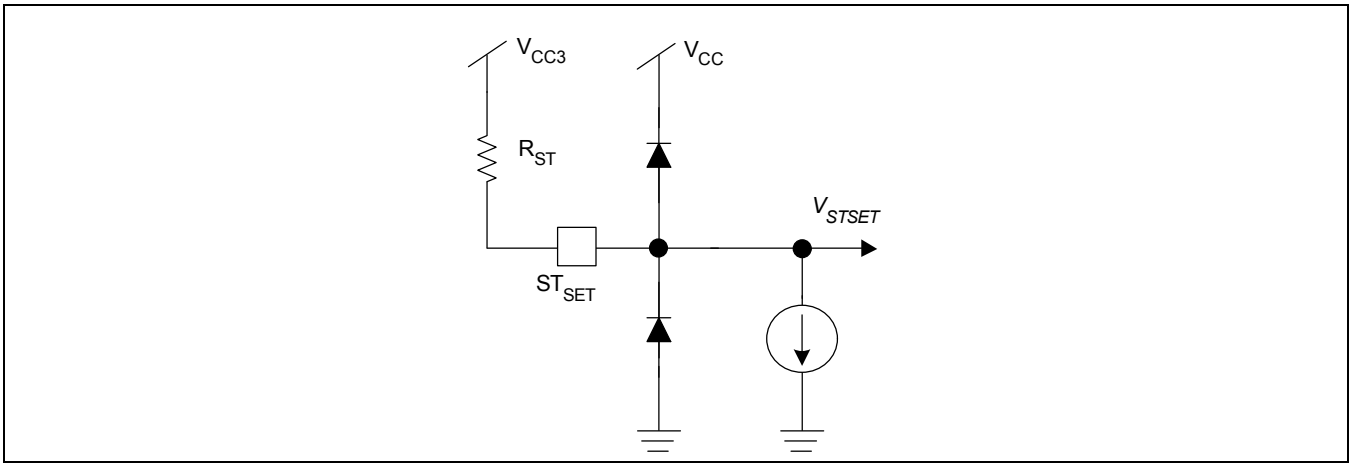
Figure 3-5. CMOS ST (M02046-15) and LOS (M02046-15 and M02046-25) Output



R_{ST} establishes a threshold voltage at the ST_{SET} pin as shown in Figure 3-6. Internally, the input signal level is monitored by the Level Detector which creates a DC voltage proportional to the input signal peak to peak value. The voltage at ST_{SET} is internally compared to the signal level from the Level Detector. When the Level Detect voltage is less than $V_{(STSET)}$, LOS is asserted and will stay asserted until the input signal level increases by a predefined amount of hysteresis. When the input level increases by more than this hysteresis above $V_{(STSET)}$, LOS is deasserted. See the applications information section for the selection of R_{ST}.

Note that ST_{SET} can be left open if the loss of signal detector function is not required. In this case LOS would be low.

Figure 3-6. STset Input

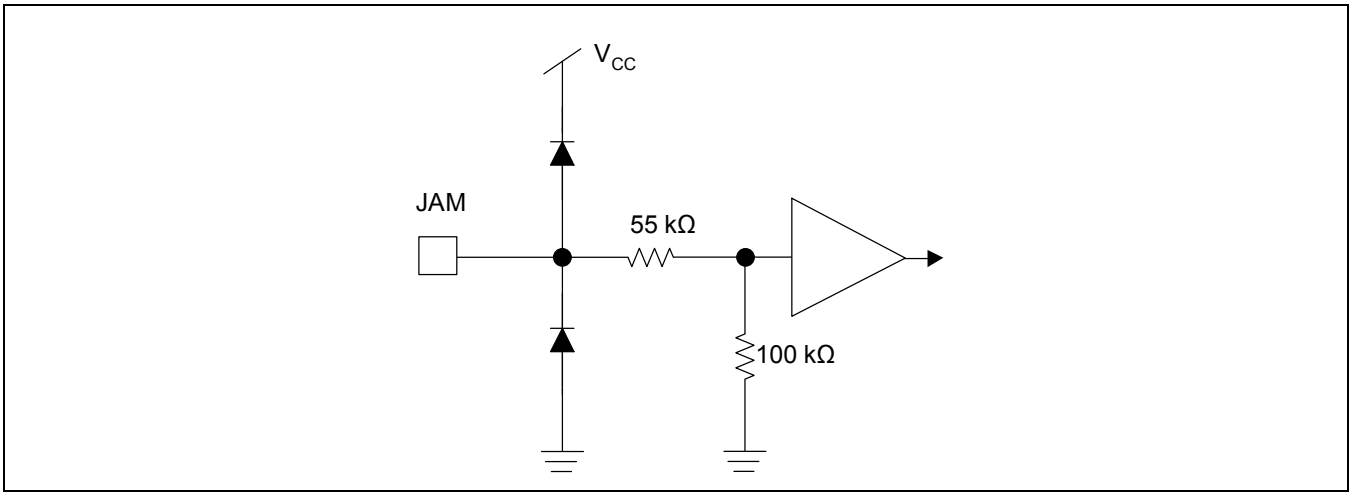


3.3.5 JAM Function

When asserted, the active high power down (JAM) pin forces the outputs to a logic “one” state. This ensures that no data is propagated through the system. The loss of signal detection circuit can be used to automatically force the data outputs to a high state when the input signal falls below the threshold. The function is normally used to allow data to propagate only when the signal is above the user's bit-error-rate requirement. It therefore inhibits the data outputs toggling due to noise when there is no signal present (“squelch”).

In order to implement this function, LOS should be connected to the JAM pin shown in Figure 3-7, thus forcing the data outputs to a logic “one” state when the signal falls below the threshold.

Figure 3-7. JAM Input



3.3.6 Voltage Regulation

The M02046 contain an on-chip voltage regulator to allow both 5V and 3.3V operation. When used at 5V, the on-chip regulator is enabled and the digital inputs and outputs are compatible with TTL 5V logic levels.

4.0 Applications Information

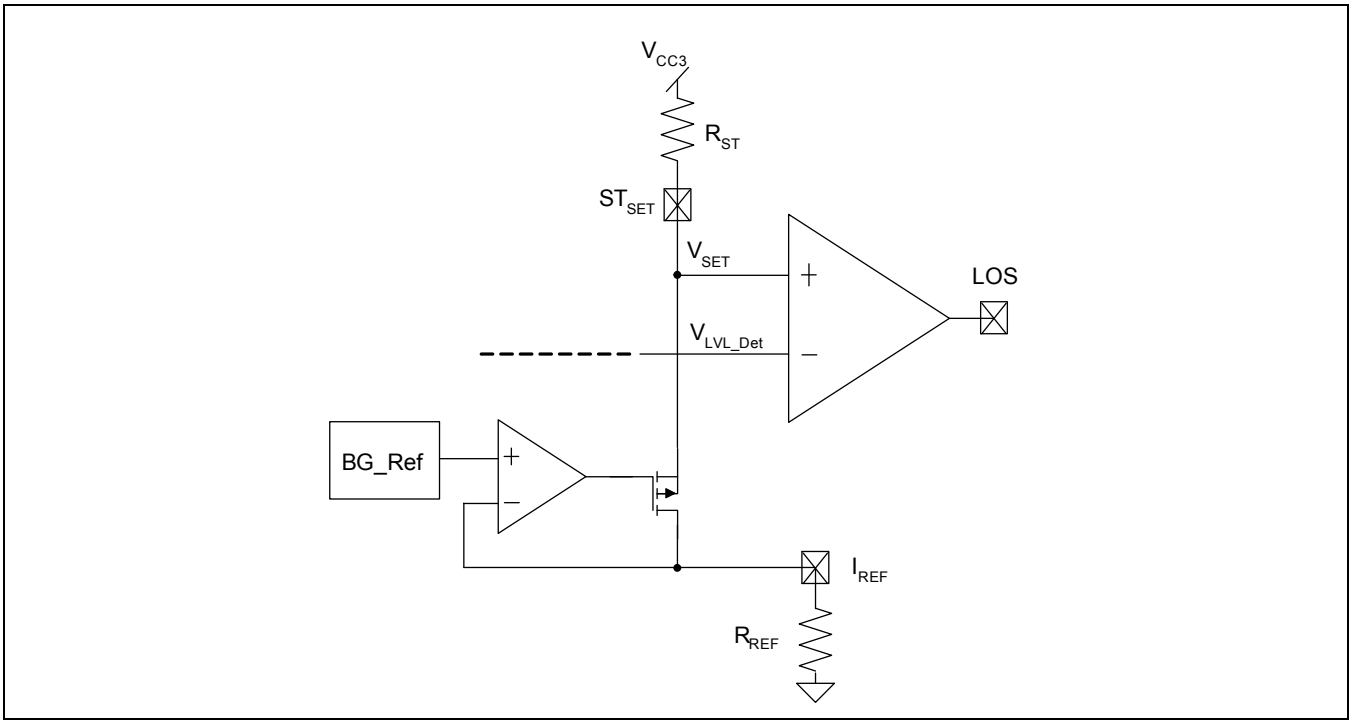
4.1 Applications

- 1.06 Gbps Fibre Channel
- 1.25 Gbps Ethernet
- 1.25 Gbps SDH/SONET
- SDH/SONET 155 Mbps Transceivers
- FTTx and Media Converters
- Fast Ethernet Receivers
- FDDI 125 Mbps Receivers
- ESCON Receivers

4.1.1 Reference Current Generation

The M02046 contain an accurate on-chip bias circuit that requires an external 12.1 kΩ 1% resistor, R_{REF}, from pin I_{REF} to ground to set the LOS threshold voltage at ST_{SET} precisely.

Figure 4-1. Reference Current Generation



4.1.2 Connecting V_{CC} and V_{CC3}

For 5V operation, the V_{CC} pin is connected to an appropriate 5V ± 7.5% supply. No potential should be applied to the V_{CC3} pin. The only connection to V_{CC3} should be R_{ST} as shown in Figure 3-6.

When V_{CC} = 5V all logic outputs and the data outputs are 5V compatible. For low power operation, V_{CC} and V_{CC3} should be connected to an appropriate 3.3V ± 7.5% supply. In this case all I/Os are 3.3V compatible.

4.1.3 Choosing an Input AC-Coupling Capacitor

When AC-coupling the input the coupling capacitor should be of sufficient value to pass the lowest frequencies of interest, bearing in mind the number of consecutive identical bits, and the input resistance of the part. For SONET data, a good rule of thumb is to chose a coupling capacitor that has a cut-off frequency less than 1/10,000 of the input data rate. For example, for 1.25 Gbps data, the coupling capacitor should be chosen as:

$f_{CUTOFF} \leq (1.25x10^9 / 10x10^3) = 125$ kHz

The -3 dB cutoff frequency of the low pass filter at the input is found as (assuming that the TIA output is also 50Ω single-ended):

$f_{3dB} = 1/ (2 * \pi * 100\Omega * C_{AC})$

so solving for C where $f_{3dB} = f_{CUTOFF}$

$C_{AC} = 1/ (2 * \pi * 100\Omega * f_{CUTOFF})$ EQ.1

and in this case the minimum capacitor is 12.8 nF.

For Ethernet or Fibre Channel, there are less consecutive bits in the data, and the recommended cut-off frequency is 1/(1,000) of the input data rate. This results in a minimum capacitor of 1.6 nF (or greater) for 1 Gbps Ethernet.

Multirate applications down to 100 Mbps

In this case, the input coupling capacitor needs to be large enough to pass 15 kHz ($155x10^6$/10,000, a condition more stringent than 100 Mbps Ethernet) which results in a capacitor value of 100 nF. However, because this low pass frequency is close to the 25 kHz low pass frequency of the internal DC servo loop, it is preferable to use a larger input coupling capacitor such as 200 nF which provides an input cutoff frequency of 7.5 kHz. This separates the two poles sufficiently to allow them to be considered independent.

In all cases, a high quality coupling capacitor should be used as to pass the high frequency content of the input data stream. It is also important that the ROSA bandwidth is sufficiently low and high enough to also support the required data rate, for it's lower and upper cutoff bandwidth impact the receiver bandwidth as much as does the limiting amp's lower and upper cutoff bandwidth.

4.1.4 Setting the Signal Detect Level

Using Figure 4-2, the value for R_{ST} is chosen to set the LOS threshold at the desired value. The resulting hysteresis is also shown in Figure 4-2.

From Figure 4-2, it is apparent that small variations in R_{ST} cause significant variation in the LOS threshold level, particularly for low input signal levels. This is because of the logarithmic relationship between the internal level detect voltage and the input signal level. It is recommended that a 1% resistor be used for R_{ST} and that allowance is provided for LOS variation, particularly when the LOS threshold is near the sensitivity limit of the M02046.

Example R_{ST} resistor values are given in Table 4-1.

Table 4-1. Typical LOS Assert and De-assert Levels for Various 1% R_{ST} Resistor Values

R_{ST} (kΩ)	VIN (mV pp) differential	
	LOS Assert	LOS De-Assert
7.50	4.9	7.8
6.81	11.7	17.0
6.19	23.2	33.4
5.49	55.0	77.3

Figure 4-2. Typical Loss of Signal Characteristic (Full Input Signal Range)

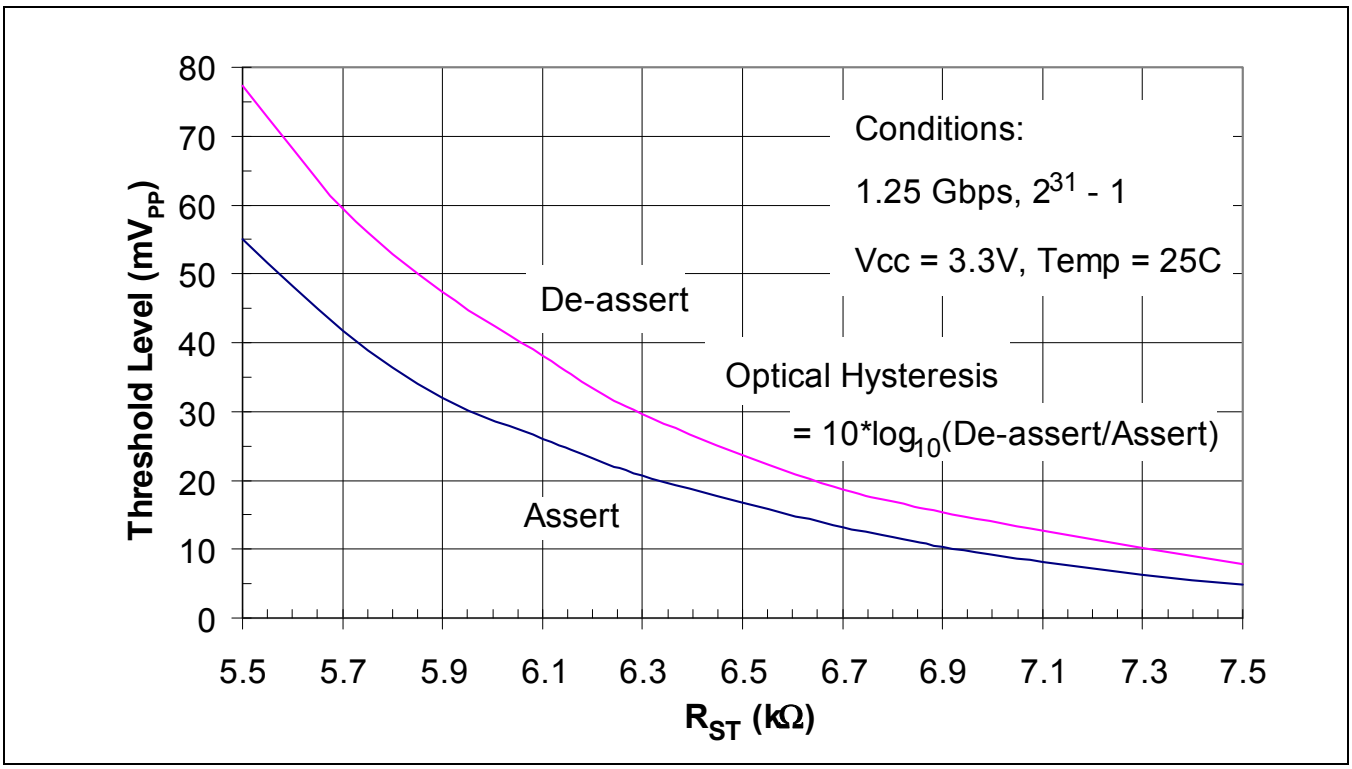


Figure 4-3. Typical Loss of Signal Characteristic (Low Input Signal Range)

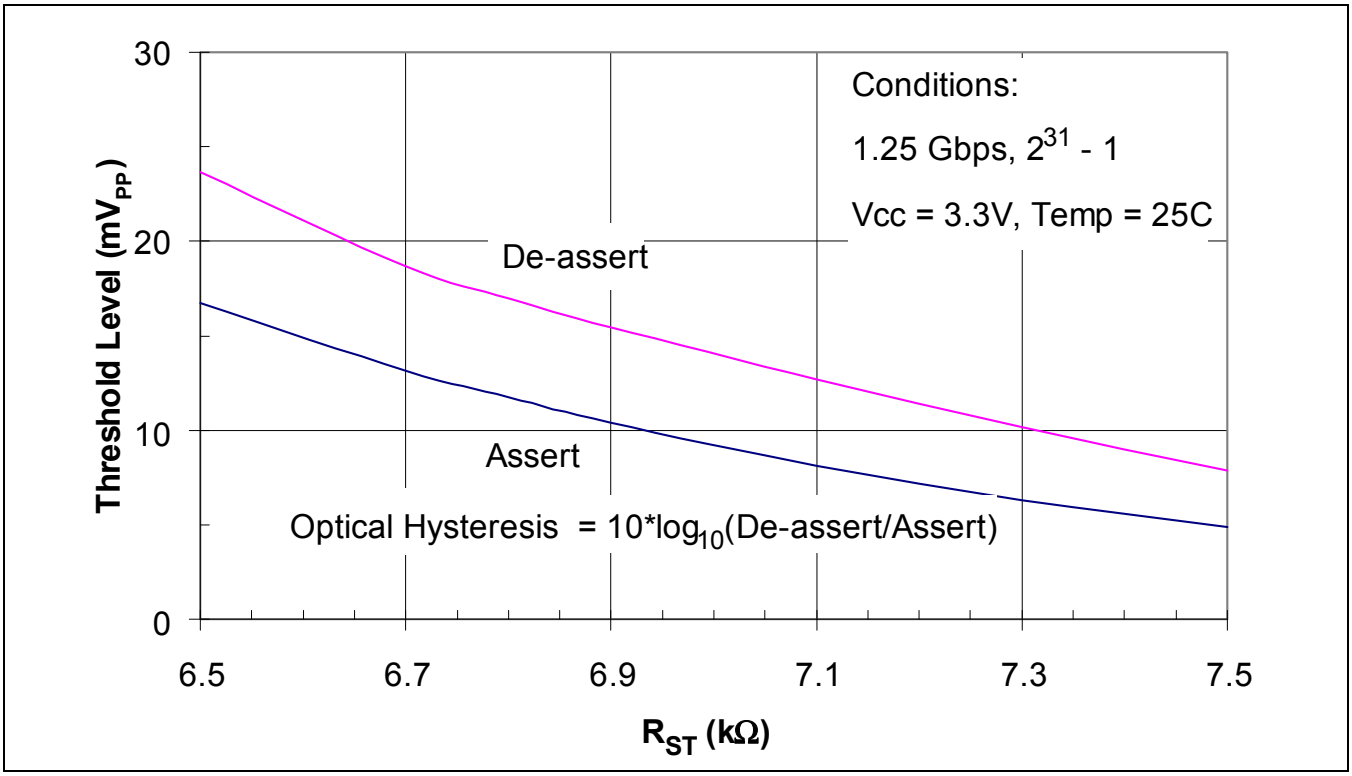


Figure 4-4. Typical Loss of Signal Characteristic (High Input Signal Range)

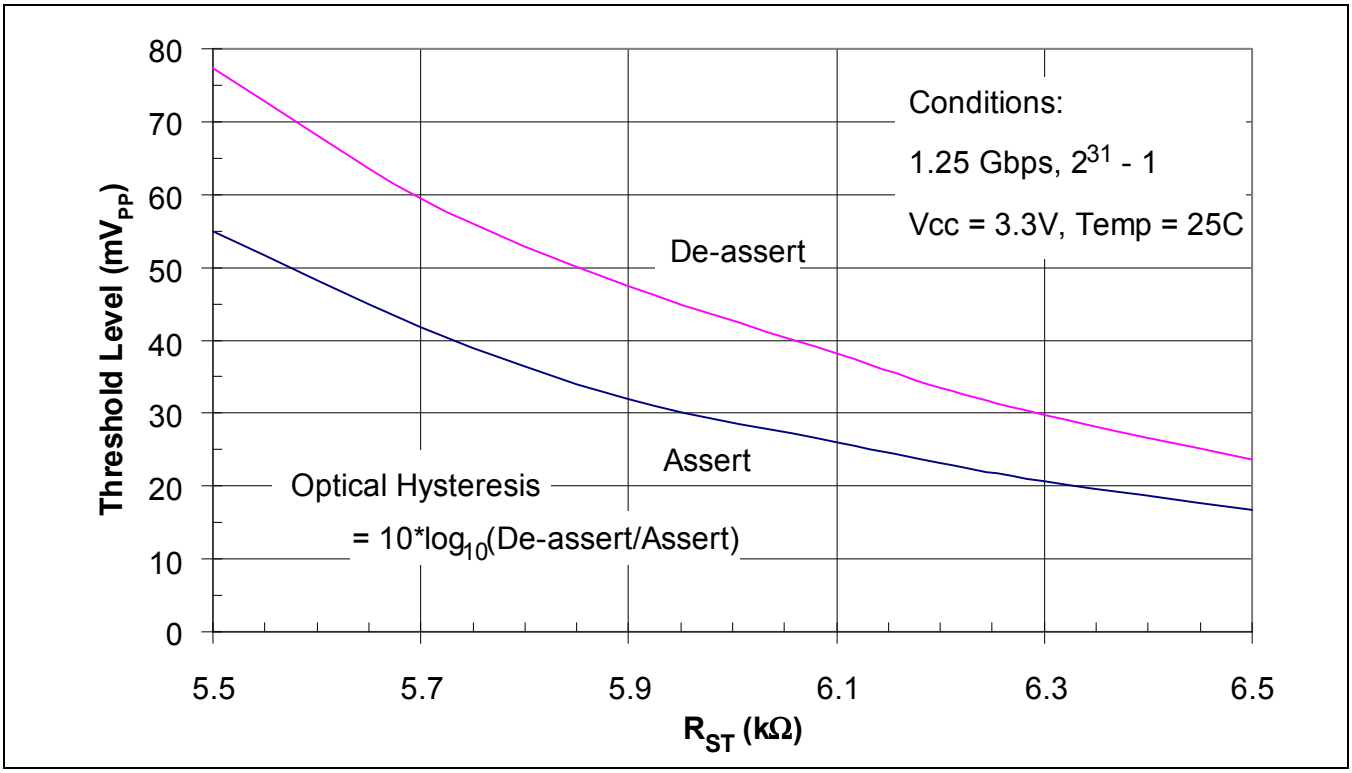
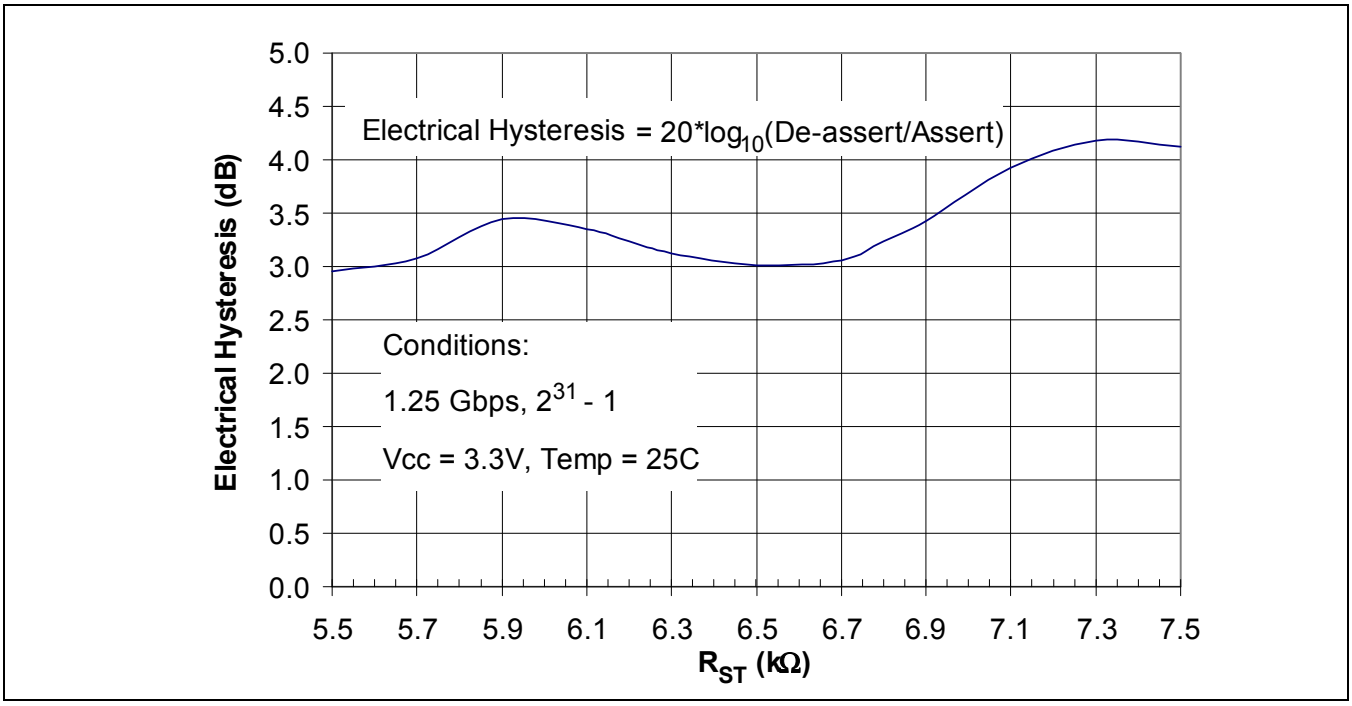


Figure 4-5. Typical Loss of Signal Hysteresis Characteristic (Full Input Signal Range)



4.1.5 PECLP and PECLN Termination

The data outputs of the M02046 are PECL compatible. For the high speed PECLP and PECLN outputs any standard AC or DC-coupling termination technique can be used. Figure 4-6 and Figure 4-7 illustrate typical AC and DC terminations.

AC-coupling is used in applications where the average DC content of the data is zero e.g. SONET. The advantage of this approach is lower power consumption, no susceptibility to DC drift and compatibility with non-PECL interfaces. Figure 4-6 shows the circuit configuration and Table 4-2 lists the resistor values. If using transmission lines other than 50Ω, the shunt terminating resistance Z_T should equal twice the impedance of the transmission line (Z_O).

DC-coupling can be used when driving PECL interfaces and has the advantage of a reduced component count. A Thevenin termination is used at the receive end to give a 50Ω load and the correct DC bias. Figure 4-7 shows the circuit configuration and Table 4-2 the resistor values.

Alternatively, if available, terminating to V_{CC} - 2V as shown in Figure 4-8 has the advantage that the resistance value is the same for 3.3V and 5V operation and it also has performance advantages at high data rates.

In the M02046, ST is a PECL output. It is recommended that it be DC terminated in a PECL load, preferably as shown in Figure 4-8, but the decoupling capacitor on the load is not required as this is a DC output.

Table 4-2. PECL Termination Resistor Values

Supply	Output Impedance	$R_{PULL-DOWN}$	Z_T	R_{TA} / R_{TB}	R_T / R_B
5V	50 Ω	270 Ω	100 Ω	2.7 kΩ / 7.8 kΩ	82 Ω / 130 Ω
3.3V	50 Ω	150 Ω	100 Ω	2.7 kΩ / 4.3 kΩ	130 Ω / 82 Ω

Figure 4-6. AC-Coupled PECL Termination

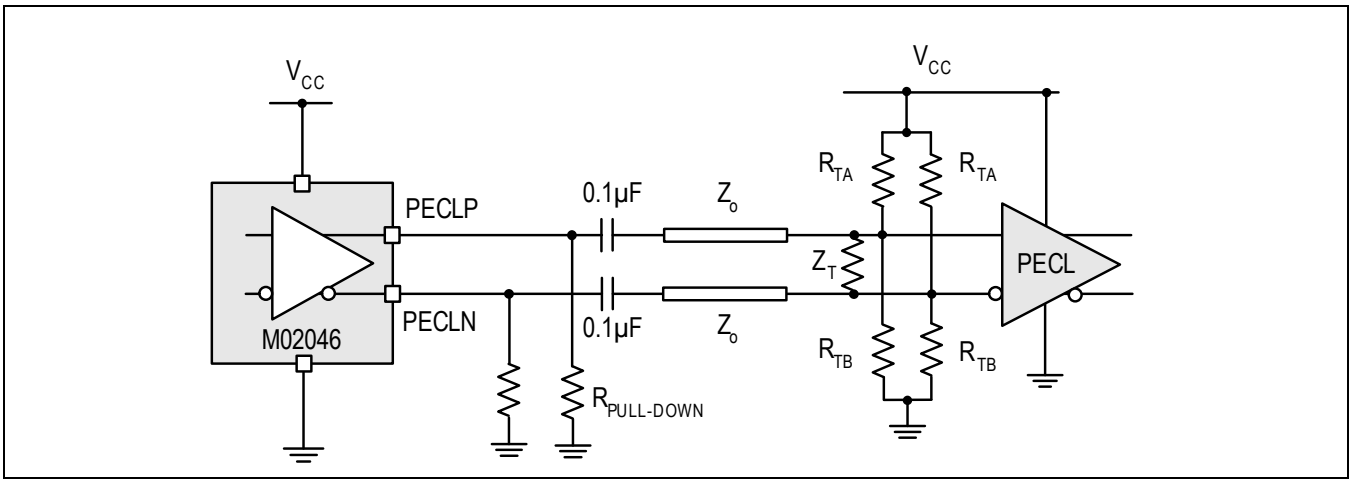


Figure 4-7. DC-Coupled PECL Termination

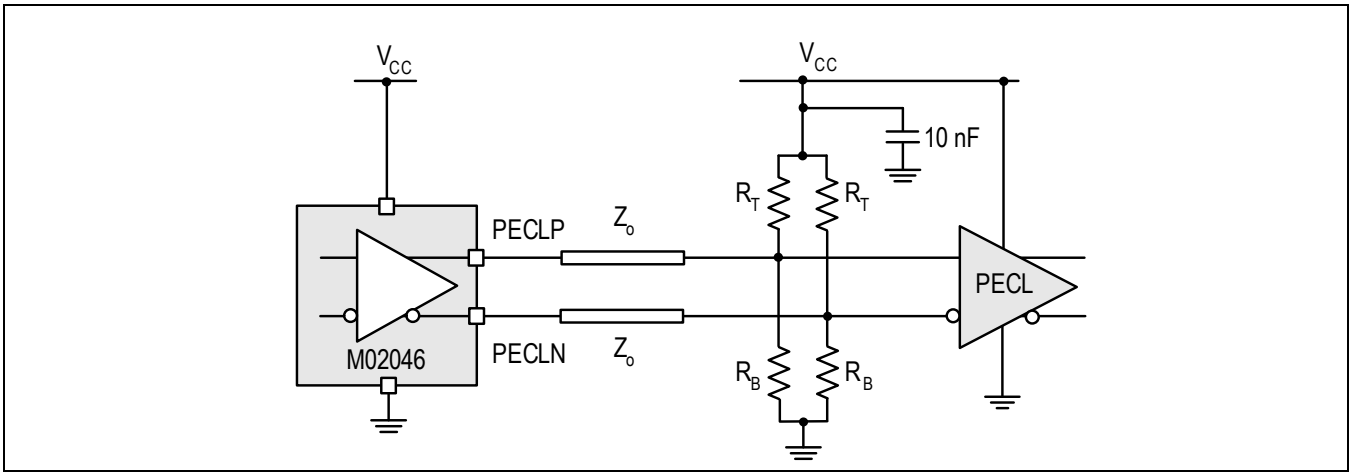
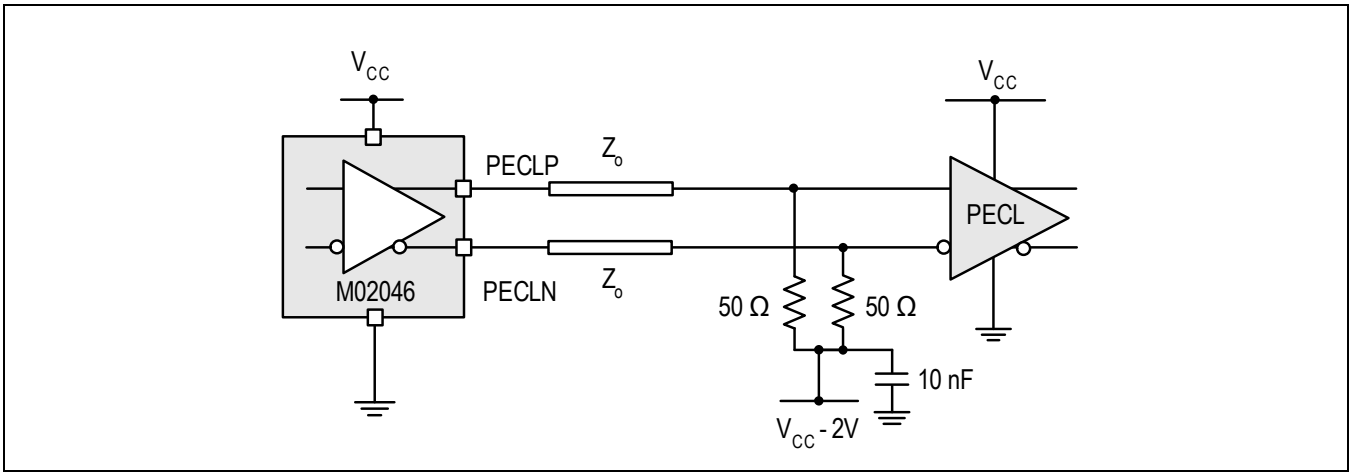


Figure 4-8. Alternative PECL Termination



4.1.6 ST_{PECL} (M02046-25) Termination

The ST (in the PECL version of the part) output of the M02046 is PECL swing compatible. In most module applications, it is not common for this output to be terminated into a standard PECL load as shown in Figure 4-8 for the data outputs because ST is typically in a V_{OH} state and this would consume ~20 mA of continuous supply current. In cases where an alternative termination can be used it is recommended that a single 510Ω resistor be connected between the ST output and ground. When this termination is used, the V_{OH} and V_{OL} levels of the ST output typically meet the standard defined PECL levels and the swing is within PECL limits. This has the additional advantage of reducing the current consumption due to ST being high to <5 mA.

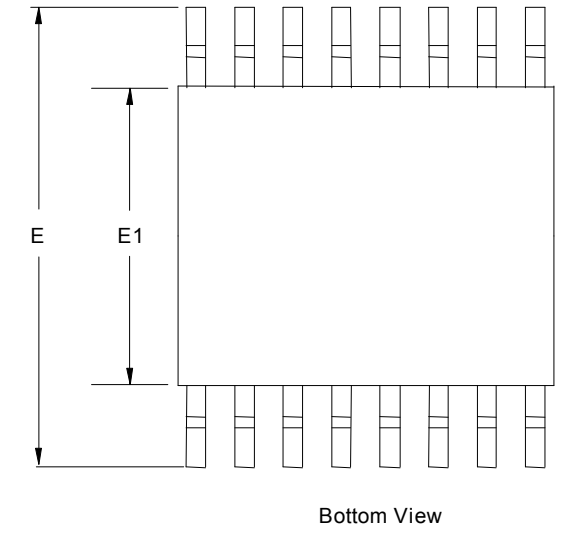
4.1.7 Using JAM

As shown in the typical applications circuit (Figure 1-2), the LOS output pin can optionally be connected to the Jam input pin. When LOS asserts the Jam function sets the data outputs to a fixed “one” state (PECLP is held high and PECLN is held low). This is normally used to allow data to propagate only when the signal is above the users' bit error rate (BER) requirement. It prevents the outputs from toggling due to noise when no signal is present.

From the LOS assert and deassert figures above (Figure 4-2 - Figure 4-4), when an input signal is below the LOS assert threshold, LOS asserts (LOS high) causing Jam to assert. When Jam asserts, the data outputs and the internal servo loop of the M02046-x5 are disabled. If the input signal reaches or exceeds the LOS deassert threshold, LOS deasserts (LOS low) causing Jam to deassert, and hence enables the data outputs and the internal servo loop. If, however, the input signal is slowly increasing to a level that does not exceed the LOS deassert threshold (operating in the hysteresis region), the internal servo loop may not be fully established and this may cause partial enabling of the data outputs. To avoid this the input signal needs to fully reach or exceed the LOS deassert level to fully enable the data outputs.

5.0 Package Specification

Figure 5-1. Package Information



Symbol	Tols/N	QSOP16
A	MAX.	1.60
A1	±.05	0.1
A2	±.05	1.40
D	±.05	4.95
E	±.10	6.00
E1	±.05	3.90
L	±.15	0.60
ccc	MAX.	0.080
ddd	MAX.	0.10
e	BASIC	0.635
b	±.025	0.224
c	±.02	0.22
R	±.05	0.25
R1	Min.	0.20