PIN Diode Limiter
1 - 2 GHz

Features
- Surface Mount Limiter in 8 mm x 5 mm x 2.5 mm Package
- Incorporates PIN Limiter & Schottky Diodes
- DC Blocks & DC Return
- Higher Average Power Handling than Plastic: 100 W CW Power
- Higher Average Peak Handling than Plastic: 1000 W CW Power
- Lower Insertion Loss: 0.35 dB
- Lower Flat Leakage Power: 17 dB
- Ultra-thin AU Termination Plating to Combat Embrittlement
- RoHS* Compliant

Description
The LM102202-Q-x-301 Surface Mount Silicon PIN Diode Limiter is a surface mount, passive two-stage power limiter which can operate over the frequency range of 1 to 2 GHz. It is manufactured using a proven hybrid manufacturing process incorporating PIN Diodes and passive devices integrated onto a ceramic substrate. This low profile, compact, surface mount component offers outstanding small and large signal performance. This product is designed for optimal small signal insertion loss for very low receiver noise figure and excellent large-input-signal flat leakage power for effective receiver protection from 1 to 2 GHz.

The very low thermal resistance (20°C/W, junction to bottom surface of package) of the PIN diodes in this device and the presence of a Schottky detector bias current source enables it to reliably handle RF incident power levels up to 50 dBm CW and RF peak incident power levels up to 60 dBm (25 µs pulse width, 5% duty cycle) at $T_C = 85°C$. The I-layer thickness of the output stage and detector current source combine to produce flat leakage of 17 dBm typical and spike leakage energy of 0.5 ergs, typical. No external control signals are required. This limiter module includes internal DC blocking capacitors in the RF signal path, as well as an internal DC return path.

Ordering Information

<table>
<thead>
<tr>
<th>Part Number1</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM102202-Q-x-301-T</td>
<td>tube packaging</td>
</tr>
<tr>
<td>LM102202-Q-x-301-R</td>
<td>250 or 500 piece reel</td>
</tr>
<tr>
<td>LM102202-Q-x-301-W</td>
<td>waffle packaging</td>
</tr>
<tr>
<td>LM102202Q-x-301-E</td>
<td>RF evaluation board with heat sink</td>
</tr>
</tbody>
</table>

1. Replace x with A, B or C.
   A = No DC block capacitor
   B = DC block capacitor at input end
   C = DC block capacitor at input and output end

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Electrical Specifications: Freq. = 1 - 2 GHz, $P_{IN} = 0$ dBm, $T_A = +25^\circ$C, $Z_0 = 50$ $\Omega$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Units</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Insertion Loss</td>
<td>$1$ GHz $\leq F \leq 2$ GHz, $P_{IN} \leq -10$ dBm</td>
<td>dB</td>
<td>—</td>
<td>0.005</td>
<td>—</td>
</tr>
<tr>
<td>Return Loss</td>
<td>$1$ GHz $\leq F \leq 2$ GHz, $P_{IN} = 0$ dBm</td>
<td>dB</td>
<td>18</td>
<td>20</td>
<td>—</td>
</tr>
<tr>
<td>$P_{1dB}$</td>
<td>$1$ GHz $\leq F \leq 2$ GHz</td>
<td>dBm</td>
<td>8</td>
<td>10</td>
<td>12</td>
</tr>
<tr>
<td>$2^{ND}$ Harmonic</td>
<td>$P_{IN} = 0$ dBm, $F = 2$ GHz</td>
<td>dBc</td>
<td>—</td>
<td>-50</td>
<td>-45</td>
</tr>
<tr>
<td>Peak Incident Power</td>
<td>RF Pulse Width = 25 $\mu$s, duty cycle = 5%, $t_{rise} \leq 2$ $\mu$s, $t_{fall} \leq 2$ $\mu$s</td>
<td>dBm</td>
<td>—</td>
<td>—</td>
<td>60</td>
</tr>
<tr>
<td>CW Incident Power</td>
<td>$1$ GHz $\leq F \leq 2$ GHz</td>
<td>dBm</td>
<td>—</td>
<td>—</td>
<td>50</td>
</tr>
<tr>
<td>Flat Leakage Power</td>
<td>$P_{IN} = 60$ dBm Peak, RF pulse width = 25 $\mu$s, duty cycle = 5%</td>
<td>dBm</td>
<td>—</td>
<td>17</td>
<td>19.5</td>
</tr>
<tr>
<td>Spike Leakage Energy</td>
<td>$P_{IN} = 60$ dBm peak, RF pulse width = 25 $\mu$s, duty cycle = 5%</td>
<td>erg</td>
<td>—</td>
<td>0.5</td>
<td>0.6</td>
</tr>
<tr>
<td>Recovery Time</td>
<td>50% falling edge of RF pulse to 1 dB IL, $P_{IN} = 50$ dBm peak, RF pulse width = 25 $\mu$s, duty cycle = 5%</td>
<td>$\mu$s</td>
<td>—</td>
<td>1.0</td>
<td>3</td>
</tr>
<tr>
<td>Recovery Time</td>
<td>50% falling edge of RF pulse to 1 dB IL, $P_{IN} = 60$ dBm peak, RF pulse width = 1 $\mu$s, duty cycle = 5%</td>
<td>$\mu$s</td>
<td>—</td>
<td>1.0</td>
<td>3</td>
</tr>
</tbody>
</table>

Absolute Maximum Ratings\(^2,3\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Absolute Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF Input &amp; Output DC Block</td>
<td></td>
</tr>
<tr>
<td>Capacitor Voltage Breakdown</td>
<td></td>
</tr>
<tr>
<td>Voltage Breakdown at 10$\mu$A</td>
<td>45 V DC</td>
</tr>
<tr>
<td>RF CW Incident Power @ +85$^\circ$C, Source &amp; Load VSWR &lt;1.2:1</td>
<td>50 dBm</td>
</tr>
<tr>
<td>Derate linearly $t$ 0 W @ $T_C = +150^\circ$C(^4)</td>
<td></td>
</tr>
<tr>
<td>RF Peak Incident Power @ +85$^\circ$C, Source &amp; Load VSWR &lt;1.2:1</td>
<td>60 dBm</td>
</tr>
<tr>
<td>Derate linearly $t$ 0 W @ $T_C = +150^\circ$C(^4)</td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance</td>
<td>25$^\circ$C/W</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>+175$^\circ$C</td>
</tr>
<tr>
<td>Operating / Storage Temperature</td>
<td>-65$^\circ$C to +150$^\circ$C</td>
</tr>
<tr>
<td>Assembly Temperature</td>
<td>260$^\circ$C for 30 seconds</td>
</tr>
</tbody>
</table>

2. Exceeding any one or combination of these limits may cause permanent damage to this device.
3. MACOM does not recommend sustained operation near these survivability limits.
4. $T_C$ is defined as the temperature of the bottom surface of the package.
Typical Performance Curves

Corrected Insertion Loss vs. Frequency (insertion loss of evaluation board subtracted from overall insertion loss)

Return Loss vs. Frequency

CW Output Power vs. CW Input Power

Flat Leakage Output Power vs. Input Power,
Pulse width = 10 µs, Duty Cycle = 1%, f = 2 GHz
Handling Procedures
Please observe the following precautions to avoid damage:

Static and Moisture Sensitivity
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these Class 0 (HBM) devices.

The moisture sensitivity level rating for this device is MSL 1.

Environmental Capabilities
This limiter is capable of meeting the environmental requirements of MIL-STD-750 and MIL-STD-202.

Thermal Grounding Caution
Product engineering dictates that the LM family of high power limiters require proper heat sinking for high power applications >40 dBm (10 W). MACOM recommends using the part number PNMN13881 heat sink block which was developed for LM family.

Assembly Instructions
The LM102202-Q-x-301 limiters are capable of being placed onto circuit boards with pick and place manufacturing equipment from tube or tape & reel dispensing. The devices are attached to the circuit board using conventional solder re-flow or wave soldering procedures with RoHS type or Sn 60 / Pb 40 type solders per Table I & Graph I Time-Temperature recommended profile.

RF Circuit Solder Footprint, case style 301 (CS301)

Recommended RF circuit is Rogers R04350B, 10 mils thick.
The hatched metal area on circuit side of device is RF, DC and thermal grounded. Vias should be solid copper fill and gold plated for optimum heat transfer from backside of switch module through circuit vias to metal thermal ground.
Criteria for Proper Mounting on PCB

When a large signal is incident upon the input of the LM102202-Q-x-301, the impedance of the coarse limiter diodes is forced to a low value by the charge which is injected into these diodes by the combination of the current from the internal detector stage and the large RF voltage initially present across these diodes. As the impedance of these diodes decreases, an increasingly large impedance mismatch with the impedance of the transmission line to which the limiter is connected is created. Ultimately, the impedance of the coarse limiter diodes is reduced to a few ohms or less. This mismatch creates a standing wave, with a current maximum and voltage minimum located at the position of the coarse limiter diodes. While the large majority of the input signal power is reflected back to its source due to the impedance mismatch, the significant RF current that flows at the current maximum causes Joule heating to occur in the coarse limiter diodes. In order to maintain the junction temperature of these diodes below their maximum rated value, there must be a path with minimal thermal resistance from the coarse diodes to the external system heat sink. Also, there must be a minimal electrical resistance and inductance between the underside of the limiter module package and the system ground in order to achieve maximum RF isolation between the input and the output of the limiter module.

For these reasons, it is imperative that there are no voids in the electrical and thermal paths directly under the coarse limiter diodes. Care must be taken when mounting the LM102202-Q-x-301 to avoid voids in the solder joint in the area along the lengthwise axis of the package, under and between the filled vias in the AlN substrate of the module which are shown in the diagram (above). It is also important to ensure no solder voids exist between the limiter module RF ports and the PCB to which the limiter module is attached. No greater than 50% of the remaining metalized area on the bottom of the package may contain solder voids.
The evaluation board for the LM102202-Q-x-301 is shown above. This evaluation board comprises two sections: the evaluation circuit for the LM102202-Q-C-301 limiter module; and, a reference transmission line.

The limiter module is mounted in position U1. Its RF input is connected to J1 and its output port is connected to J2, via two 50-Ω microstrip transmission lines.

For LM102202-Q-A-301 external DC blocking capacitors are recommended at input and output ports. For LM102202-Q-B-301 an external DC blocking capacitor is recommended at the RF output port. LM102202-Q-C-301 contains internal DC blocking capacitors in its input and output ports and does not need external DC blocking capacitors.

The reference path 50-Ω microstrip transmission line structure can be utilized to determine the insertion loss of the transmission line structures connected between J1 and the limiter module input, as well as between the limiter module output and J2, so that their respective insertion losses may be subtracted from the total insertion loss measured between J1 and J2. This enables the resolution of the insertion loss of the limiter module only.

The evaluation board supplied is mounted on a heat sink. The maximum RF input power specified in the Absolute Maximum Ratings table must not be exceeded.

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Table 1: Time-Temperature Profile for Sn 60 / Pb 40 or RoHS Type Solders

<table>
<thead>
<tr>
<th>Profile Feature</th>
<th>Sn-Pb Eutectic Assembly</th>
<th>Pb-Free Assembly</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average ramp-up rate (TL to TP)</td>
<td>3°C/second maximum</td>
<td>3°C/second maximum</td>
</tr>
<tr>
<td>Preheat</td>
<td></td>
<td></td>
</tr>
<tr>
<td>- Temperature Minimum (TSMIN)</td>
<td>100°C</td>
<td>150°C</td>
</tr>
<tr>
<td>- Temperature Maximum (TSMAX)</td>
<td>150°C</td>
<td>200°C</td>
</tr>
<tr>
<td>- Time (Minimum to maximum) (ts)</td>
<td>60-120 seconds</td>
<td>60-180 seconds</td>
</tr>
<tr>
<td>TSMAX to TL</td>
<td>—</td>
<td>3°C/second maximum</td>
</tr>
<tr>
<td>- Ramp-up Rate</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Time Maintained above:</td>
<td></td>
<td></td>
</tr>
<tr>
<td>- Temperature (TL)</td>
<td>183°C</td>
<td>217°C</td>
</tr>
<tr>
<td>- Time (TL)</td>
<td>60-150 seconds</td>
<td>60-150 seconds</td>
</tr>
<tr>
<td>Peak Temperature (TP)</td>
<td>225 +0 / -5°C</td>
<td>245 +0 / -5°C</td>
</tr>
<tr>
<td>Time within 5°C of actual Peak Temperature (TP)</td>
<td>10-30 seconds</td>
<td>20-40 seconds</td>
</tr>
<tr>
<td>Ramp-down Rate</td>
<td>6°C/second maximum</td>
<td>6°C/second maximum</td>
</tr>
<tr>
<td>Time 25°C to Peak Temperature</td>
<td>6 minutes maximum</td>
<td>8 minutes maximum</td>
</tr>
</tbody>
</table>

Graph1: Solder Re-Flow Time-Temperature Function
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Pin Out

Outline Drawing, Case Style 301 (CS301)

The hatched metal area on circuit side of device is RF and DC grounded.
Dimensions are in inches (mm)
Substrate Material: 20 mil thick Alumina Nitride (ALN)
RF Cover: Black Ceramic
Top Side and Backside Metallization: 100 µ IN. typical plated over Ti-Pd.