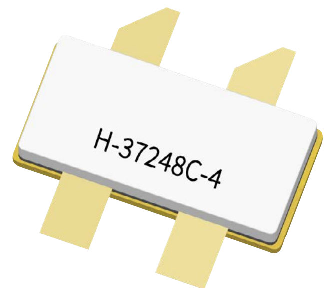
GTVA261802FC

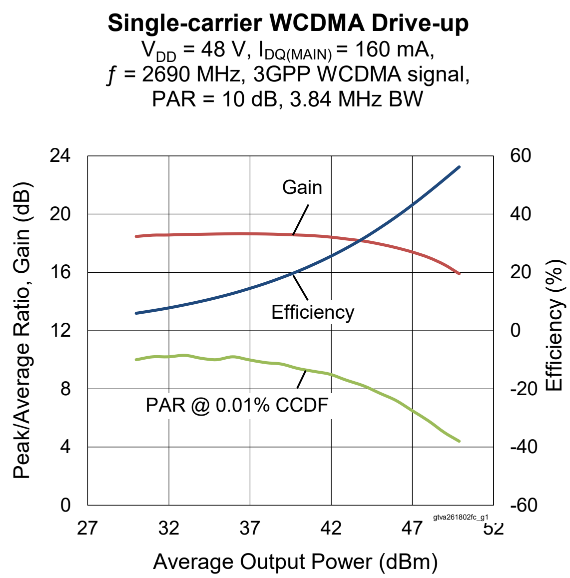
Thermally-Enhanced High Power RF GaN on SiC HEMT
170 W, 48 V, 2620 – 2690 MHz



Package Types: H-37248C-4

Description

The GTVA261802FC is a 170-watt GaN on SiC high electron mobility transistor (HEMT) for use in multi-standard cellular power amplifier applications. It features input matching, high efficiency, and a thermally-enhanced package with earless flange.



Features

- GaN on SiC HEMT technology
- Input matched
- Typical Pulsed CW performance, combined outputs, 2690 MHz, 48 V, 10 µs pulse width, 10% duty cycle
  - Output power at P_{3dB} = 170 W
  - Drain Efficiency at P_{3dB} = 65.5%
  - Gain at P_{3dB} = 15 dB
- Capable of handling 10:1 VSWR @ 48 V, 180 W (CW) output power
- Human Body Model Class 1A (per ANSI/ESDA/JEDEC JS-001)
- Low thermal resistance
- Pb-free and RoHS compliant

RF Characteristics

Single-carrier WCDMA Specifications (tested in the production test fixture)

V_{DD} = 48 V, I_{DQ} = 160 mA, P_{OUT} = 50 W avg, ƒ = 2690 MHz, 3GPP, channel bandwidth = 3.84 MHz, peak/average = 10 dB @ 0.01% CCDF

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Gain	G_{ps}	15.5	16.8	—	dB
Drain Efficiency	η_D	40	43	—	%
Adjacent Channel Power Ratio	ACPR	—	-27	-24.5	dBc
Output PAR @ 0.01% CCDF	OPAR	4.5	5.3	—	dB

Note:
All published data at T_{CASE} = 25°C unless otherwise indicated
ESD: Electrostatic discharge sensitive device—observe handling precautions!

RoHS compliant

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DC Characteristics

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain-source Breakdown Voltage	$V_{BR(DSS)}$	150	—	—	V	V_{GS} = -8 V, I_D = 10 mA
Drain-source Leakage Current	I_{DSS}	—	—	1.5	mA	V_{GS} = -8 V, V_{DS} = 10 V
Gate Threshold Voltage	$V_{GS(th)}$	–3.8	–3.0	–2.3	V	V_{DS} = 10 V, I_D = 10 mA

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	0	—	50	V	
Gate Quiescent Voltage	$V_{GS(Q)}$	–3.60	–2.97	-2.3		V_{DS} = 48 V, I_D = 160 mA

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source Voltage	V_{DSS}	125	V
Gate-source Voltage	V_{GS}	–10 to +2	
Gate Current	I_G	10.8	mA
Drain Current	I_D	4	A
Junction Temperature	T_J	225	°C
Storage Temperature Range	T_{STG}	–65 to +150	

Operation above the maximum values listed here may cause permanent damage. Maximum ratings are absolute ratings; exceeing only one of these values may cause irreversible damage to the component. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For reliable continuous operation, the device should be operated within the operating voltage range (V_{DD}) specified above.

Thermal Characteristics

Characteristics	Symbol	Value	Unit	Conditions
Thermal Resistance	$R_{\theta JC}$	1.06	°C/W	T_{CASE} = 70°c, 100 W CW

Ordering Information

Type and Version	Order Code	Package Description	Shipping
GTVA261802FC V1 R0	GTVA261802FC-V1-R0	H-37248C-4, earless flange	Tape & Reel, 50 pcs
GTVA261802FC V1 R2	GTVA261802FC-V1-R2	H-37248C-4, earless flange	Tape & Reel, 250 pcs

Typical Performance (data taken in test fixture)

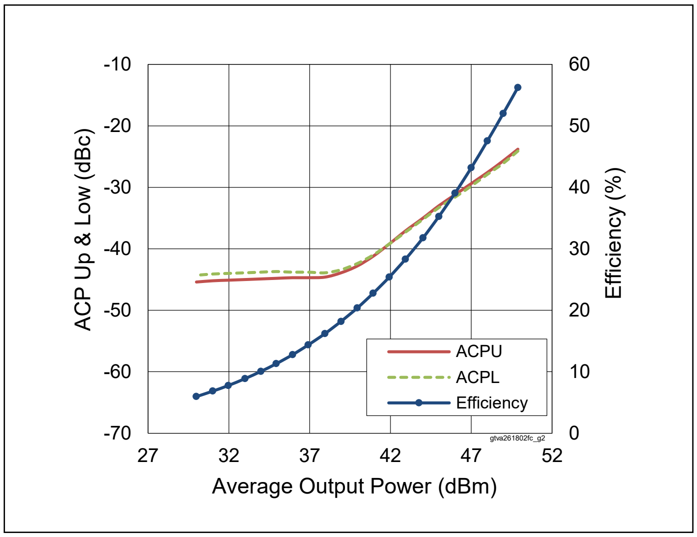


Figure 1. Single-carrier WCDMA Drive-up

V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 160 mA,
f = 2690 MHz, 3GPP WCDMA signal,
PAR = 10 dB, BW = 3.84 MHz

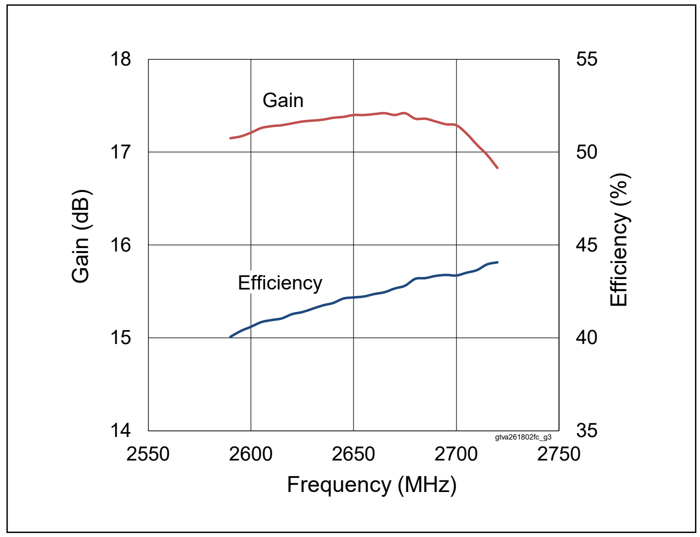


Figure 2. Single-carrier WCDMA Broadband Performance

V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 160 mA,
P_{OUT} = 47 dBm, 3GPP WCDMA signal,
PAR = 10 dB

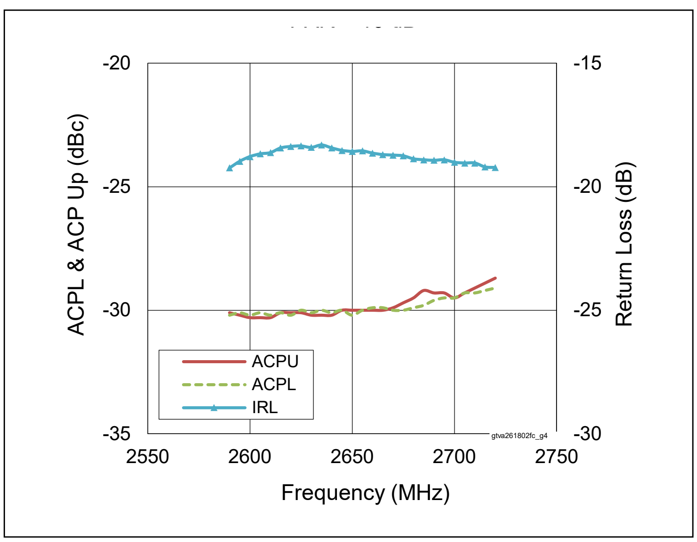


Figure 3. Single-carrier WCDMA Broadband Performance

V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 160 mA,
P_{OUT} = 47 dBm, 3GPP WCDMA signal,
PAR = 10 dB

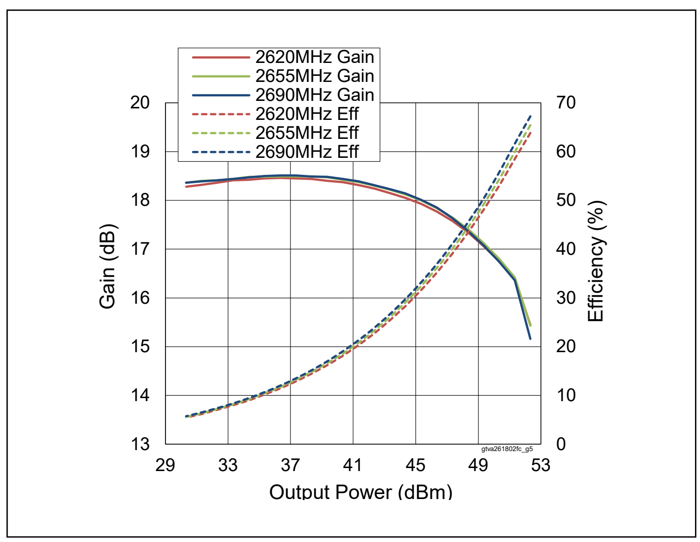


Figure 4. CW Performance

V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 160 mA

Typical Performance (cont.)

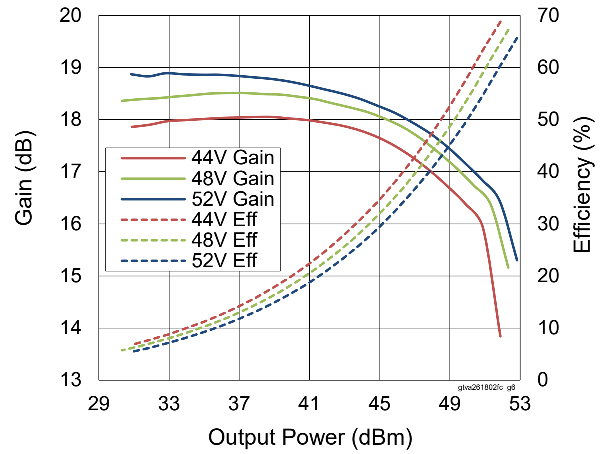


Figure 5. CW Performance at various V_{DD}

$I_{DQ(MAIN)}$ = 160 mA, f = 2690 MHz

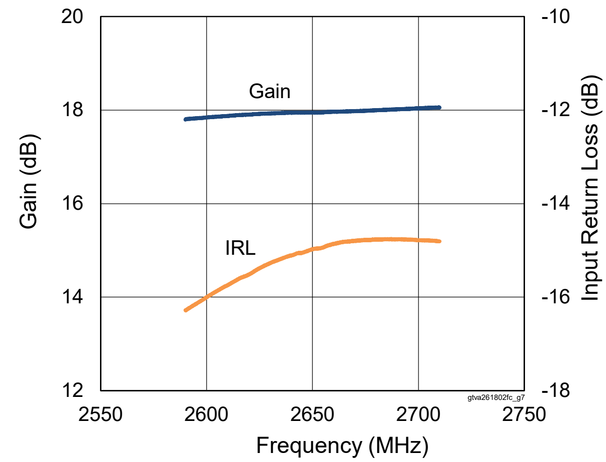


Figure 6. CW Performance Small Signal Gain & Input Return Loss

V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 160 mA

Load Pull Performance

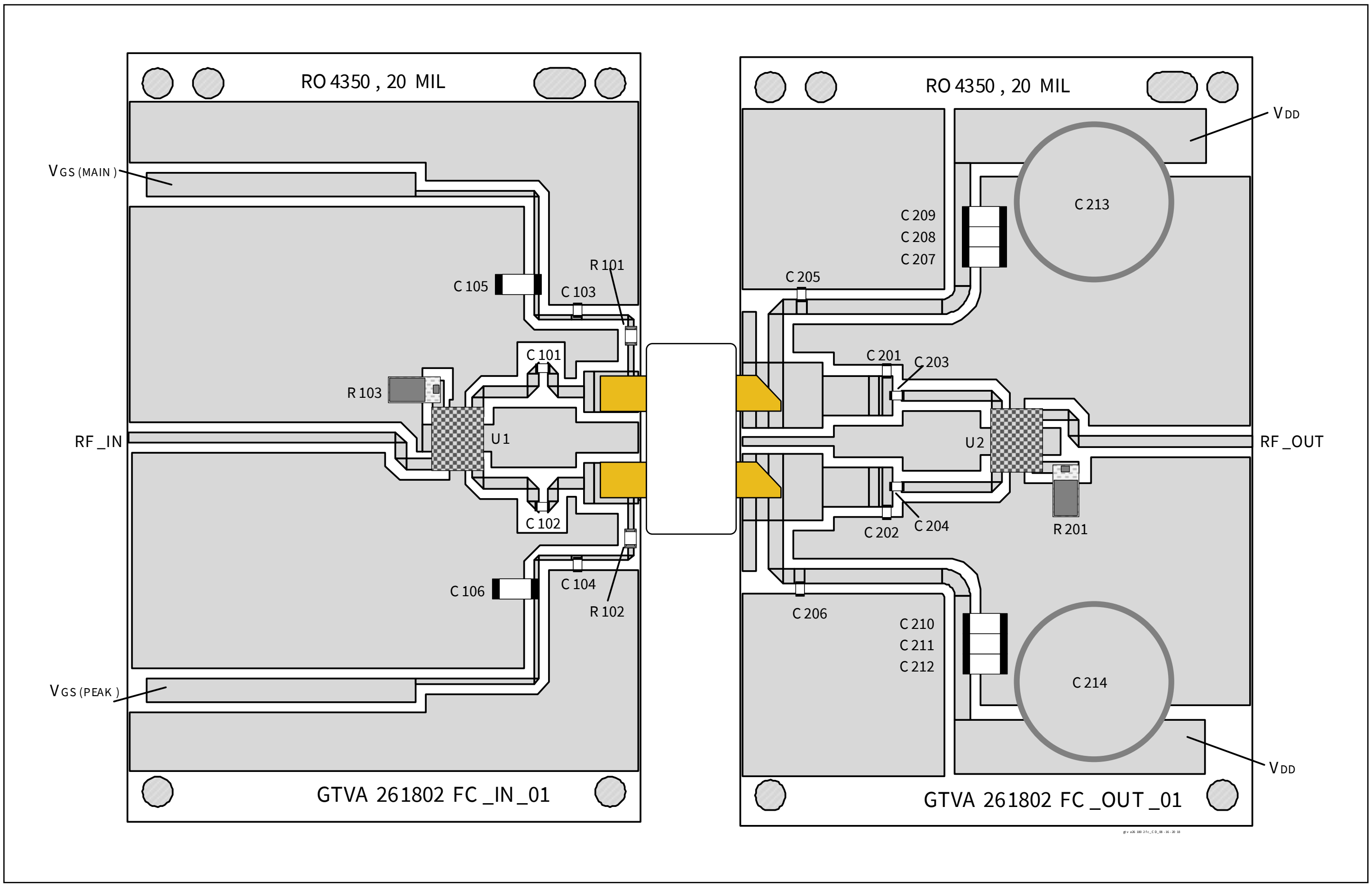
Each Side Load Pull Performance – Pulsed CW signal: 10 µs, 10% duty cycle, 48 V, I_{DQ} = 80 mA, class AB

		P_{3dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]
2620	32.6-j23.3	7.02-j0.46	16	50.35	108.4	69.2	3.6+j1.73	16.4	48.60	72.4	77.7
2690	41.87-j10.33	5.38-j0.83	15.9	50.21	105	65.1	5.38-j0.83	15.8	48.60	72.4	77.6

Peak Side Load Pull Performance – Pulsed CW signal: 10 µs, 10% duty cycle, 48 V, I_{DQ} = 80 mA, class AB

		P_{3dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]
2620	32.6-j23.3	7.02-j0.46	16	50.35	108.4	69.2	3.6+j1.73	16.4	48.60	72.4	77.7
2690	41.87-j10.33	5.38-j0.83	15.9	50.21	105	65.1	5.38-j0.83	15.8	48.60	72.4	77.6

Evaluation Board, 2620 – 2690 MHz



Reference circuit assembly diagram (not to scale)

Evaluation Board Part Number	LTN/GTVA261802FC-V1
PCB Information	Rogers 4350, 0.508 mm [0.020"] thick, 2 oz. copper, ε_r = 3.66, f = 2620 – 2690 MHz

Components Information

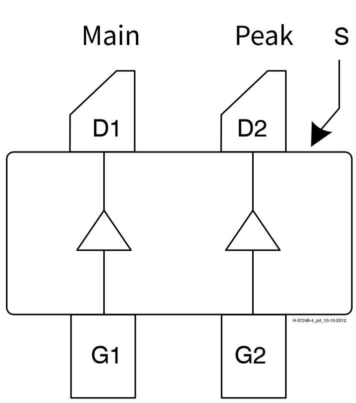
Component	Description	Manufacturer	P/N
Input			
C101, C102, C103, C104	Capacitor, 12 pF	ATC	ATC600F120JT250X
C105, C106	Capacitor, 100V, 4.7 µF	TDK Corporation	C4532X7S2A475M230KB
R101, R102	Resistor, 10 ohms	Panasonic Electronic Components	ERJ-8GEYJ100V
R103	Resistor, 50 ohms	Richardson	C16A50Z4
U1	Hybrid coupler	Anaren	X3C26P1-03S
Output			
C201, C202	Capacitor, 0.5 pF	ATC	ATC600F0R5JT250X
C203, C204, C205, C206	Capacitor, 12 pF	ATC	ATC600F120JT250X
C207, C208, C209, C210, C211, C212	Capacitor, 100 V, 4.7 µF	TDK Corporation	C4532X7S2A475M230KB
C213, C214	Capacitor, 470 µF	Cornell Dubilier Electronics (CDE)	SEK471M050ST
R201	Resistor, 50 ohms	Richardson	C16A50Z4
U2	Hybrid coupler	Anaren	X3C26P1-03S

Bias Sequencing

Bias On
1. Ensure RF is turned off
2. Apply pinch-off voltage of –5 V to the gate
3. Apply nominal drain voltage
4. Bias gate to desired quiescent drain current
5. Apply RF

Bias Off
1. Turn RF off
2. Apply pinch-off voltage to the gate
3. Turn-off drain voltage
4. Turn-off gate voltage

Pinout Diagram (top view)



Pin	Description
D1	Drain Device 1 (Main)
D2	Drain Device 2 (Peak)
G1	Gate Device 1(Main)
G2	Gate Device 2 (Peak)
S	Source (flange)

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Package Outline Specifications – Package H-37248C-4

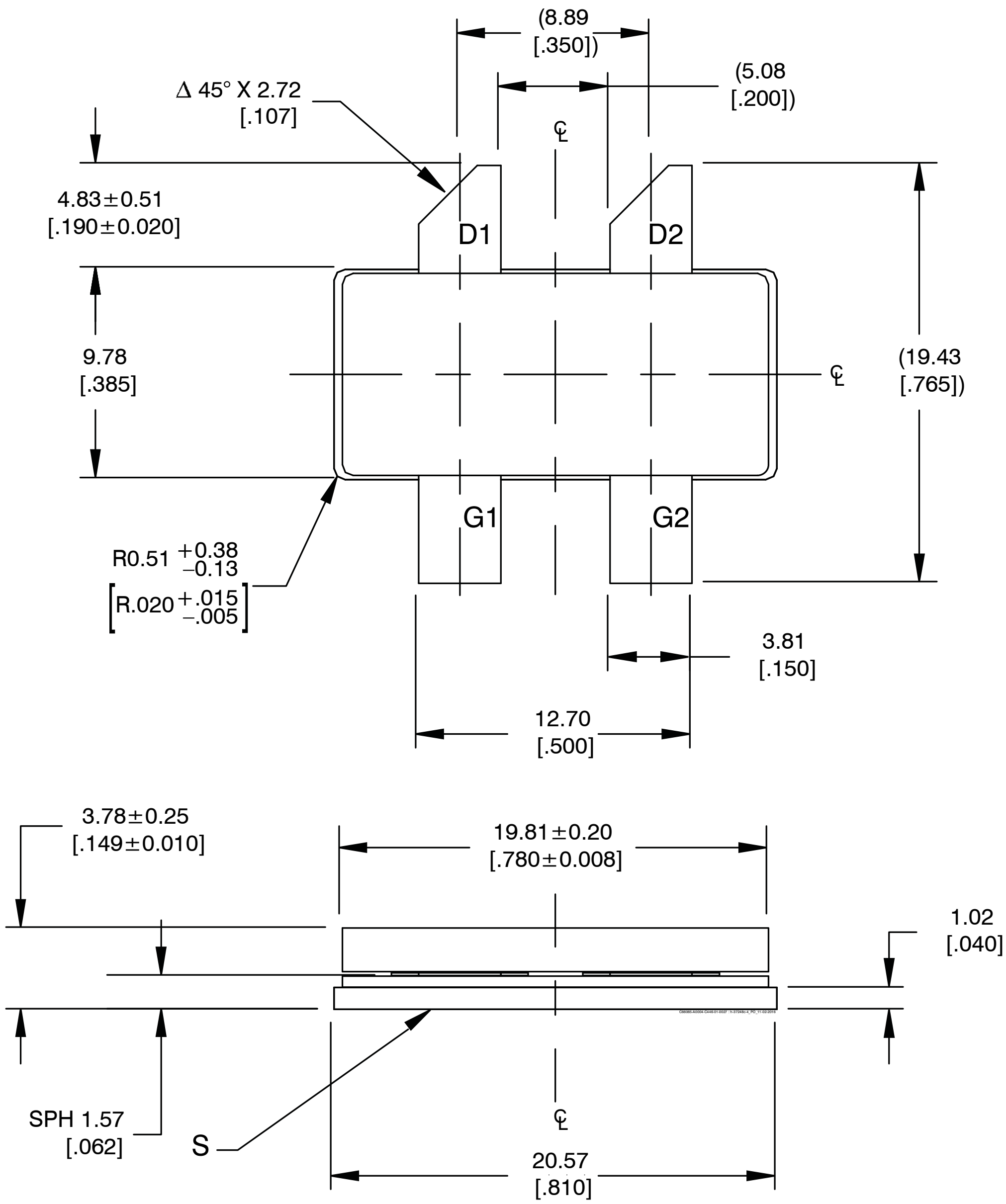

Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994
2. Primary dimensions are mm, alternate dimensions are inches
3. All tolerances ± 0.127 [0.005]
4. Pins: D1, D2 – drain, G1, G2 – gate, S – source (flange)
5. Lead thickness: 0.13 ± 0.05 [0.005 ± 0.002]
6. Gold plating thickness: 1.14 ± 0.38 micron [45 ± 15 microinch]

Notes & Disclaimer