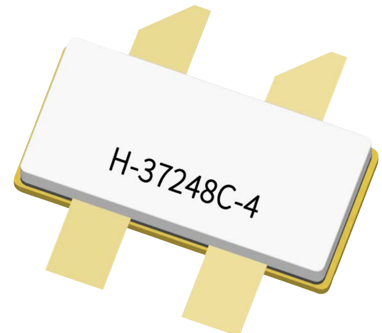
GTRA214602FC

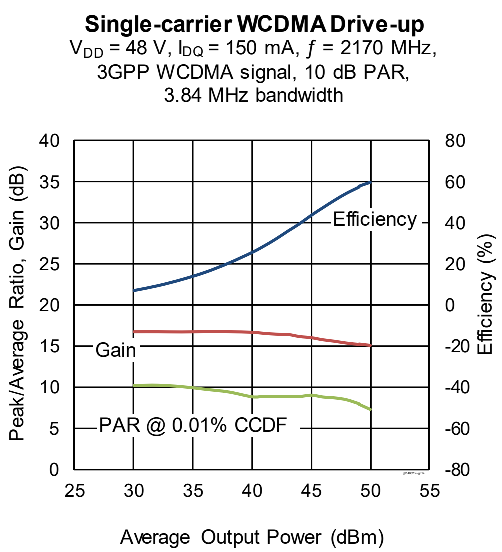
Thermally-Enhanced High Power RF GaN on SiC HEMT
490 W, 48 V, 2110 – 2170 MHz



Package Types: H-37248C-4
PN: GTRA214602FC

Description

The GTRA214602FC is a 490-watt (P_{3dB}) GaN on SiC high electron mobility transistor (HEMT) designed for use in multi-standard cellular power amplifier applications. It features input matching, high efficiency, and a thermally-enhanced package with earless flange.



Features

- GaN on SiC HEMT technology
- Input matched
- Asymmetric Doherty design
  - Main: P_{3dB} = 170 W Typ
  - Peak: P_{3dB} = 350 W Typ
- Typical pulsed CW performance: 16 µs pulse width, 10% duty cycle, 2140 MHz, 48 V, Doherty fixture
  - Gain = 15 dB @ 49 dBm
  - Efficiency = 60% @ 49 dBm
  - Output power at P_{3dB} = 490 W
- Human Body Model Class 1B (per ANSI/ESDA/ JEDEC JS-001)
- Low thermal resistance
- Pb-free and RoHS compliant

Target RF Characteristics

Single-carrier WCDMA Specifications (tested in the Doherty test fixture)
V_{DD} = 48 V, I_{DQ} = 150 mA, $V_{GS(PEAK)}$ = –5.5 V, P_{OUT} = 80 W avg, ƒ = 2170 MHz
3GPP signal, channel bandwidth = 3.84 MHz, peak/average = 10 dB @ 0.01% CCDF

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Gain	G_{ps}	13	14.4	—	dB
Drain Efficiency	η_D	56	59	—	%
Adjacent Channel Power Ratio	ACPR	—	–30	–27	dBc
Output PAR @ 0.01% CCDF	OPAR	7.1	8.2	—	dB

Note:
All published data at T_{CASE} = 25°C unless otherwise indicated
ESD: Electrostatic discharge sensitive device—observe handling precautions!

RoHS compliant

DC Characteristics

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain-source Breakdown Voltage (main)	$V_{BR(DSS)}$	150	—	—	V	V_{GS} = -8 V, I_D = 10 mA
Drain-source Breakdown Voltage (peak)						
Drain-source Leakage Current	I_{DSS}	—	—	5.5	mA	V_{GS} = -8 V, V_{DS} = 10 V
Gate Threshold Voltage (main)	$V_{GS(th)}$	–3.8	–3.0	–2.3	V	V_{DS} = 10 V, I_D = 20 mA
Gate Threshold Voltage (peak)						V_{DS} = 10 V, I_D = 38 mA

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	0	—	50	V	
Gate Quiescent Voltage	$V_{GS(Q)}$	-3.7	–3.1	-2.6		V_{DS} =48 V, I_D = 150 mA

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source Voltage	V_{DSS}	125	V
Gate-source Voltage	V_{GS}	–10 to +2	
Operating Voltage	V_{DD}	55	
Gate Current (main)	I_G	20	mA
Gate Current (peak)		38.4	
Drain Current (main)	I_D	7.5	A
Drain Current (peak)		14.4	
Junction Temperature	T_J	225	°C
Storage Temperature Range	T_{STG}	–65 to +150	

Operation above the maximum values listed here may cause permanent damage. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the component. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For reliable continuous operation, the device should be operated within the operating voltage range (V_{DD}) specified above.

Thermal Characteristics

Thermal resistance, junction to case: T_{CASE} = 70°C, 2170 MHz, V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 150 mA, $V_{GS(PEAK)}$ = –5.5 V

Characteristics	Symbol	Value	Unit	Conditions
Thermal Resistance (main)	$R_{\theta JC}$	2.0	°C/W	76 W DC
Thermal Resistance (peak)		1.5		106 W DC

Ordering Information

Type and Version	Order Code	Package	Shipping
GTRA214602FC V1 R0	GTRA214602FC-V1-R0	H-37248C-4	Tape & Reel, 50 pcs
GTRA214602FC V1 R2	GTRA214602FC-V1-R2	H-37248C-4	Tape & Reel, 250 pcs

Typical Performance (data taken in a the production test fixture)

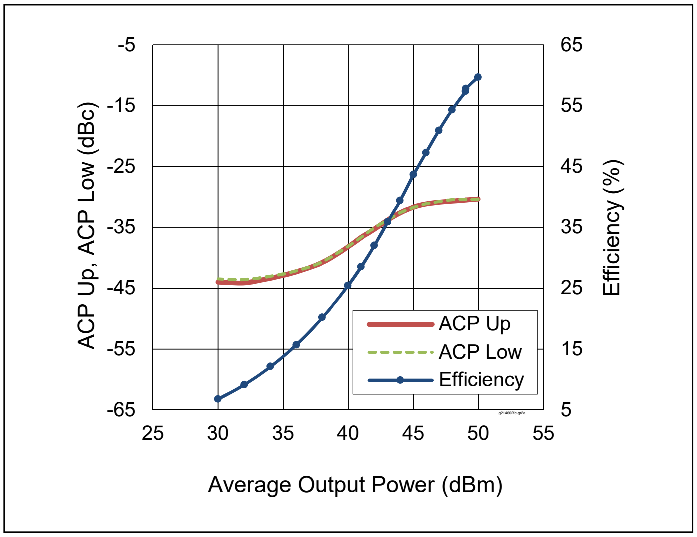


Figure 1. Single-carrier WCDMA Drive-up

V_{DD} = 48 V, I_{DQ} = 150 mA, ƒ = 2170 MHz,
3GPP WCDMA signal, 10 dB PAR,
3.84 MHz bandwidth

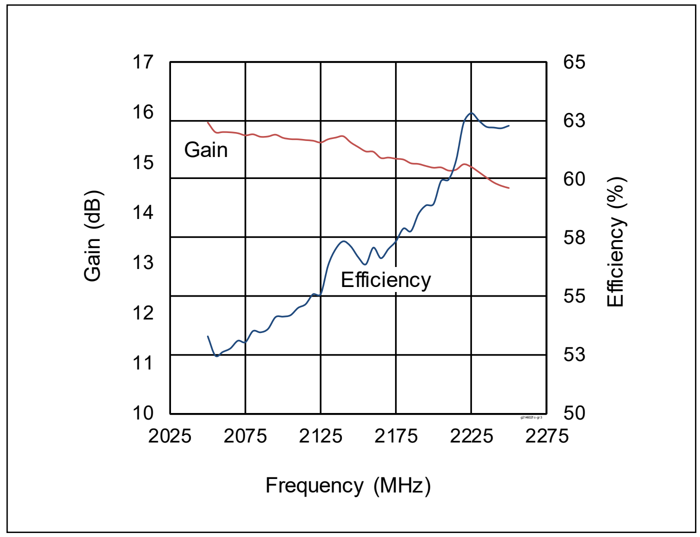


Figure 2. Single-carrier WCDMA Broadband Performance

V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 150 mA, P_{OUT} = 49 dBm,
3GPP WCDMA signal, 10 dB PAR,
3.84 MHz bandwidth

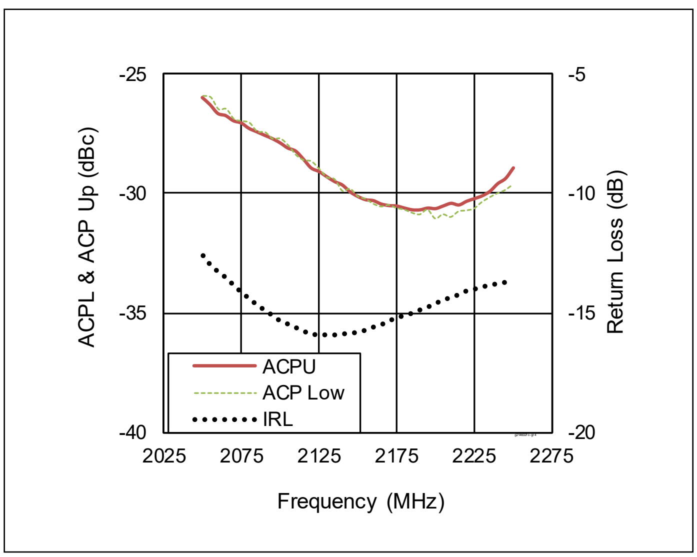


Figure 3. Single-carrier WCDMA Broadband Performance

V_{DD} = 48V, $I_{DQ(MAIN)}$ = 150 mA, P_{OUT} = 49 dBm,
3GPP WCDMA signal, 10 dB PAR,
3.84 MHz bandwidth

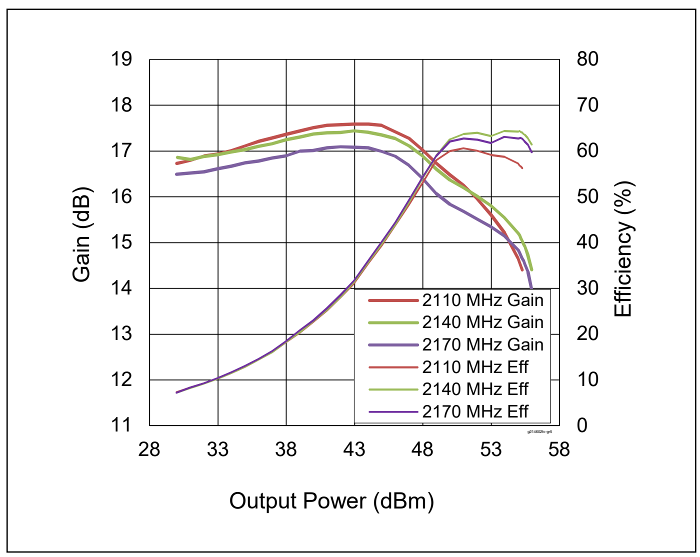


Figure 4. Pulsed CW Performance

V_{DD} = 48 V, I_{DQ} = 150 mA,
40 µs pulse width, 10% duty cycle

Typical Performance (cont.)

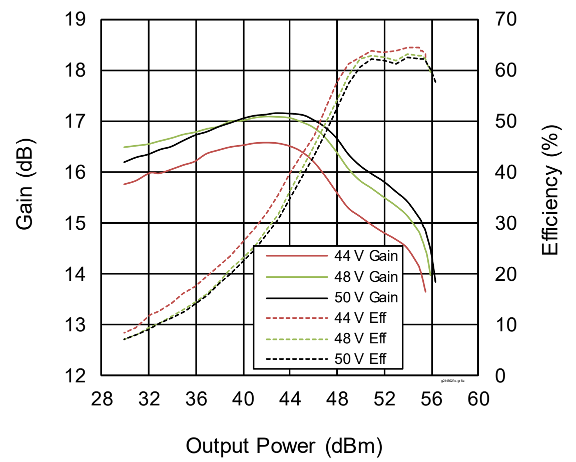


Figure 5. Pulsed CW Performance at various V_{DD}

I_{DQ} = 150 mA, 40 µs pulse width, 10% duty cycle, *ƒ* = 2170 MHz

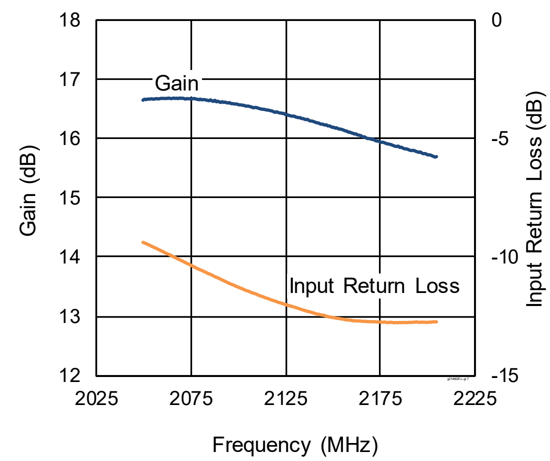


Figure 6. CW Performance Small Signal Gain & Input Return Loss

V_{DD} = 48 V, I_{DQ} = 150 mA,

Load Pull

Main Side Load Pull Performance – Pulsed CW signal: 10 µs pulse width, 10% duty cycle; 48 V, I_{DQ} = 150 mA, class AB

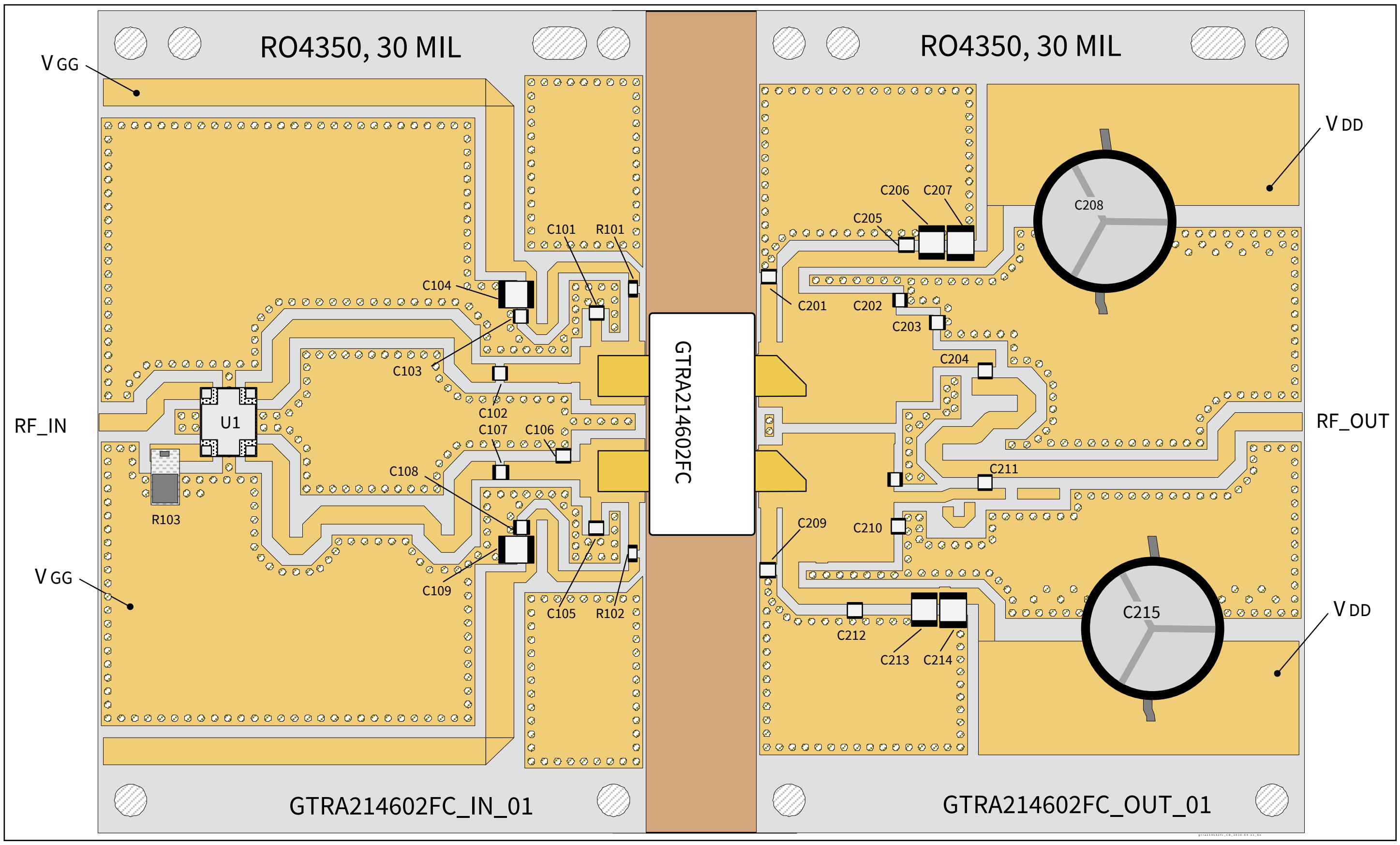
		P_{3dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	ηD [%]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	ηD [%]
2110	7.7 – j13.6	3.1 – j1.8	17.2	53.00	200	71.0	2.8 + j0.4	18.9	50.90	123	80.8
2140	13.8 – j12.5	3.5 – j2.3	16.6	52.80	191	68.1	2.4 + j0.7	19	50.60	115	83.0
2170	13.0 – j7.0	3.0 – j2.3	16.4	52.80	191	68.1	2.6 + j0.4	18.3	50.80	120	82.5

Peak Side Load Pull Performance – Pulsed CW signal: 10 µs pulse width, 10% duty cycle; 48 V, $V_{GS(PEAK)}$ = –3.6 V, class C

		P_{3dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	ηD [%]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	ηD [%]
2110	5.8 – j9.0	2.4 – j3.7	15.5	56.40	437	67	2.2 – j1.6	17.2	54.60	288	77.2
2140	7.0 – j9.5	2.5 – j3.7	15.5	56.30	427	66	2.2 – j1.8	17.1	54.60	288	76.0
2170	8.2 – j8.0	2.5 – j3.9	15.3	56.40	437	65	2.0 – j1.8	17.5	54.80	302	79.0

Evaluation Board, 2110 – 2170 MHz

Test Fixture Part Number	LTA/GTRA214602FC-V1
PCB Information	Rogers 4350, 0.762 mm [0.030”] thick, 2 oz. copper, ε_r = 3.66



Reference circuit assembly diagram (not to scale)

Bias Sequencing

Bias ON

1. Ensure RF is turned off
2. Apply pinch-off voltage of –5 V to the gate
3. Apply nominal drain voltage
4. Bias gate to desired quiescent drain current
5. Apply RF

Bias OFF

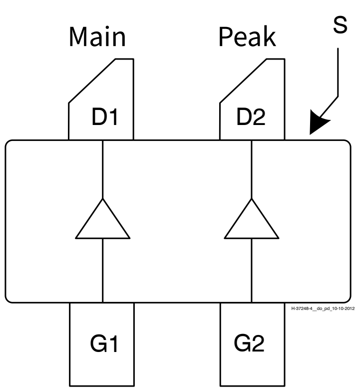
1. Turn RF off
2. Apply pinch-off voltage of to the gate
3. Turn off drain voltage
4. Turn off gate voltage

Rev. 02.1, 2022-1-27

Components Information

Component	Description	Manufacturer	P/N
Input			
C101, C105	Capacitor, 1.5 pF	ATC	ATC600F1R5BT250XT
C102, C103, C107, C108	Capacitor, 18 pF	ATC	ATC600F180JT250XT
C104, C109	Capacitor, 10 µF, 100 V	Murata Electronics	GRM32EC72A106KE05L
C106	Capacitor, 1.3 pF	ATC	ATC600F1R3BT250XT
R101, R102	Resistor, 9.1 ohms	Panasonic Electronic Components	ERJ-3GEYJ9R1V
R103	Resistor, 50 ohms	Anaren	C8A50Z4A
U1	Hybrid coupler	Anaren	X3C21P1-03S
Output			
C201, C209	Capacitor, 1 pF	ATC	ATC600F1R0BT250XT
C202	Capacitor, 0.9 pF	ATC	ATC600F0R9BT250XT
C203	Capacitor, 0.2 pF	ATC	ATC600F0R2BT250XT
C204	Capacitor, 7.5 pF	ATC	ATC600F7R5BT250XT
C205, C212	Capacitor, 18 pF	ATC	ATC600F180JT250XT
C206, C207, C213, C214	Capacitor, 10 µF, 100 V	Murata Electronics	GRM32EC72A106KE05L
C208, C215	Capacitor, 470 µF, 100 V	Panasonic Electronic Components	ECA-2AHG471B
C210	Capacitor, 0.7 pF	ATC	ATC600F0R7BT250XT
C211	Capacitor, 15 pF	ATC	ATC600F150JT250XT

Pinout Diagram (top view)



Pin	Description
D1	Drain Device 1
D2	Drain Device 2
G1	Gate Device 1
G2	Gate Device 2
S	Source (flange)

Package Outline Specifications – Package H-37248C-4

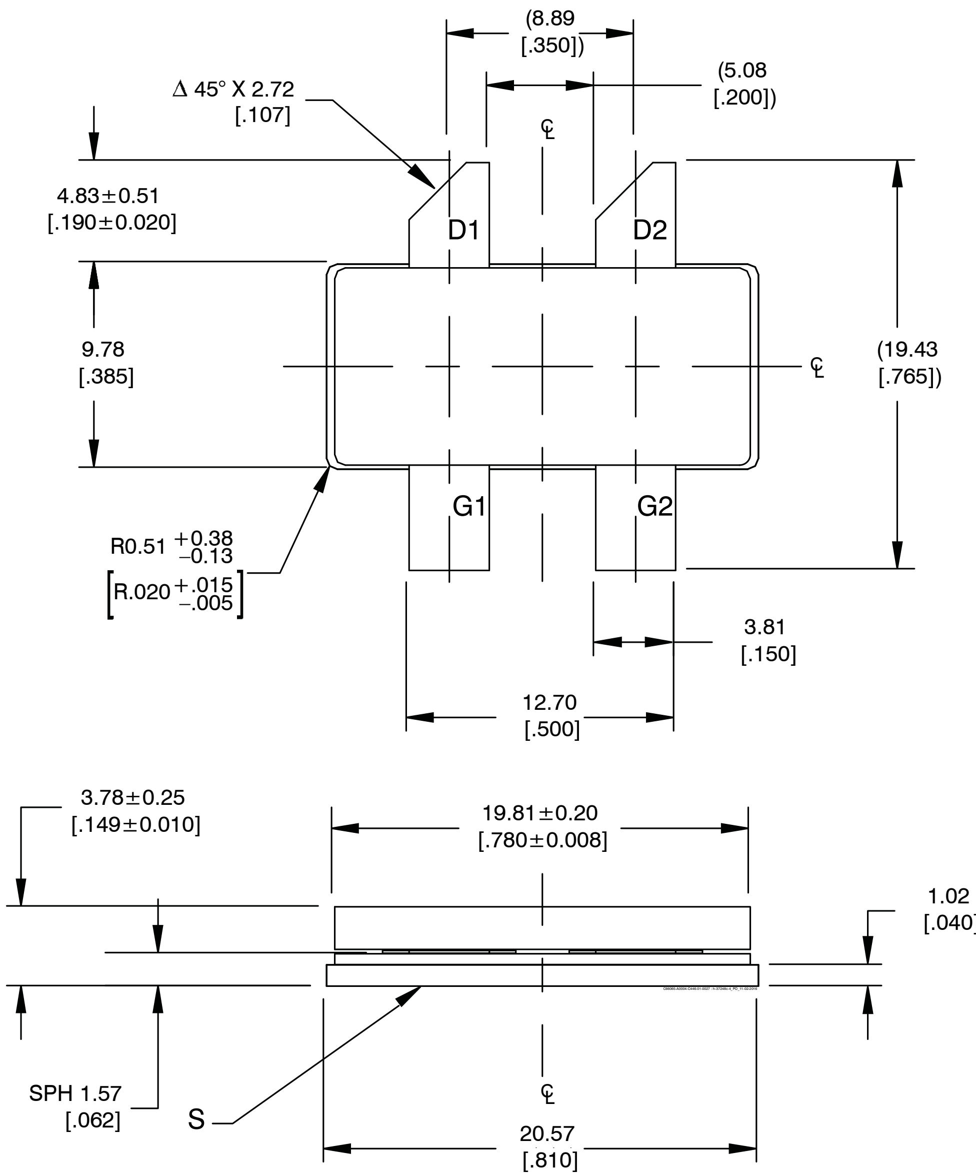


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994
2. Primary dimensions are mm, alternate dimensions are inches
3. All tolerances ± 0.127 [0.005]
4. Pins: D1, D2 – drain, G1, G2 – gate, S – source (flange)
5. Lead thickness: 0.13 ± 0.05 [0.005 ± 0.002]
6. Gold plating thickness: 1.14 ± 0.38 micron [45 ± 15 microinch]

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