

Transmit / Receive Module

8.0 - 11.5 GHz

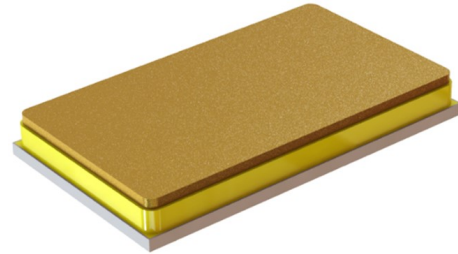


ENGSD00085

Rev. V1

Features

- 8.0 to 11.5 GHz Band Coverage
- Gain RX/TX: >23 dB
- Noise Figure: 1.25 dB
- OIP3: >20 dBm
- TX Saturated Output Power: 3 W
- PAE @ P_{SAT}: 35%
- Size: (0.427" x 0.254" x 0.060")
- RoHS* Compliant



Applications

- Commercial or Military Radar
- Electronic Warfare Circuits
- Receive Circuits
- Telecom Infrastructure
- Test & Measurement Systems

Description

The ENGSD00085 is a Transmit/Receive module operating across 8 to 11.5 GHz. The module provides 23 dB small signal gain in both transmit and receive paths. In the receive path, the module offers noise figure of 1.25 dB typical. In the transmit path, the module offers 3 W saturated output power and 35% PAE. The ENGSD00085 uses microstrip or stripline interfaces for the RF input and output ports. The module is packaged in a ceramic QFN package.

Ordering Information

Part Number	Package
ENGSD00085	bulk

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

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Electrical Specifications @ T_A = 25°C:

Receive Mode:

Freq. = 8 - 11.5 GHz, VD_LNA = +3.5 V, SW_V0 = +5 V, SW_V1 = -20 V

Parameter	Min	Typ	Max	Units
RX Gain	23	26	29	dB
Noise Figure	—	1.25	2.0	dB
OIP3	18	20	—	dBm
Output P1dB	12	14	—	dBm
RX Input Return Loss	10	12	—	dB
RX Output Return Loss	10	14	—	dB
VD_LNA Supply Current	80	100	120	mA

Transmit Mode:

Freq. = 8 - 11.5 GHz, VD1_PA = VD2_PA = +28 V, SW_V0 = -20 V, SW_V1 = +5 V

Parameter	Min	Typ	Max	Units
TX Gain	22	25	28	dB
Saturated Output Power	2.5	3.0	—	Watts
PAE at Psat	—	35, average	—	%
TX Input Return Loss	7.5	10	—	dB
TX Output Return Loss	—	6	—	dB
VD_PA Supply Current (Idq)	—	200	—	mA
VD_PA Supply Current (at Psat)	—	350	480	mA

Common Requirements:

Parameter	Min	Typ	Max	Units
Current (+5 V)	8	10	20	mA
Current (-20 V) SW_V0, SW_V1, SW_V2	—	0.005	0.1	
Switch Isolation	35	38	—	dB
Switching Time 50% CTRL to 90% / 10% of detected RF	—	150	200	ns

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
VD1_PA, VD2_PA	20	28	30	V
VD_LNA	2.5	3.5	4.0	V
SW_V0, SW_V1	-20	-20 or +5	+5	V
VG1_PA, VG2_PA	-1.3	-1.8	-2.0	V
VG_LNA	-0.8	-0.5	-0.3	V
Operating Temperature	-40	+25	+85	°C

Switch Truth Table

State	SW_V0 (V)	SW_V1 (V)
TX Path ON	-5	-20
RX Path ON	-20	+5

Absolute Maximum Ratings^{1,2}

Parameter	Absolute Maximum
VD1_PA, VD2_PA	+32 V
VD_LNA	+4.5 V
SW_V0, SW_V1	+7 V or -25 V
VG1_PA, VG2_PA	-6 V
VG_LNA	+1.5 V
RX RF Input Power	20 dBm
TX RF Input Power	30 dBm
Storage Temperature	-65°C to +125°C

1. Exceeding any one or combination of these limits may cause permanent damage to this device.
2. MACOM does not recommend sustained operation near these survivability limits.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

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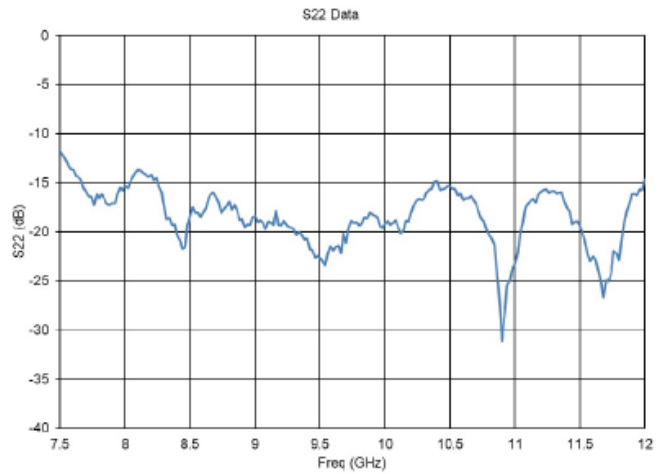
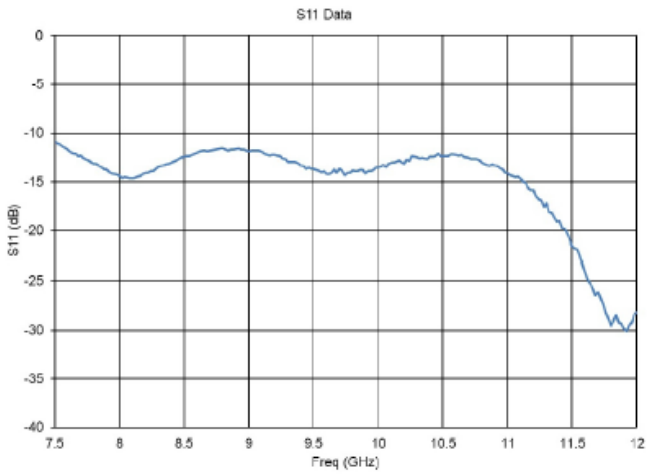
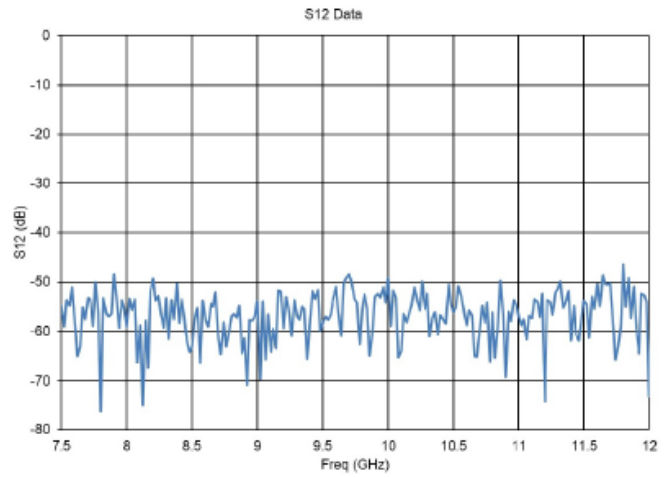
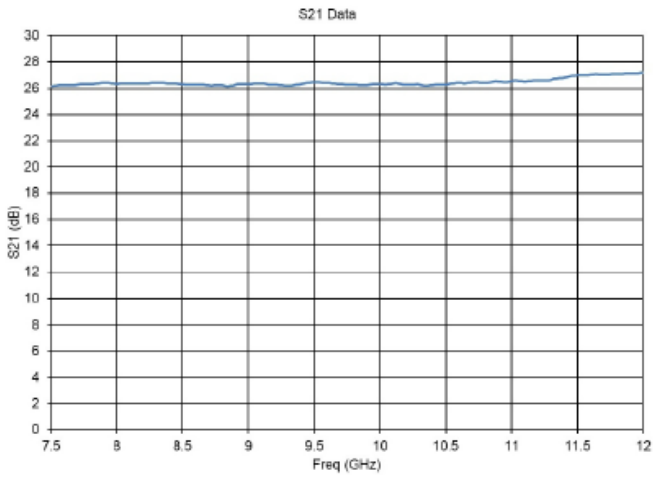


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Typical Performance @ +25°C - Receive Mode

Small Signal Gain, Reverse Isolation, Input/Output Return Loss:
VD_LNA = +3.3 V, SW_V0 = +5 V, SW_V1 = -20 V, RX Idq = 100 mA



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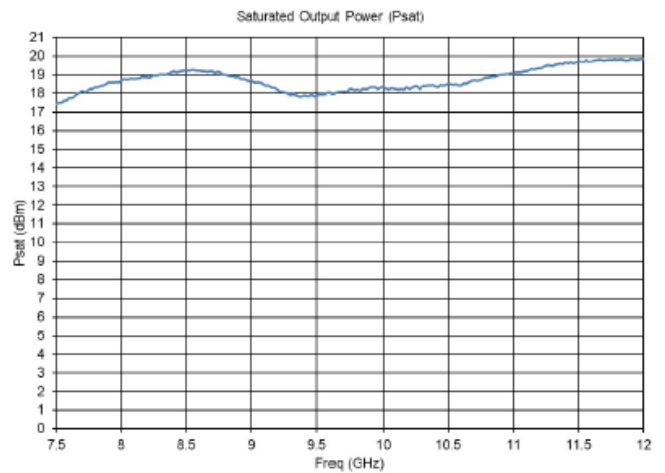
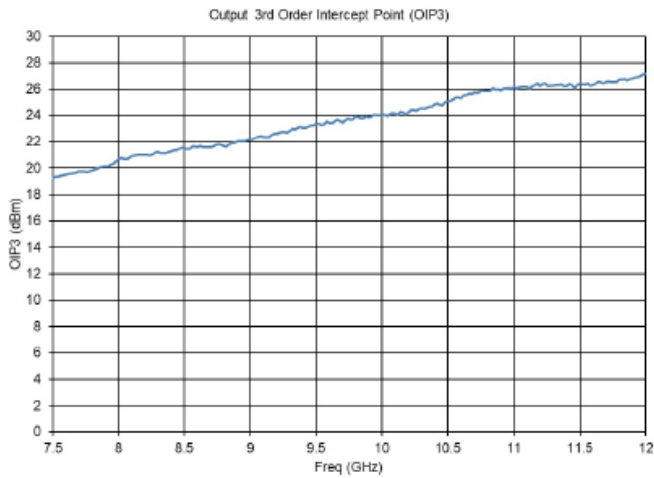
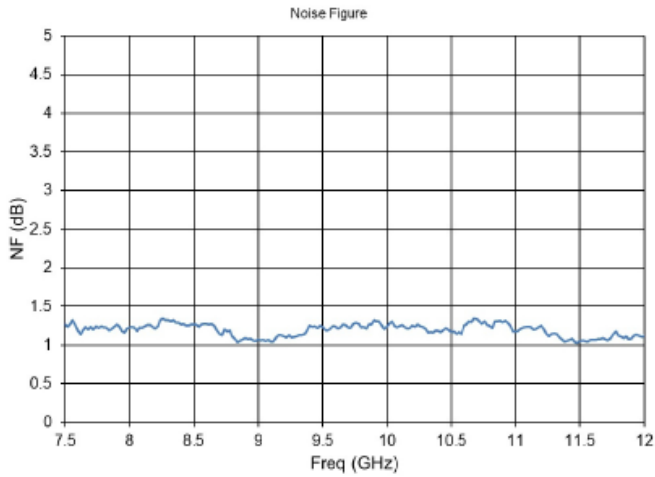
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Rev. V1

Typical Performance @ +25°C - Receive Mode

Noise Figure, OP1dB, OIP3, Terminated Mode Return Loss:

VD_LNA = +3.5 V, SW_V0 = +5 V, SW_V1 = -20 V, RX Idq = 100 mA



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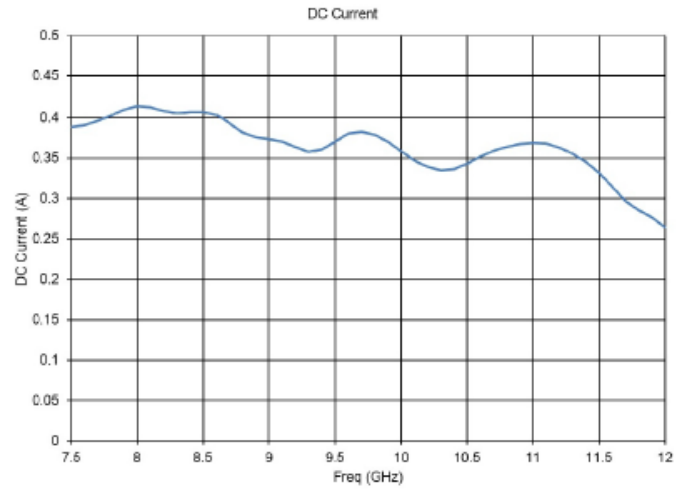
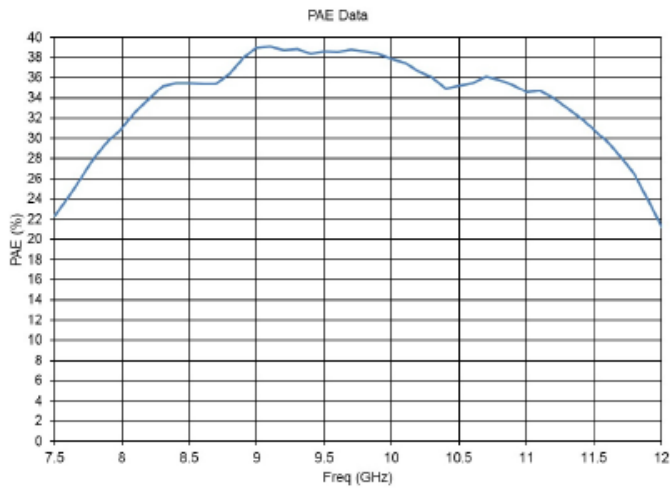
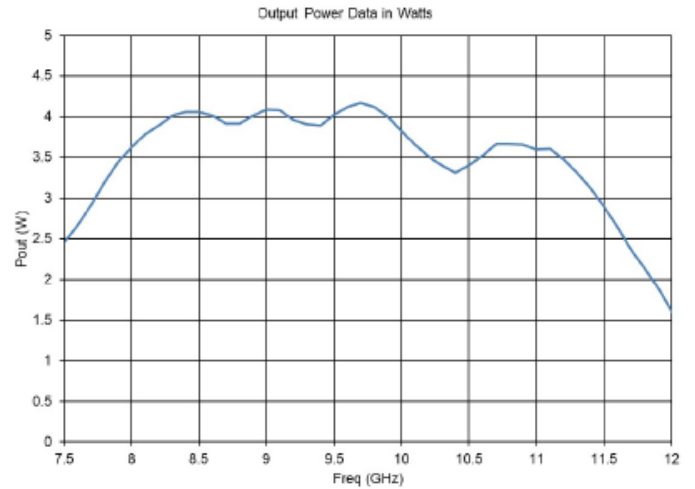
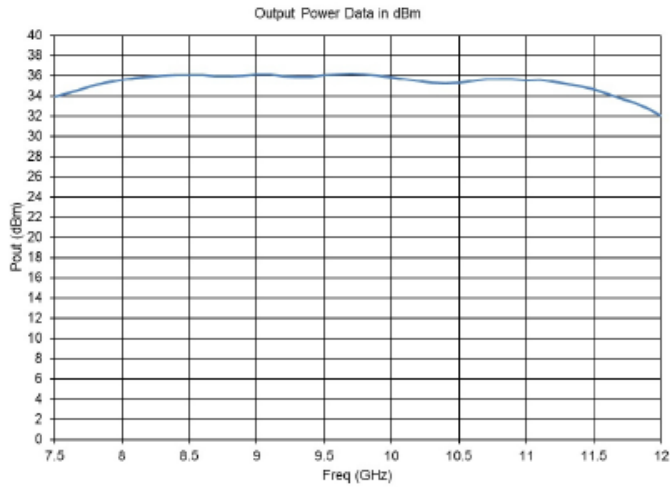
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Typical Performance @ +25°C - Transmit Mode

Output Power, PAE, DC Current:

VD1_PA = VD2_PA = +28 V, SW_V0 = -20 V, SW_V1 = +5 V, TX Idq = 200 mA, VG1_PA = VG2_PA = -1.8 V, P_{IN} = 15 dBm



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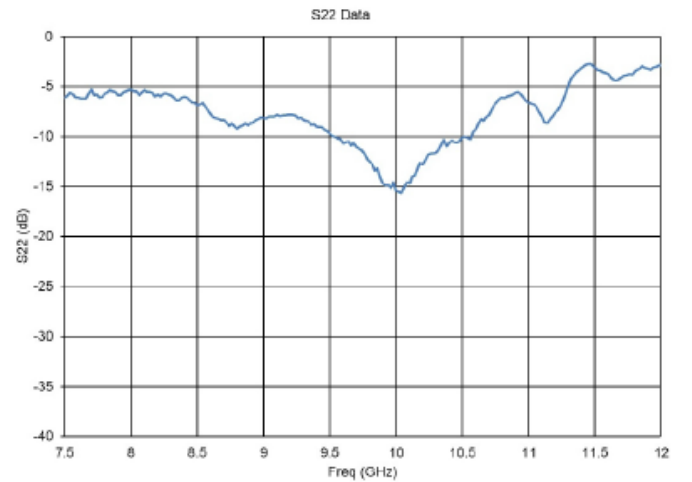
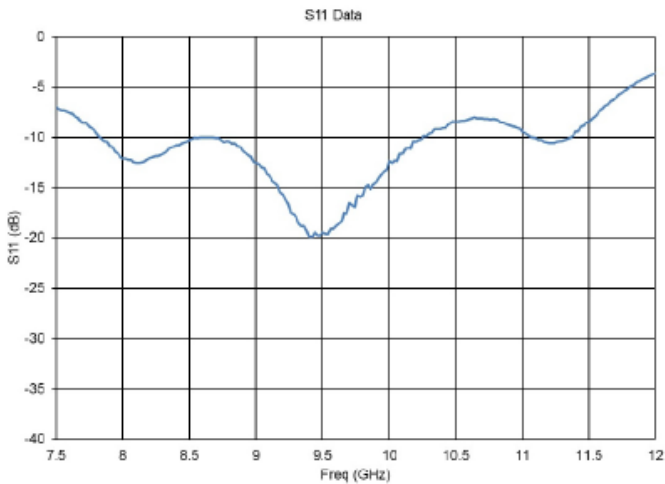
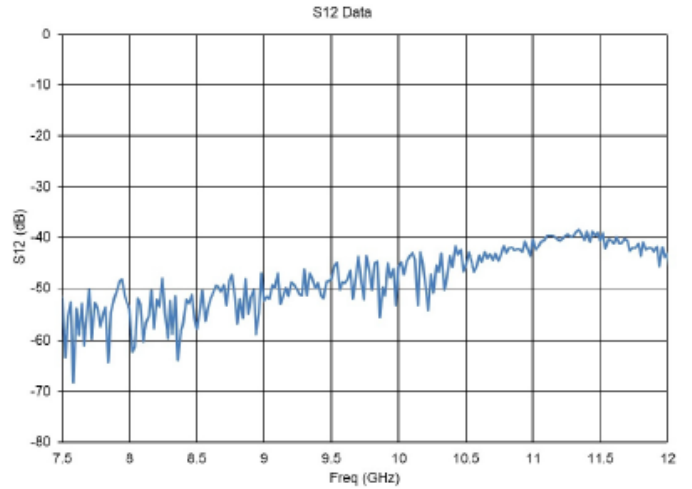
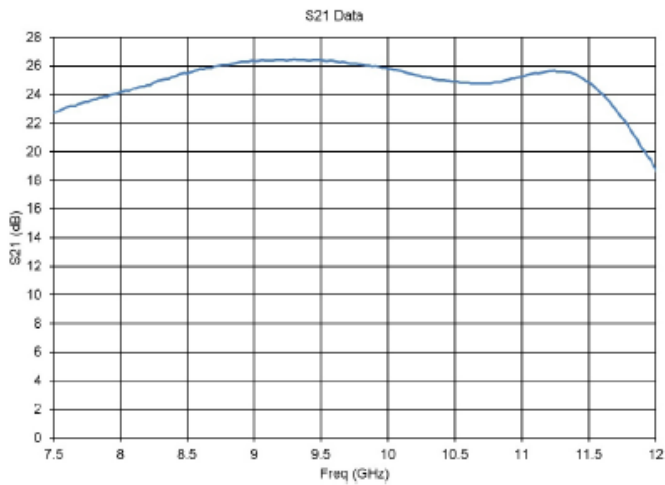
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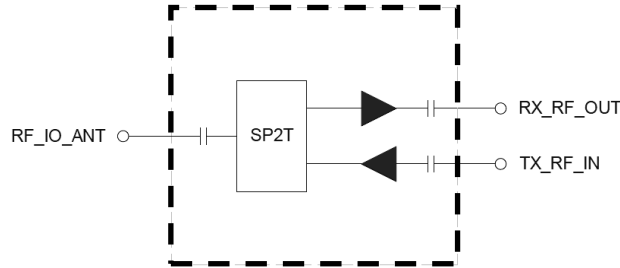
Typical Performance @ +25°C - Transmit Mode

Small Signal Gain, Reverse Isolation, Input/Output Return Loss:

VD1_PA = VD2_PA = +28 V, SW_V0 = -20 V, SW_V1 = +5 V, TX Idq = 200 mA, VG1_PA = VG2_PA = -1.8 V



RF Block Diagram

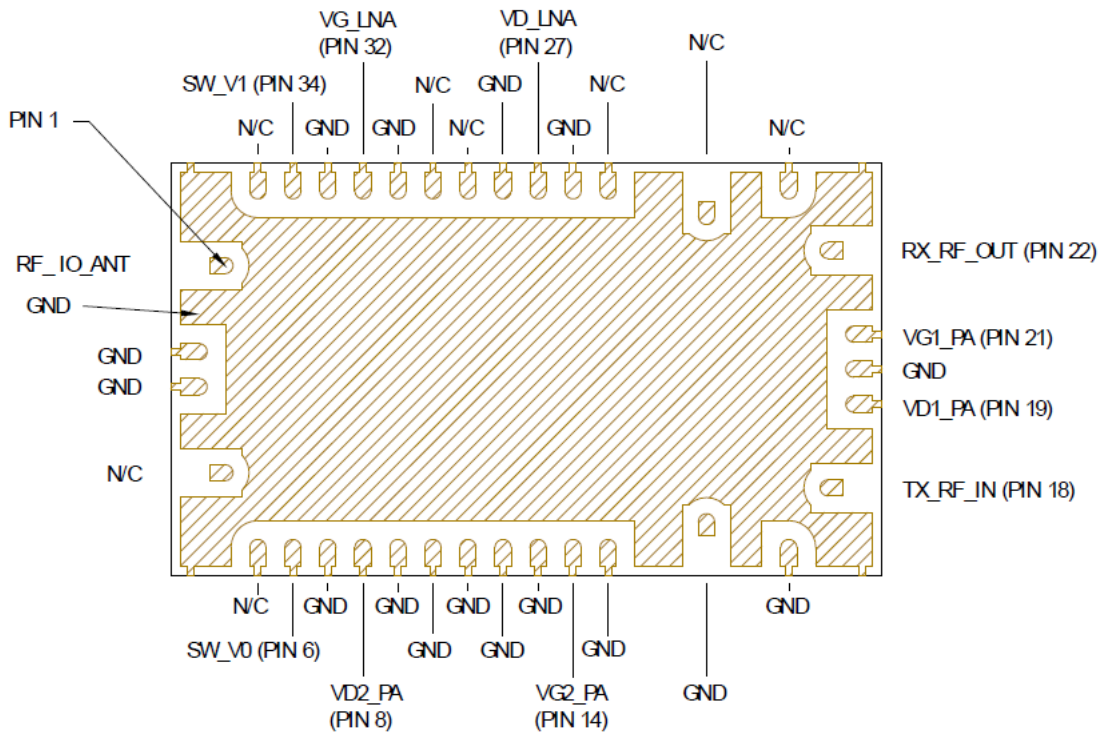


Notes:

All RF Ports are AC coupled.

Add 4.7 μ F to 10 μ F capacitor to gate and drain lines if power supply capacitors are greater than 4 inches away at the next assembly.

Pinout Configuration



Package Bottom As Seen Through The Top Cover

T/R Module Biasing Procedure

To prevent inadvertent damage to the T/R module, the following bias procedure is recommended.

RX Mode Bias Up Procedure

1. Set +3.5 V power supply current limit to 0.15 A
2. Set SW_V0 = +5 V, SW_V1 = -20 V
3. Apply -1.5 V to VG_LNA
4. Apply +3.5 V to VD_LNA
5. Adjust VG_LNA to set LNA Idq = 100 mA
6. Turn on RF signal

RX Mode Bias Down Procedure

1. Turn off RF signal
2. Set VD_LNA to 0 V
3. Set VG_LNA to 0 V

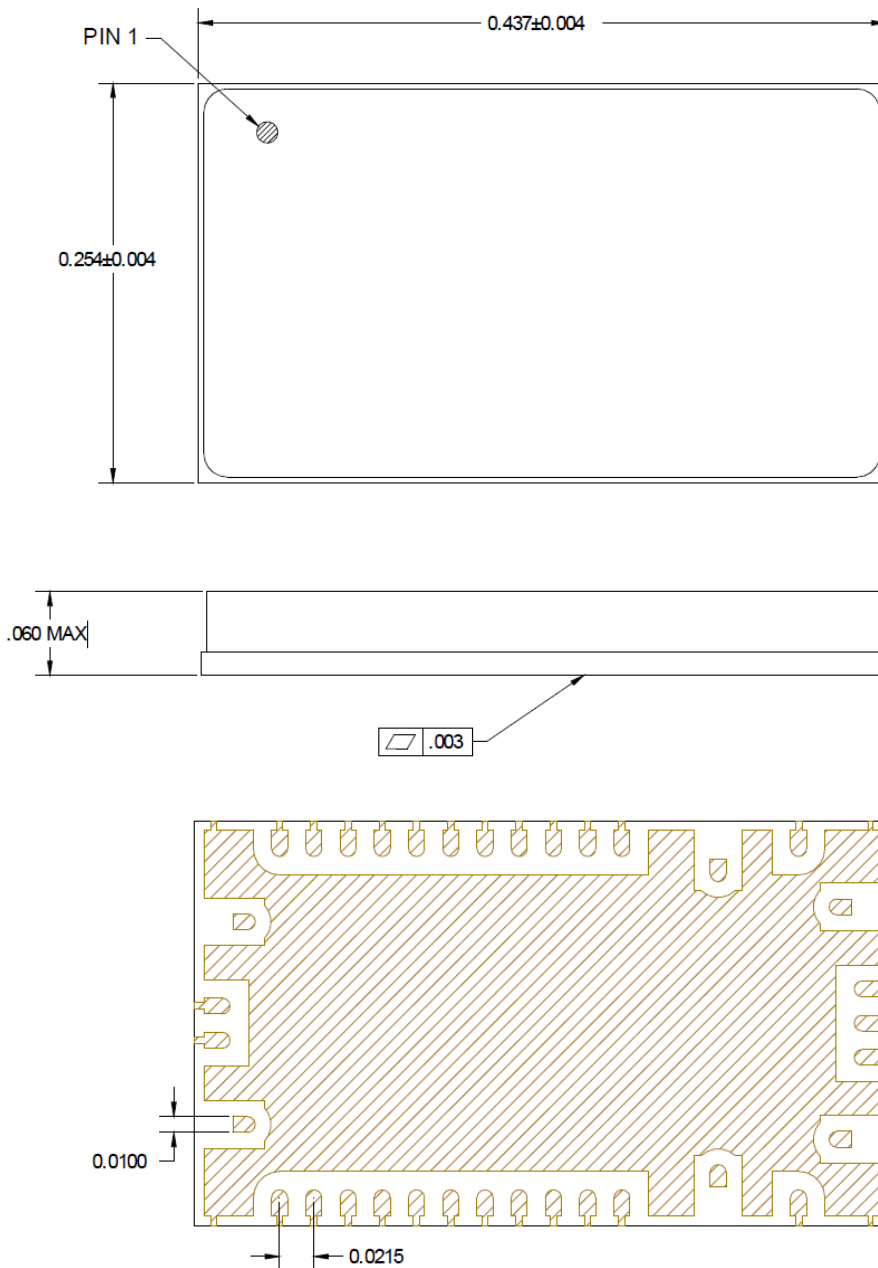
TX Mode Bias Up Procedure

1. Set +28 V power supply current limit to 0.40 A
2. Set SW_V0 = -20 V, SW_V1 = +5 V
3. Apply -5 V to VG1_PA and VG2_PA
4. Apply +28 V to VD1_PA and VD2_PA
5. Adjust VG1_PA and VG2_PA to set PA Idq = 200 mA
6. Turn on RF signal

TX Mode Bias Down Procedure

1. Turn off RF signal
2. Set VD1_PA and VD2_PA to 0 V
3. Set VG1_PA and VG2_PA to 0 V

Outline Drawing



Notes (unless otherwise specified):

1. Pads gold plated 40-60 microinches AU PER MIL-G- 45204 TYPE III
2. Do not exceed 280°C processing temperature
3. Final package gross leak hermetic. Optional fine leak hermetic to 1.0×10^{-7} ATM CC/EC AIR if requested
4. Contact factory for recommended board footprint

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