15 dB Gain pHEMT Low Noise Amplifier, DIE
2 - 18 GHz

ENGLA00263A

Rev. V1

Features

- Operation Across 2 - 18 GHz
- Small Signal Gain: 15 dB
- Noise Figure: 1.9 - 4.1 dB
- I/O Return Loss: 11.8 dB
- IM3: -42 dBm @ mid band
- Positive Gate Supply Voltage
- Die Size:
  - 2.65 x 1.73 x 0.1 mm
  - 4.58 sq. mm
  - 0.104 x 0.068 inch
- RoHS* Compliant

Applications

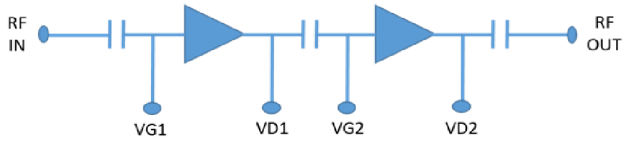
- Wideband EW / Radar / SATCOM, and Weather Radar Application
- Radio Transmitters when biased for linearity
- Test & Measurement Systems

Description

The ENGLA00263A is a wideband pHEMT two-stage 15-dB gain low noise amplifier, operating across 2 to 18 GHz. The design is 50-ohm matched. The amplifier has a typical noise figure of 1.9 - 4.1 dB across 2. to 18.0 GHz. The amplifier has gold backside metallization and is designed for gold-tin eutectic or high thermal conductivity silver epoxy attachment.

Functional Block Diagram

MMIC RF ports are DC-blocked. RF ports designed for 50 ohms.



Ordering Information

Part Number	Package
ENGLA00263A	Die

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications:

Freq. = 2 - 18 GHz, T_A = +25°C, VD = 3.0 V; IDQ = 34 mA (Iq), VG ~ +0.49, 0.66 V

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Small Signal Gain	—	dB	14	15	—
Noise Figure	—	dB	—	1.9 - 4.1	3.0 - 5.0
Input Return Loss	—	dB	11	14	—
Output Return Loss	—	dB	10	12	—
IM3	—	dBm	—	-42	-38
OP1dB	10 dB @ 10 GHz	dBm	6	8, 10, 12	—
Supply Current	—	mA	—	34	40
Thermal Resistance	includes 25-µm thick AuSn T_B = 90°C	ºC/W	—	490	—

Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Units
Drain Voltage	—	3	4	V
Gate Voltage	0 = pinch-off	0.49, 0.66	0.8	V
Quiescent Drain Current	—	34	44	mA

Absolute Maximum Ratings[1,2]

Parameter	Absolute Maximum
Drain Voltage	5.5 V
Gate Voltage	1 V
RF Input Power	20 dBm
Operating Temperature	-55°C to +100°C
Storage Temperature	-65°C to +150°C

1. Exceeding any one or combination of these limits may cause permanent damage to this device.
2. MACOM does not recommend sustained operation near these survivability limits.

Handling Procedures

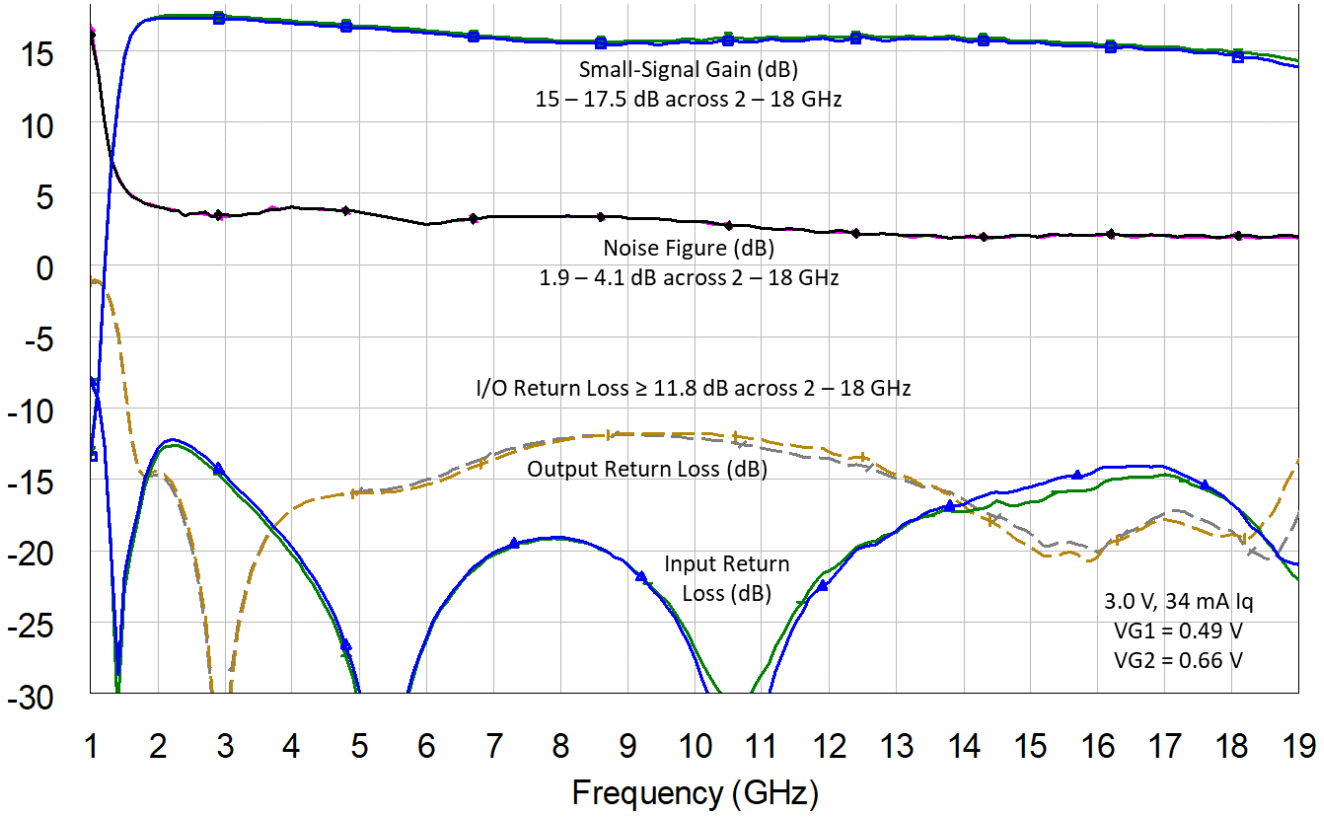
Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

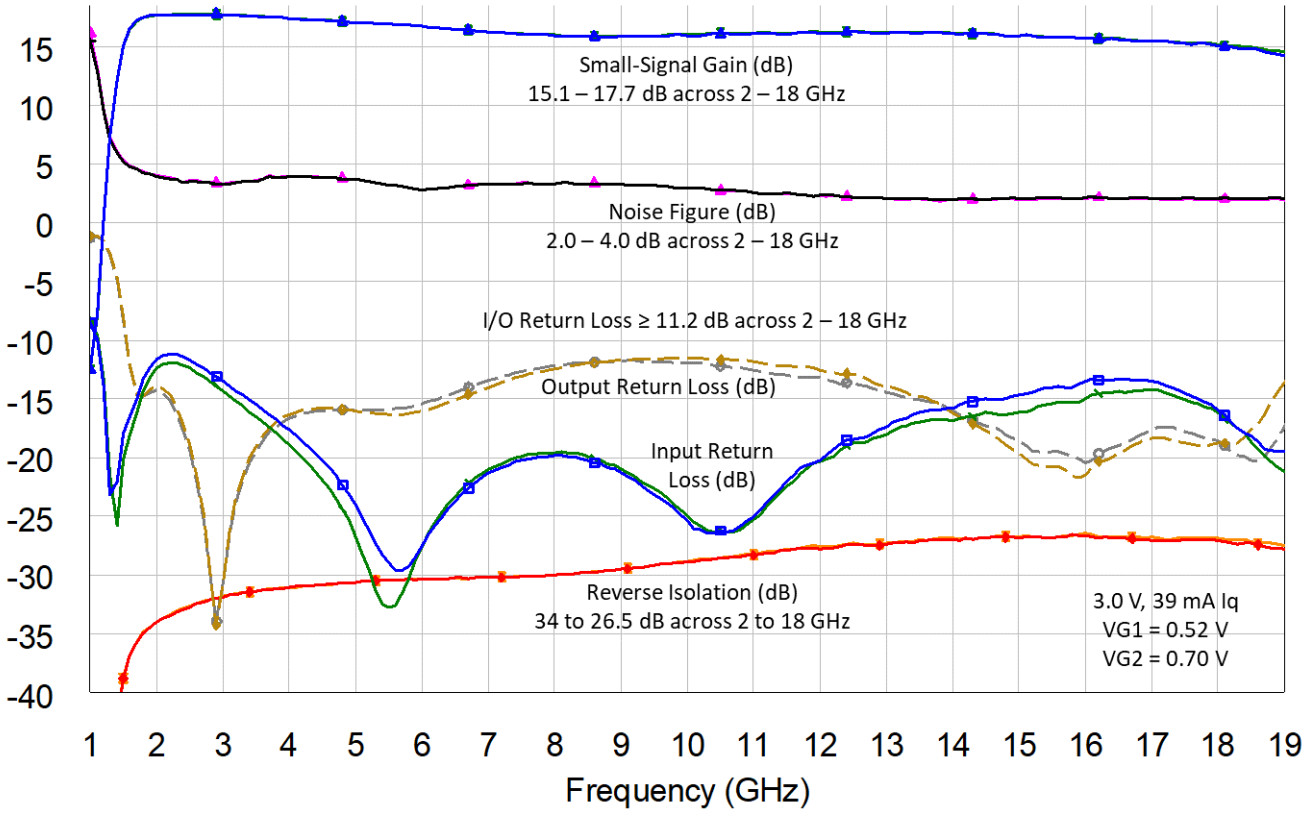
Measured RF Data: With Wirebonds and External Microstrip Flares

Small Signal Gain, Noise Figure and In / Out Return Loss (for two ENGLA00263A amplifiers):
T = 25 ºC, 3 V, 34 mA



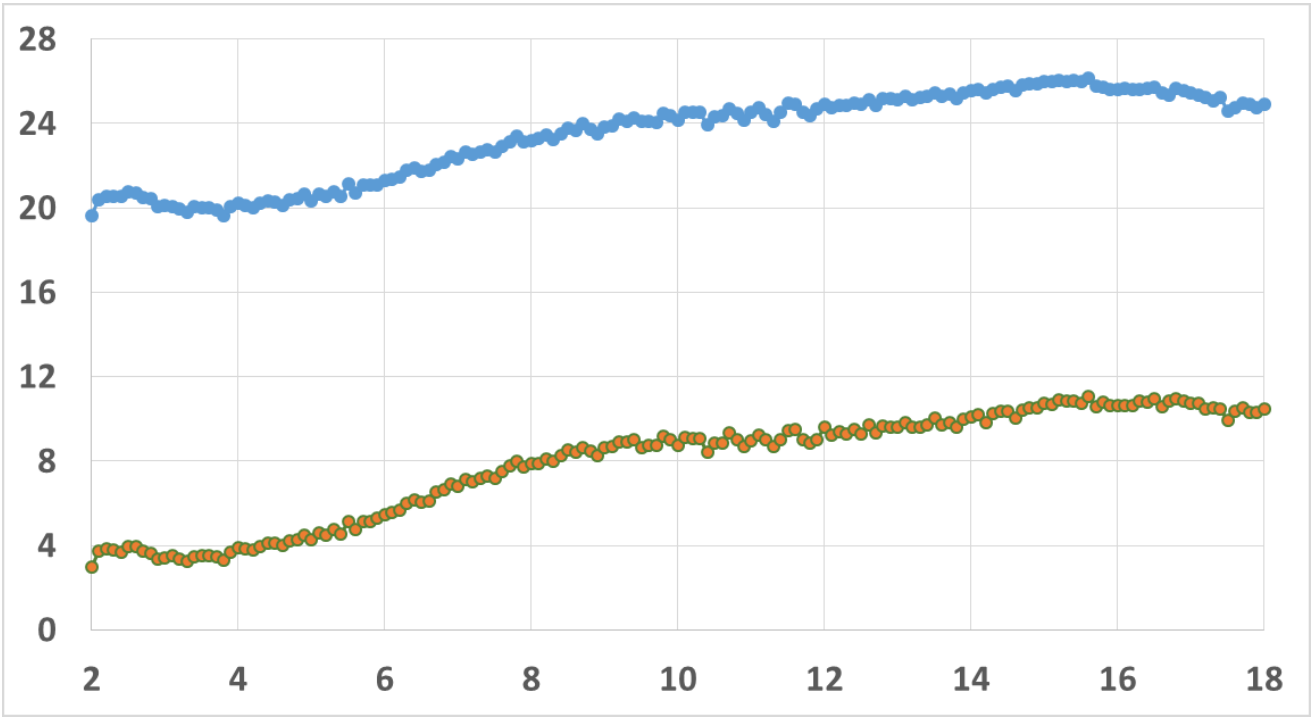
Measured RF Data: With Wirebonds and External Microstrip Flares

Small Signal Gain, Noise Figure and In / Out Return Loss (for two ENGLA00263A amplifiers):
T = 25 ºC, 3 V, 39 mA



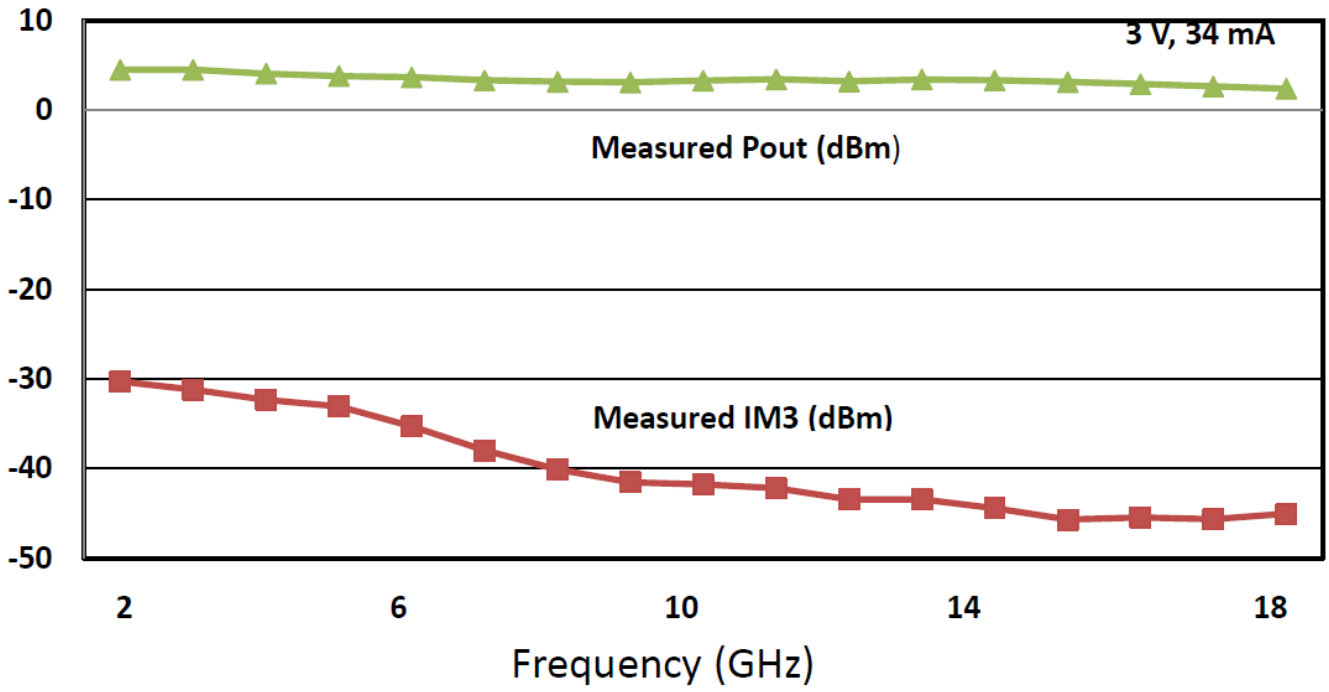
Measured RF Data: With Wirebonds and External Microstrip Flares

Input / Output Third-Order Intermodulation Distortion: T = 25 ºC, 3 V, 34 mA



Measured RF Data: With Wirebonds and External Microstrip Flares

Output Power / IM3: T = 25 °C, 3 V, 34 mA

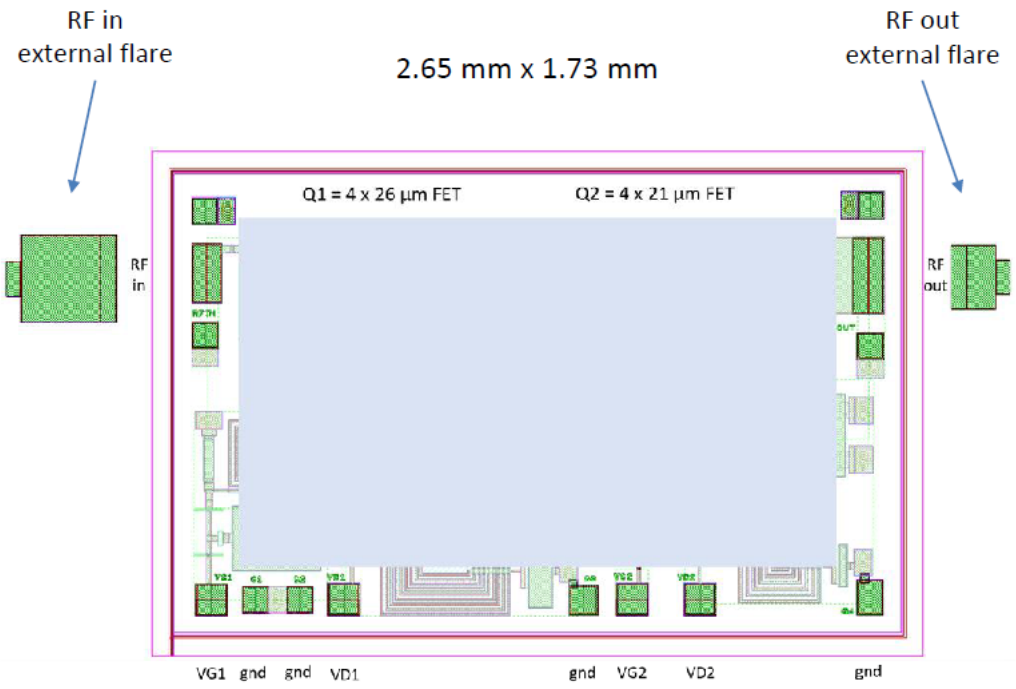


Measured RF Data: With Wirebonds and External Microstrip Flares

S-Parameters: T = 25 °C, 3 V, 34 mA

	S11		S21		S12		S22	
Freq	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
(GHZ)	(DB)	(deg)	(DB)	(deg)	(DB)	(deg)	(DB)	(deg)
1	-8.19	163.59	-13.39	-61.30	-69.44	19.83	-1.12	-67.71
2	-12.81	-159.69	17.27	96.12	-33.56	-157.76	-14.40	-102.28
3	-14.74	135.92	17.24	-12.51	-31.47	92.61	-35.94	54.33
4	-19.78	108.26	16.91	-82.27	-30.73	29.83	-17.12	-8.79
5	-29.79	96.36	16.60	-138.70	-30.34	-16.08	-16.00	-26.94
6	-26.05	-162.97	16.27	170.81	-30.09	-54.91	-15.41	-32.38
7	-20.13	172.23	15.84	124.60	-29.98	-88.87	-13.59	-44.11
8	-19.07	142.22	15.55	81.85	-29.81	-118.92	-12.31	-66.42
9	-21.04	109.56	15.52	40.12	-29.37	-147.63	-11.80	-93.43
10	-27.67	66.15	15.57	-0.85	-28.73	-176.39	-11.81	-125.23
11	-31.40	-72.49	15.70	-43.93	-28.28	154.48	-12.26	-162.00
12	-22.20	-124.42	15.77	-85.44	-27.76	124.70	-13.08	160.72
13	-18.61	-147.99	15.78	-128.98	-27.39	96.05	-14.64	125.13
14	-16.78	-169.37	15.70	-171.91	-27.03	65.00	-16.89	96.04
15	-15.50	174.41	15.56	143.34	-26.90	35.47	-19.71	88.70
16	-14.30	158.26	15.31	100.24	-26.75	4.13	-20.45	101.23
17	-14.14	132.65	15.09	53.83	-27.13	-26.88	-17.82	96.73
18	-16.64	109.60	14.71	6.60	-27.14	-60.69	-18.91	100.91
19	-20.98	117.34	13.86	-46.04	-27.89	-97.25	-13.74	132.95

MMIC Assembly Drawing:
50-ohm microstrip line with on 5-mil alumina: 120 µm

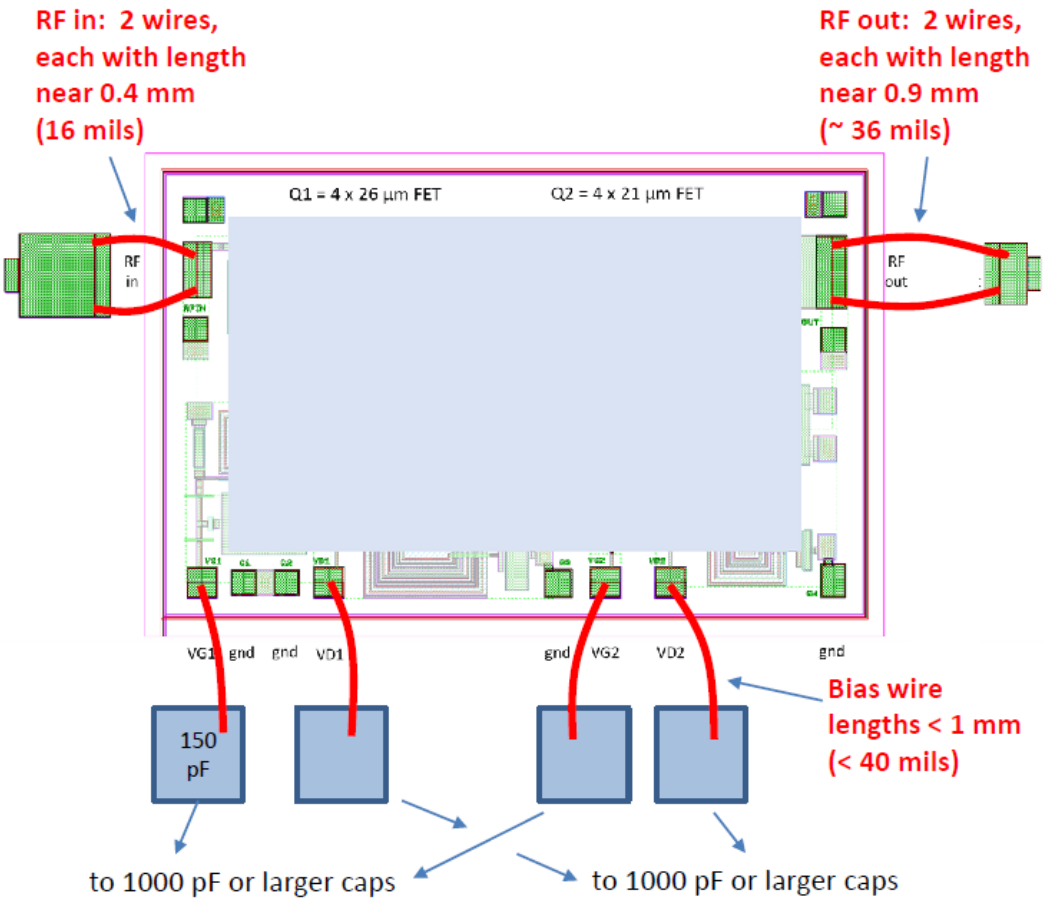


RF In: 320 µm (*x*) x 300 µm (*y*)
RF Out: 156 µm (*x*) x 221 µm (*y*)

Assembly Comments

1. If mounting the MMIC using either AuSn solder, or high thermal conductivity silver epoxy, the regions underneath the FET heat sources should be void free. Even small voids underneath the FETs could cause FET channel temperature to significantly increase.
2. RF ports are DC blocked.
3. RF I/O port impedances are near 50 ohms.

MMIC Assembly Drawing: Bond Wire Interconnects

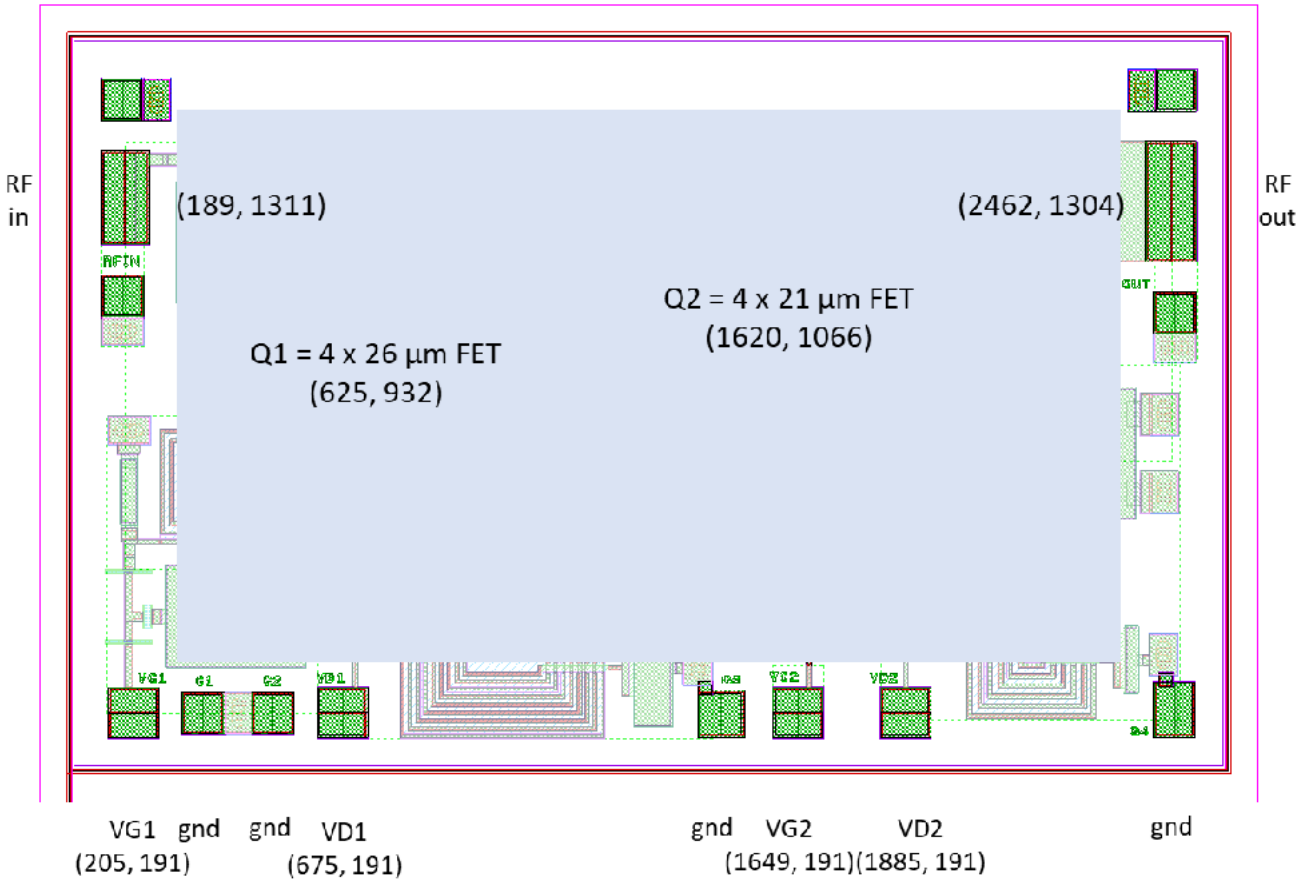


Gold wire diameter: 25.4 µm (1 mil)

Ceramic bypass capacitors: 150 pF
(>100 pF over temperature)

Outline Drawing – MMIC Dimensions: 2.65 mm x 1.73 mm

Center coordinates of bond pads and FETs are noted as (x, y µm)
RF I/O pads are 100 µm x 200 µm in dimension or larger
Gate and Drain bias pads are 100 µm x 100 µm in dimension or larger



Notes:
1. All dimensions are given in micrometers (µm) unless specified. Typ. tolerance: +25 µm / -25 µm.
2. SiC thickness (excluding front side/back side metallization): 75 µm. Typical tolerance +/- 8 µm.
3. Backside metallization is gold.
4. Bond pad metallization is gold.