Wideband High Gain Low Noise Amplifier, DIE
2 - 18 GHz

ENGLA00183A
Rev. V1

Features

- High Gain: 30 - 33 dB
- Low Noise Figure: 2.7 dB
- Positive Gain Slope
- Good I/O Return Loss: 15 / 12 dB
- Die Size:
  3.18 x 1.65 x 0.1 mm
  0.125 x 0.065 x 0.004 inch
- RoHS* Compliant

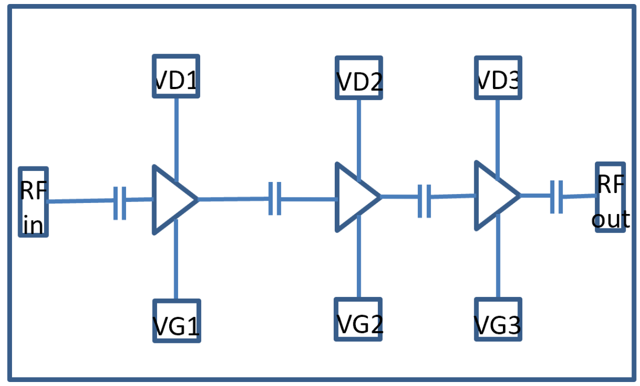
Applications

- Military & Commercial SATCOM
- Obsolescence Replacement
- Receiver or Transmitter
- Telecom Infrastructure
- Space Hybrids
- Test & Measurement Systems

Description

The ENGLA00183A is a Wideband High Gain Low noise Amplifier (LNA) operating across 2 to 18 GHz. The design is 50 ohm matched and includes on board bias circuitry. The amplifier offers 30 dB gain with 3 dB positive gain slope to overcome high frequency roll–off due to interconnect losses; 2.7 dB de-embedded noise figure; and greater than 25 dBm output third-order intercept point (OIP3) across the band, at room temperature. The MMIC has gold backside metallization and is designed to be silver epoxy or gold-tin solder attached. The RF interconnects are designed to account for wire bonds to external 50 ohm microstrip lines for optimal integrated return loss. No additional ground interconnects are required.

Functional Block Diagram



Ordering Information

Part Number	Package
ENGLA00183A	Die

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications:

Freq. = 2 - 18 GHz, T_A = +25°C, *VD = 3.3 V; ID total = 237 mA*
VG1 = -0.12 V, ID1 = 114 mA, VG2 = -0.08 V, ID2 = 63 mA, VG3 = -0.08 V, ID3 = 60 mA

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	—	dB	29	32	33
Noise Figure	De-embedded Input Loss	dB	—	2.7	3.3
Input Return Loss	—	dB	—	15	—
Output Return Loss	—	dB	—	12	—
Output P1dB	—	dBm	—	18	—
Output IP3	—	dBm	23	27	—
Supply Current	—	mA	—	237	—
Thermal Resistance	Channel to MMIC Backside; Backside @ 100°C	ºC/W	—	78	—

Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Units
Drain Voltage	3.0	3.3	3.6	V
Gate Voltage	-0.25	-0.12	-0.06	V
Drain Current	—	237	—	mA

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

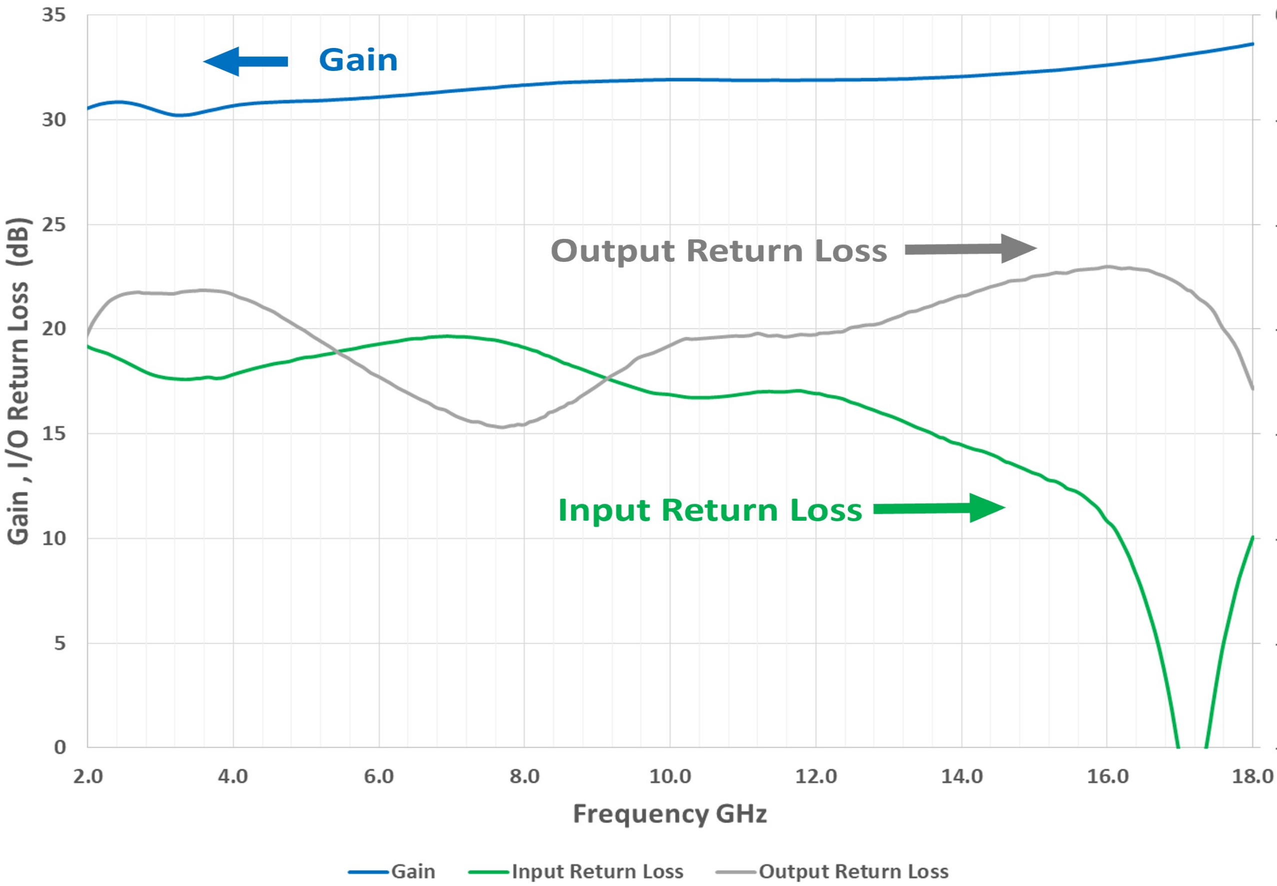
Absolute Maximum Ratings[1,2]

Parameter	Absolute Maximum
Drain Voltage	5 V
Gate Voltage	-2 V
RF Input Power	17 dBm
Junction Temperature	+170°C
Operating Temperature	-55°C to +100°C
Storage Temperature	-65°C to +150°C

1. Exceeding any one or combination of these limits may cause permanent damage to this device.
2. MACOM does not recommend sustained operation near these survivability limits.

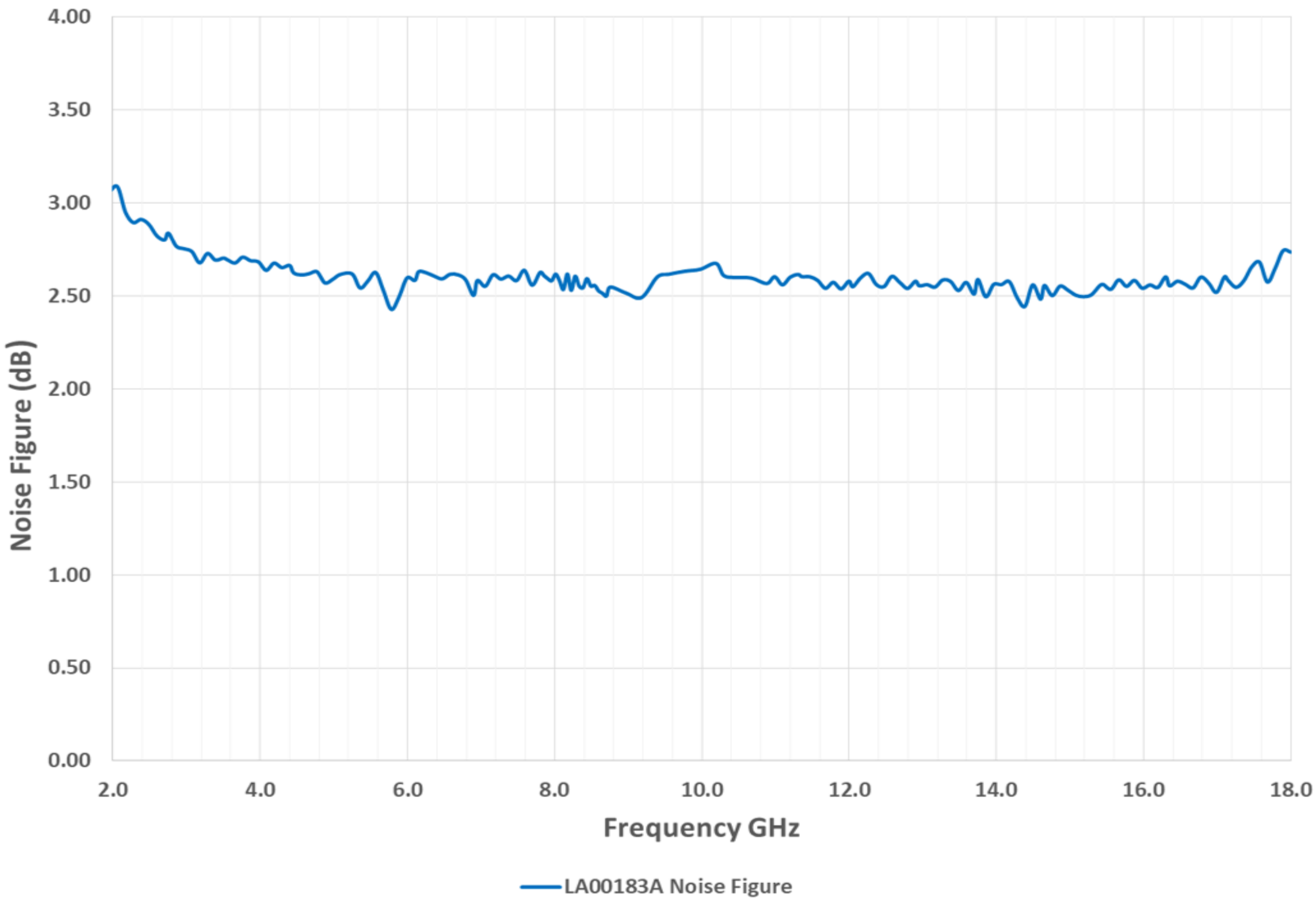
Measured RF Data: With Wirebonds and External 50 Ω Line

Gain and In / Out Return Loss: T = 25 ºC, VD = 3.3 V; ID total = 237 mA
VG1 = -0.12 V, ID1 = 114 mA, VG2 = -0.08 V, ID2 = 63 mA, VG3 = -0.08 V, ID3 = 60 mA



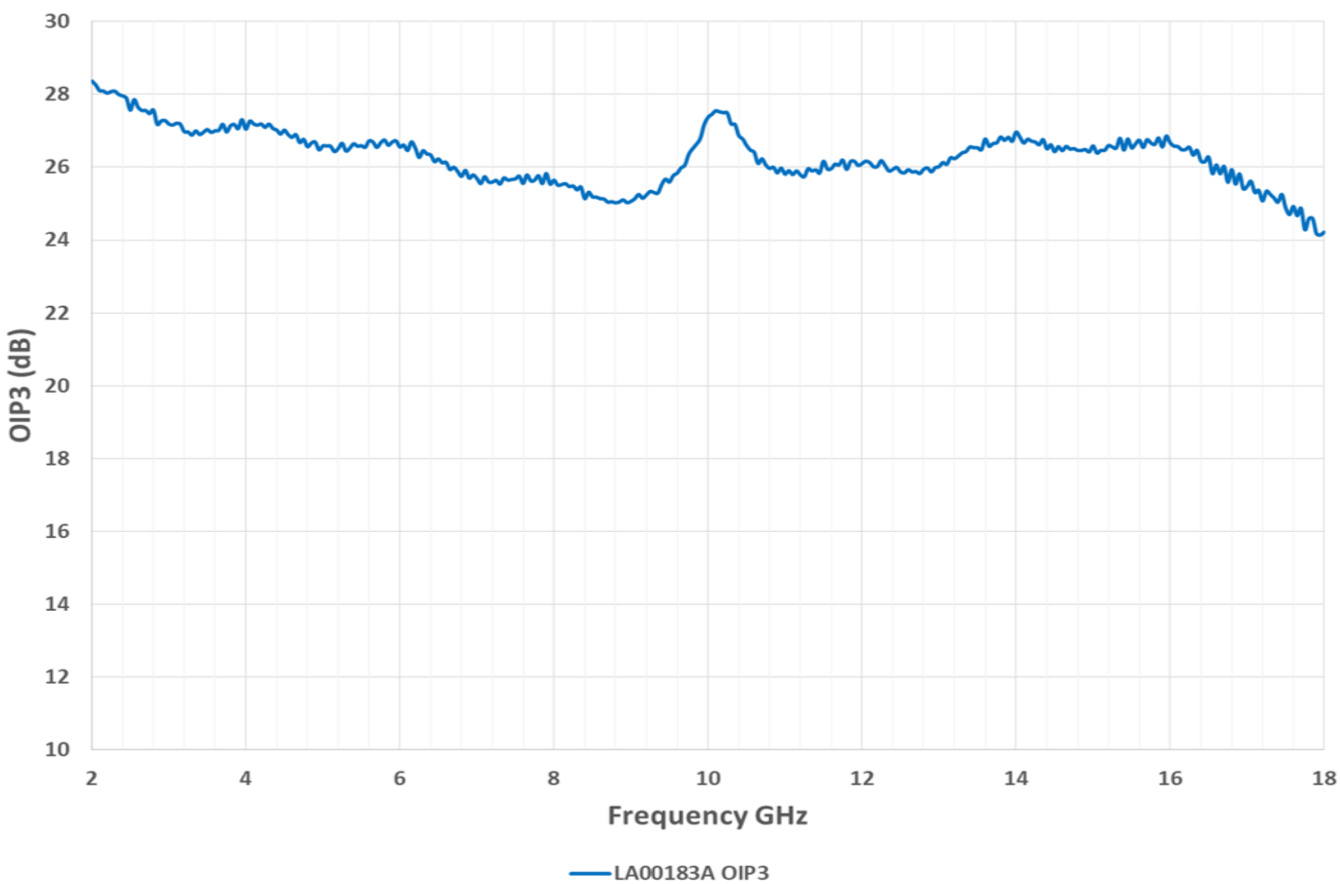
Measured RF Data: With Wirebonds to External 50 Ω Microstrip Lines

Noise Figure: T = 25 ºC, VD = 3.3 V; ID total = 237 mA
VG1 = -0.12 V, ID1 = 114 mA, VG2 = -0.08 V, ID2 = 63 mA, VG3 = -0.08 V, ID3 = 60 mA
(De-embedded Input Loss)



Measured RF Data: With Wirebonds to External 50 Ω Microstrip Lines

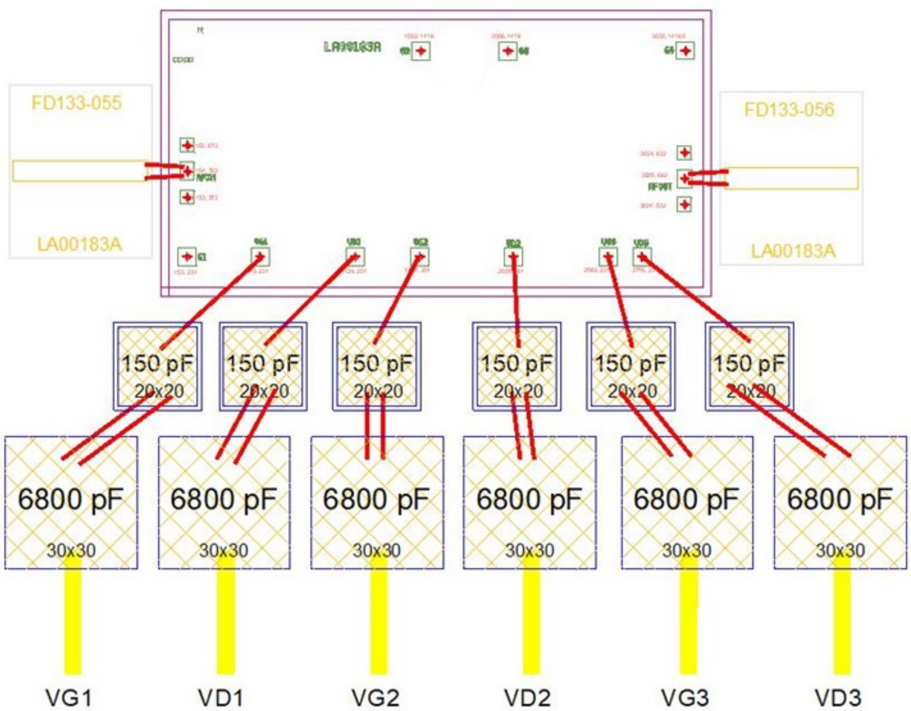
Output Third-Order Intercept: T = 25 ºC, VD = 3.3 V; ID total = 237 mA
VG1 = -0.12 V, ID1 = 114 mA, VG2 = -0.08 V, ID2 = 63 mA, VG3 = -0.08 V, ID3 = 60 mA



External I/O Microstrip Flare Dimensions (on 5-mil Alumina) and I/O Bond Wire Inductances for Optimum Insertion and Return Loss Performance

S-parameters can be supplied at DIE level such that optimal flare dimensions can be made for the substrate connection medium used (if different from 5-mil Alumina).

Pad Flare Dimension	Flare Length x-dim, (µm)	Flare Width y-dim, (µm)	Wire Inductance (nH)	Wire Length (µm)	Wire Length (mils)	# of Wires
RF Input	775	120	0.115	230	9	2
RF Output	775	120	0.115	230	9	2

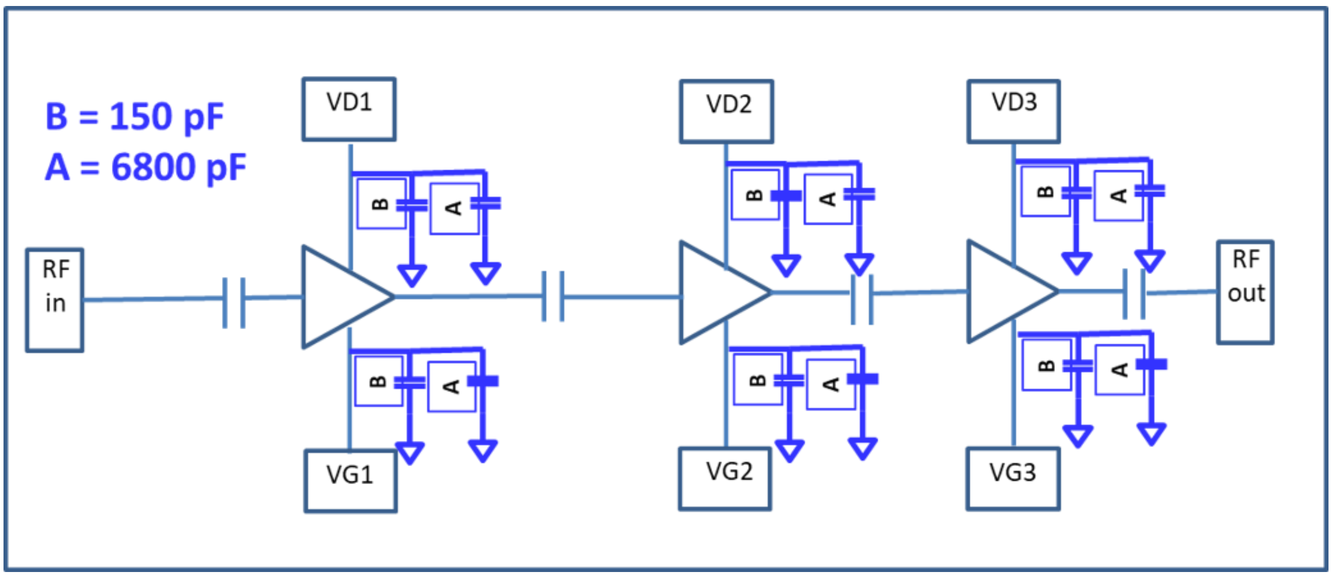


Notes:
1. To achieve bond wire inductance noted, bond the number of wires shown in parallel from each external flare to each associated MMIC RF bond pad as shown above.
2. Gold Wire Details:
   Diameter: 25.4 µm (1 mil)
   Spacing: 4 mils (~ 100 µm) typical
   Height above Ground: 8 mils (~ 200 µm) typical (wedge bonds)
3. Wire Length is total length if the wire were made perfectly straight.

Assembly Guidelines

The backside metallization is RF/DC ground. Attachment should be accomplished with electrically and thermally conductive epoxy, or with gold-tin (AuSn) solder. This device supports high frequency performance. Care should be made to following the wirebond dimensions as shown in the flare diagram.

Application Circuit and Turn-on Procedure



VD1, VD2, VD3 can be combined after bypass capacitors

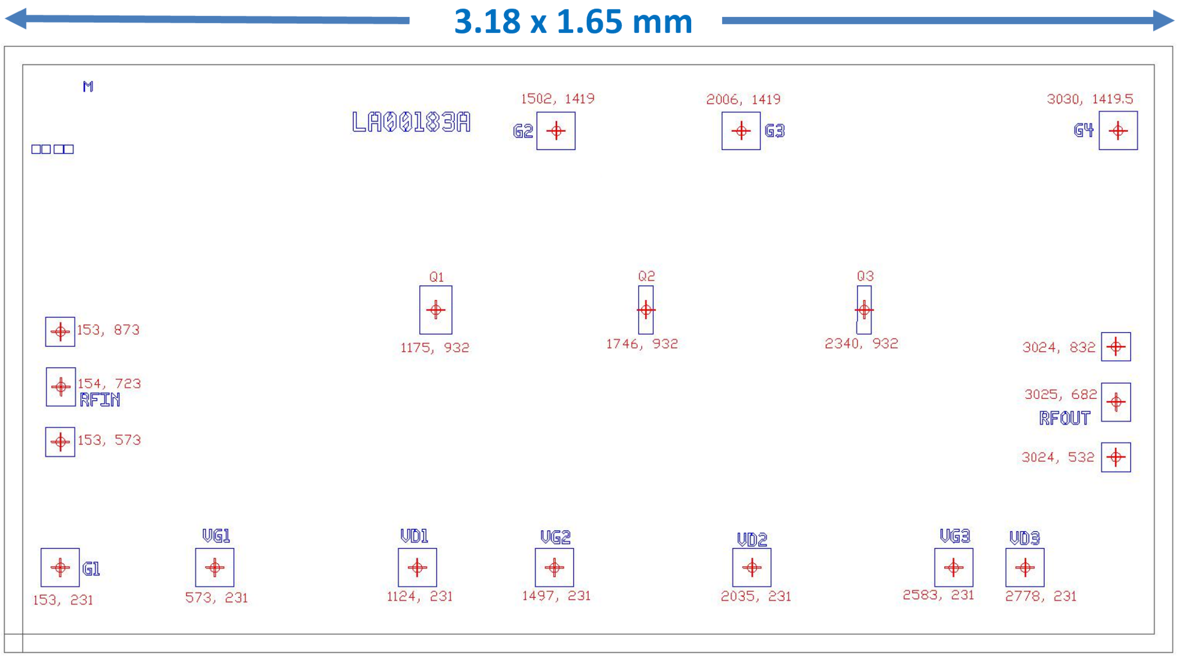
Bias Up Sequence:

1. Set Idd limit to 350 mA
2. Set Gate Voltage (VG) = -2.0 V
3. Set Drain Voltage (VD) = 3.3 V
4. Adjust VG1, VG2, VG3 more positive until target ID1,ID2, ID3
5. Turn ON RF Signal

Bias Down Sequence:

1. Turn OFF RF Signal
2. Reduce VG to -2.0 V , Idd should be 0 mA
3. Reduce VD to 0 V
4. Turn OFF DC Supplies

Outline Drawing



Pad Dimensions

Pad	Pad Description	Length x-dim, (µm)	Width y-dim, (µm)	Length x-dim, (mils)	Width y-dim, (mils)
RFIN	RF input (port 1)	154	723	6.1	28.5
VG1	VG1 stage 1 gate bias	573	231	22.6	9.1
VD1	VD1 stage 1 drain bias	1124	231	44.3	9.1
VG2	VG2 stage 2 gate bias	1497	231	58.9	9.1
VD2	VD2 stage 2 drain bias	2035	231	80.1	9.1
VG3	VG3 stage 3 gate bias	2583	231	101.7	9.1
VD3	VD3 stage 3 drain bias	2778	231	109.4	9.1
RFOUT	RF output (port 2)	3025	682	119.1	26.9
G1	GND1	153	231	6.0	9.1
G2	GND2	1502	1419	59.1	55.9
G3	GND3	2006	1419	79.0	55.9

Notes:
All dimensions are given in both µm and mils.
Substrate thickness: 100 µm (0.004”).
Backside metallization is gold.
Bond pad metallization is gold.