High Linearity Ka-Band Low Noise Amplifier, DIE 27.0 - 31.5 GHz

ENGLA00100
Rev. V1

Features

- High Linearity: OIP3 = 30 dBm
- Low Noise Figure: 1.5 dB
- Gain: 22 dB, Low Gain Ripple
- Good I/O Return Loss: 17 / 15 dB
- Self-Biased (single supply voltage)
- Die Size:
  3.92 x 1.80 x 0.1 mm
  0.154 x 0.071 x 0.004 inch
- RoHS* Compliant

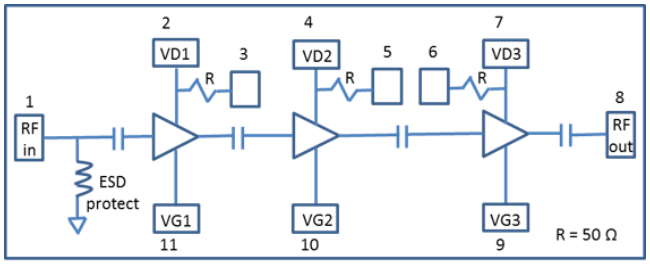
Applications

- Military & Commercial SATCOM
- Obsolescence Replacement
- Receiver or Transmitter
- Telecom Infrastructure
- Space Hybrids
- Test & Measurement Systems

Description

The ENGLA00100 is a high linearity, low noise amplifier (LNA) operating across 27 to 31.5 GHz. The design is 50 ohm matched and includes on board bias circuitry. The amplifier offers 22-dB gain, 1.5 dB noise figure, and 30-dBm output third-order intercept point (OIP3) across the band, at room temperature. The MMIC has gold backside metallization and is designed to be silver epoxy or gold-tin solder attached. The RF interconnects are designed to account for wire bonds and external microstrip flares for optimal integrated return loss. No additional ground interconnects are required.

Functional Block Diagram



Ordering Information

Part Number	Package
ENGLA00100	Die

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications:
Freq. = 27.0 - 31.5 GHz, T_A = +25°C, V_D = 3.3 - 4.5 V, VG = -0.33 V, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	—	dB	19.5	22.0	—
Noise Figure	—	dB	—	1.5	2.1
Input Return Loss	—	dB	12	17	—
Output Return Loss	—	dB	10	15	—
Output P1dB	27 GHz 32 GHz	dBm	9	12 14	—
Output IP3	4.0 - 4.5 V 3.3 V	dBm	24	30 28	—
Output IP2	—	dBm	44	50	—
Supply Current	4.0 - 4.5 V	mA	75	99	130
Thermal Resistance	—	ºC/W	—	98	—

Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Units
Drain Voltage	3.3	4.0	4.5	V
Gate Voltage	-0.45	-0.33	-0.25	V
Drain Current	75	99	130	mA

Absolute Maximum Ratings[1,2]

Parameter	Absolute Maximum
Drain Voltage	5 V
Gate Voltage	-2 V
RF Input Power	17 dBm
Junction Temperature	+165°C
Operating Temperature	-55°C to +100°C
Storage Temperature	-65°C to +150°C

1. Exceeding any one or combination of these limits may cause permanent damage to this device.
2. MACOM does not recommend sustained operation near these survivability limits.

Handling Procedures

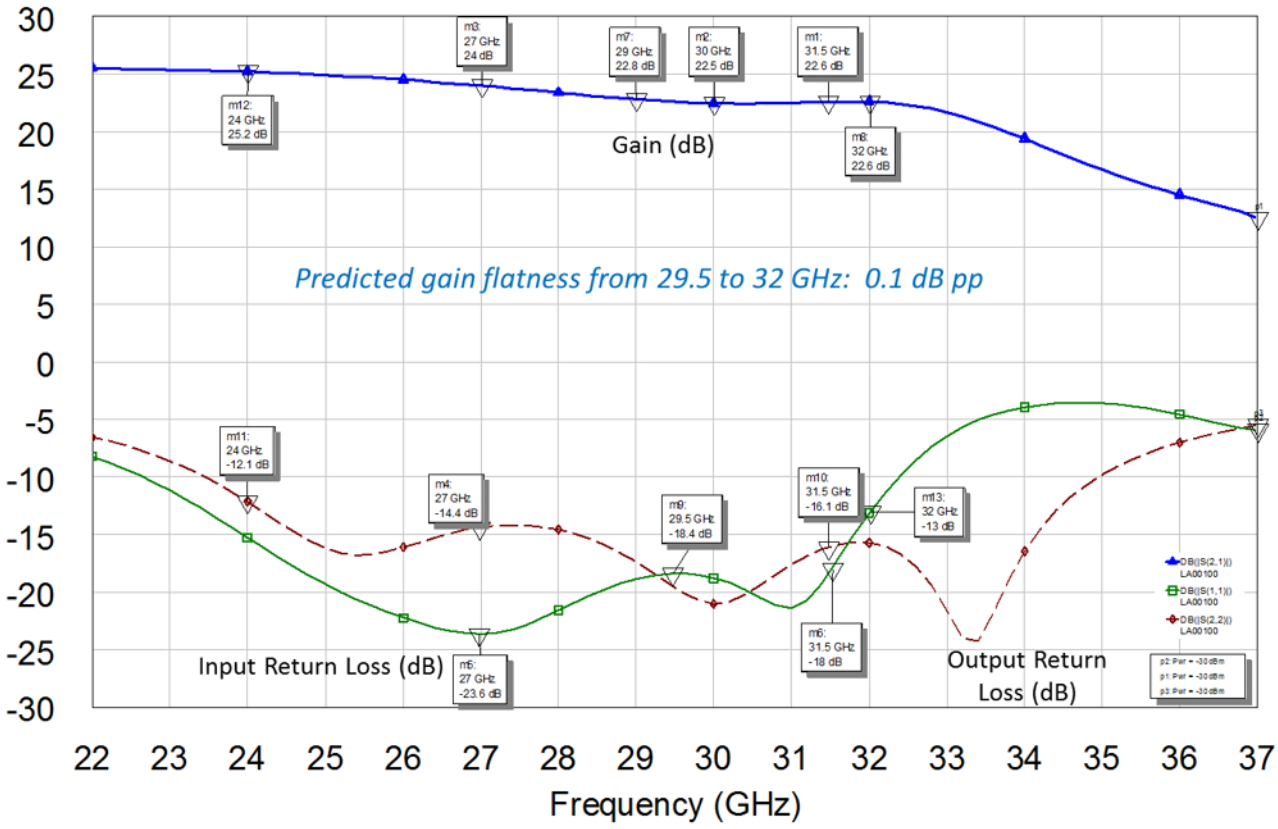
Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

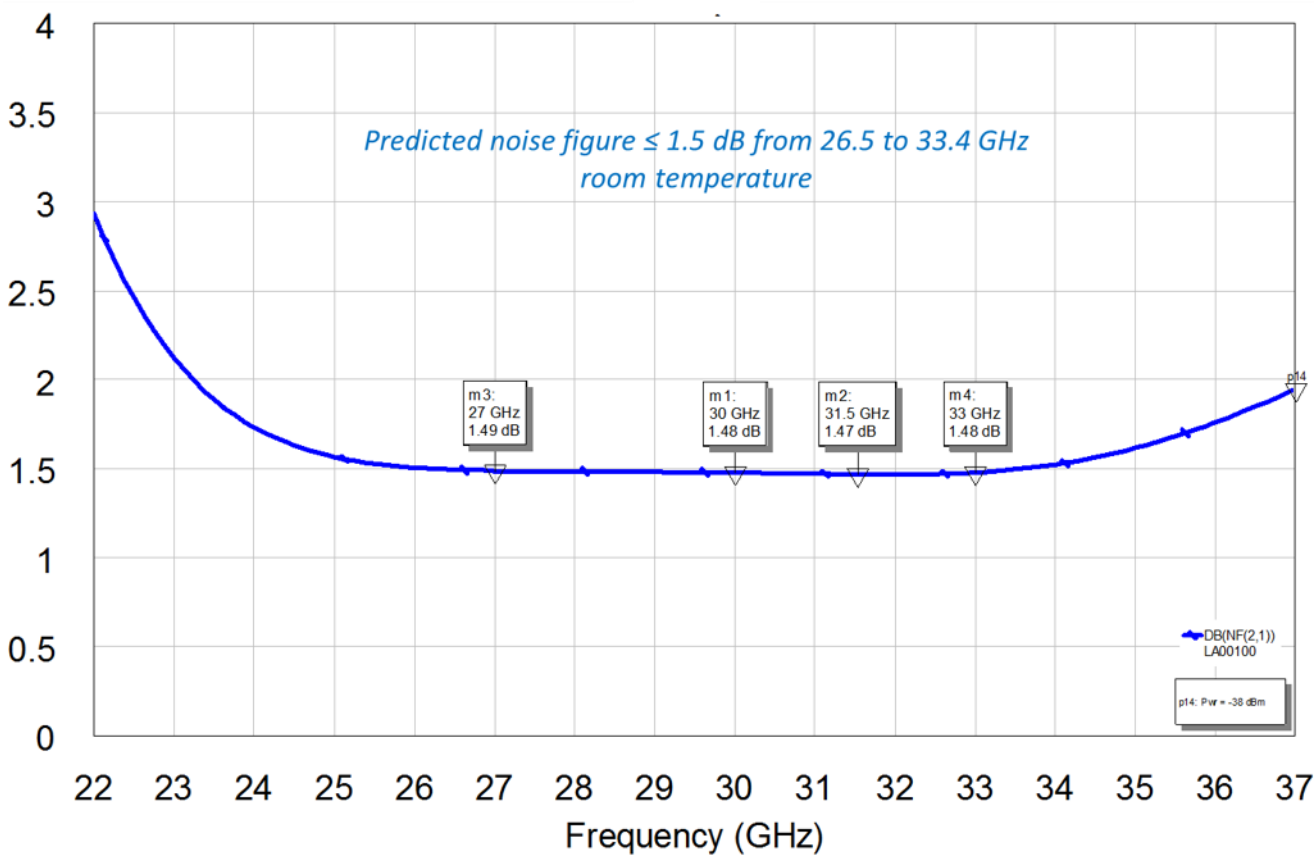
Measured RF Data: With Wirebonds and External Flare Pads

Gain and In / Out Return Loss: V_D = 4 V, V_G = 0.33 V; I_D = 99 mA, T_A = 25°C



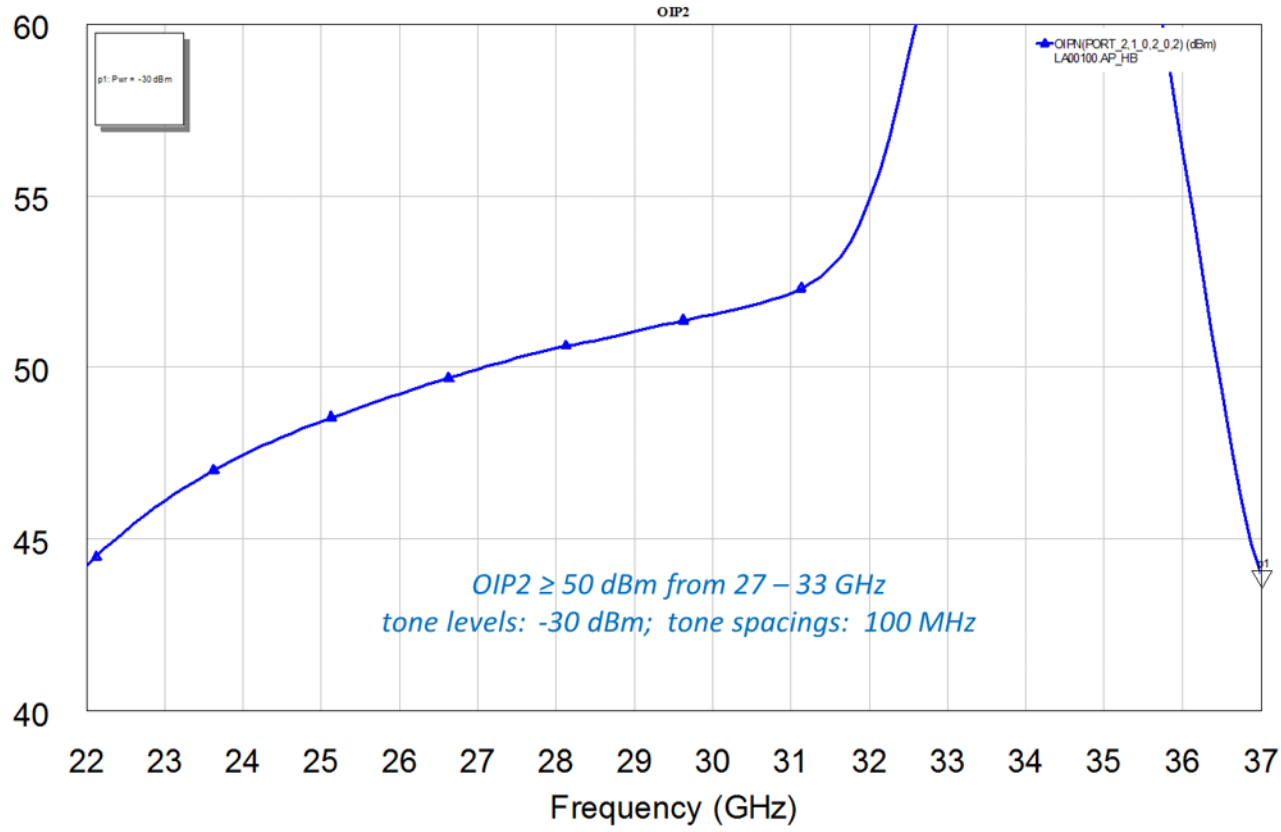
Measured RF Data: With Wirebonds to External 50 Ω Microstrip Lines

Noise Figure: V_D = 4 V, V_G = 0.33 V; I_D = 99 mA, T_A = 25°C



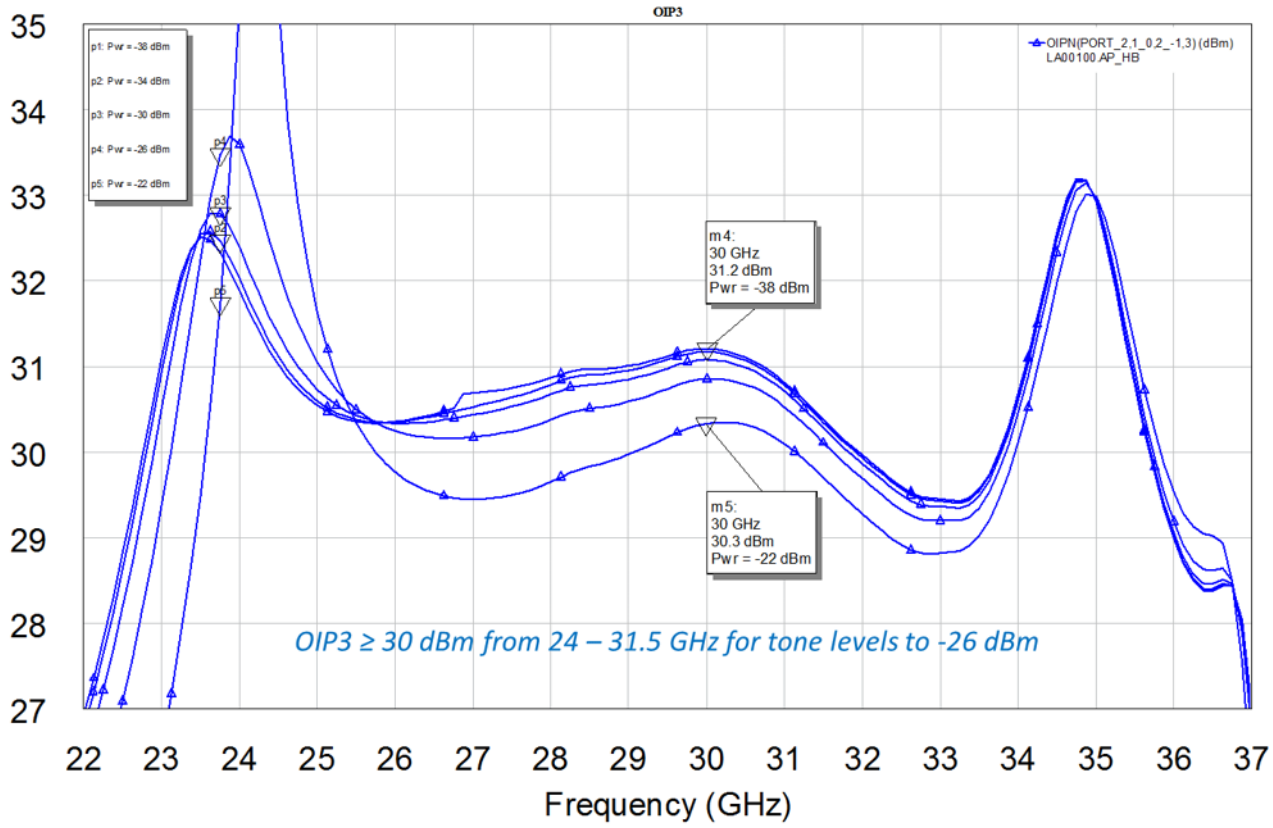
Measured RF Data: With Wirebonds to External 50 Ω Microstrip Lines

Output Second-Order Intercept: V_D = 4 V, V_G = 0.33 V; I_D = 99 mA, T_A = 25°C, 100 MHz spacing, -30 dBm/tone



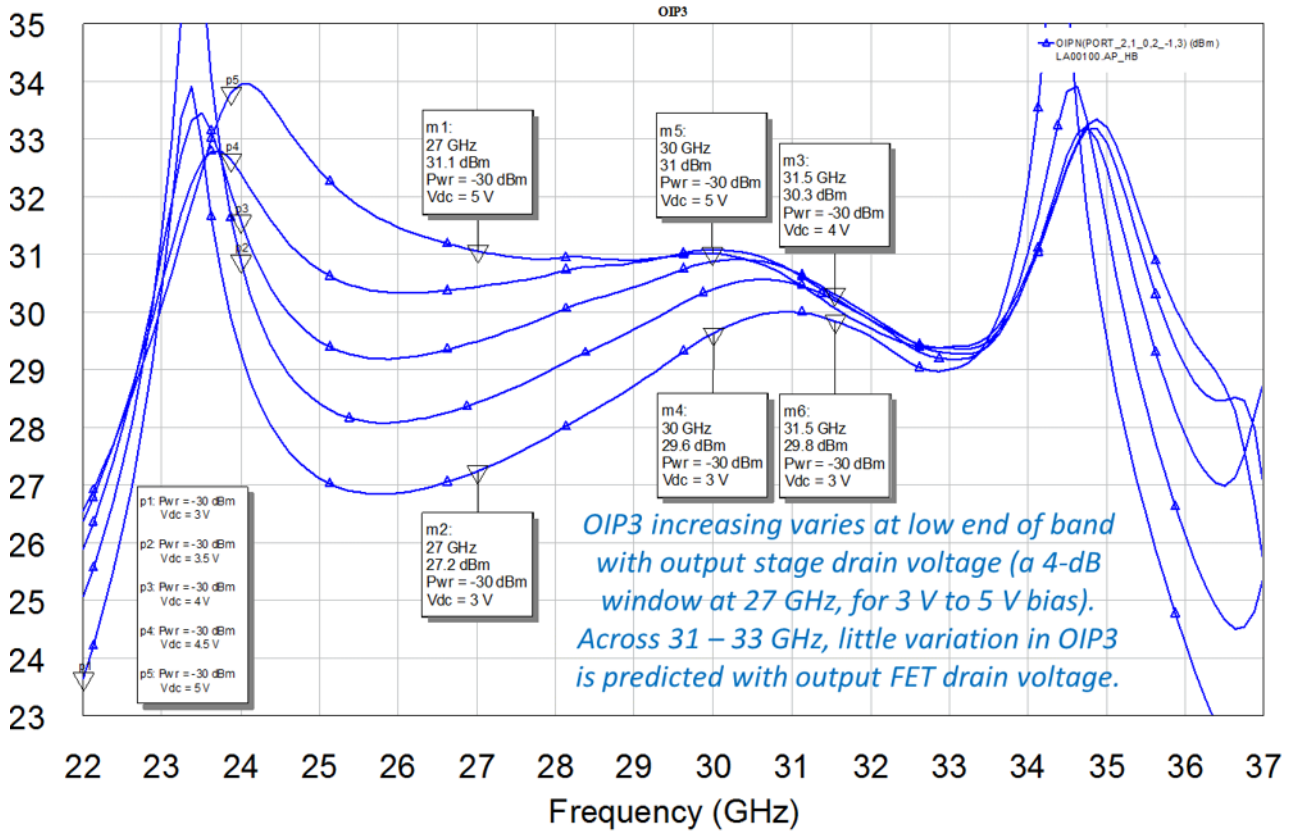
Measured RF Data: With Wirebonds to External 50 Ω Microstrip Lines

Output Third-Order Intercept: V_D = 4 V, V_G = 0.33 V; I_D = 99 mA, T_A = 25°C, 100 MHz spacing, -33 to -22 dBm, in 4 –dB steps



Measured RF Data: With Wirebonds to External 50 Ω Microstrip Lines

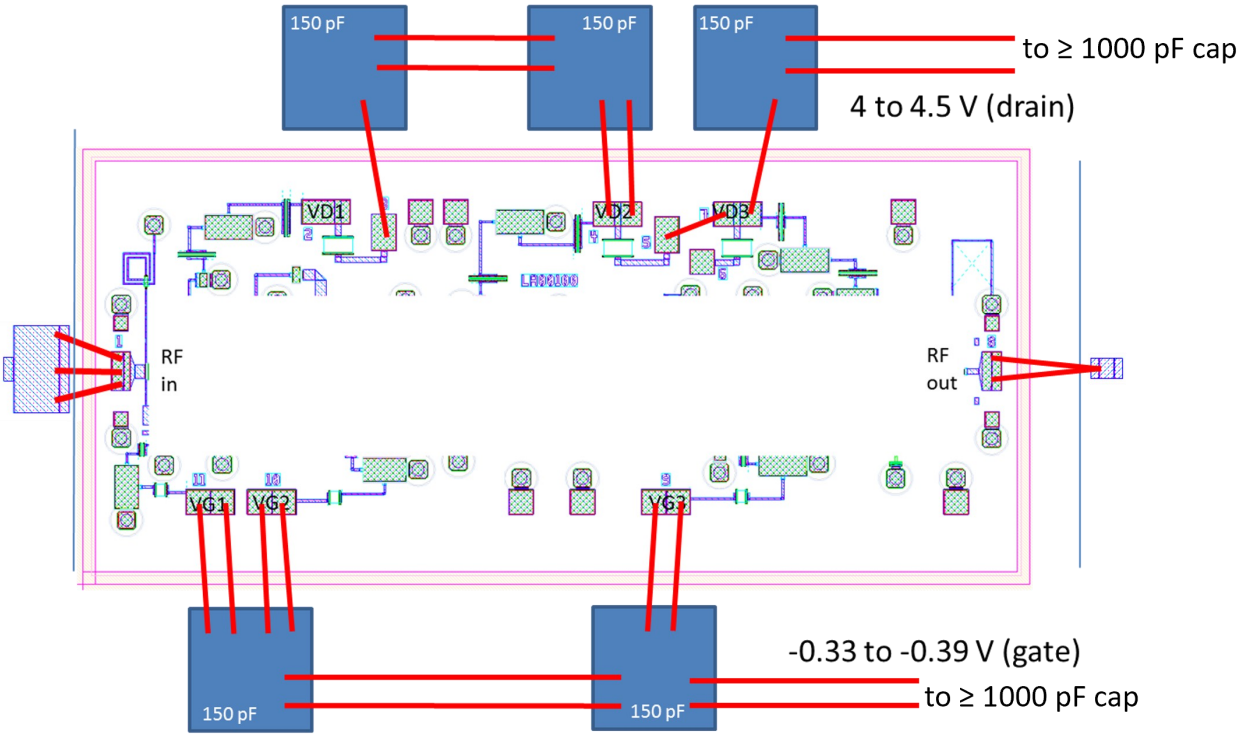
Output Third-Order Intercept: V_D = 4 V, V_G = 0.33 V; I_D = 99 mA, T_A = 25°C,
100 MHz spacing, -30 dBm,
Output transistor drain voltage varied from 3.0 V to 5.0 V in 0.5 V steps



External I/O Microstrip Flare Dimensions (on 5-mil Alumina) and I/O Bond Wire Inductances for Optimum Insertion and Return Loss Performance

S-parameters can be supplied at DIE level such that optimal flare dimensions can be made for the substrate connection medium used (if different from 5-mil Alumina).

Pad Flare Dimension	Flare Length x-dim, (µm)	Flare Width y-dim, (µm)	Wire Inductance (nH)	Wire Length (µm)	Wire Length (mils)	# of Wires
RF Input	280	440	0.07	280	11	3
RF Output	no flare	122	0.21	610	24	2



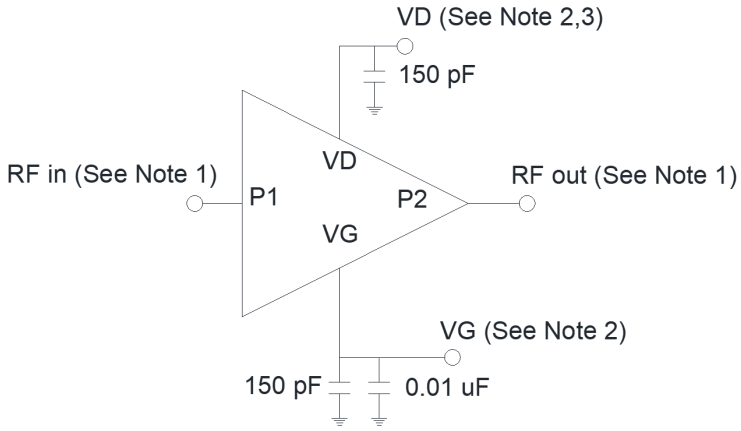
Notes:

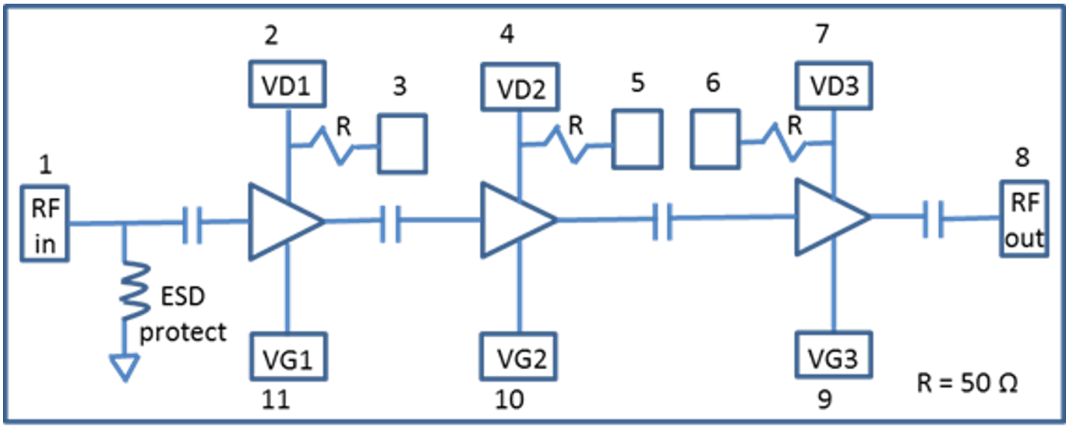
1. To achieve bond wire inductance noted, bond the number of wires shown in parallel from each external flare to each associated MMIC RF bond pad as shown above.
2. Gold Wire Details:
   Diameter: 25.4 µm (1 mil)
   Spacing: 4 mils (~ 100 µm) typical
   Height above Ground: 8 mils (~ 200 µm) typical (wedge bonds)
3. Wire Length is total length if the wire were made perfectly straight.

Assembly Guidelines

The backside metallization is RF/DC ground. Attachment should be accomplished with electrically and thermally conductive epoxy, or with gold-tin (AuSn) solder. This device supports high frequency performance. Care should be made to following the wirebond dimensions as shown in the flare diagram.

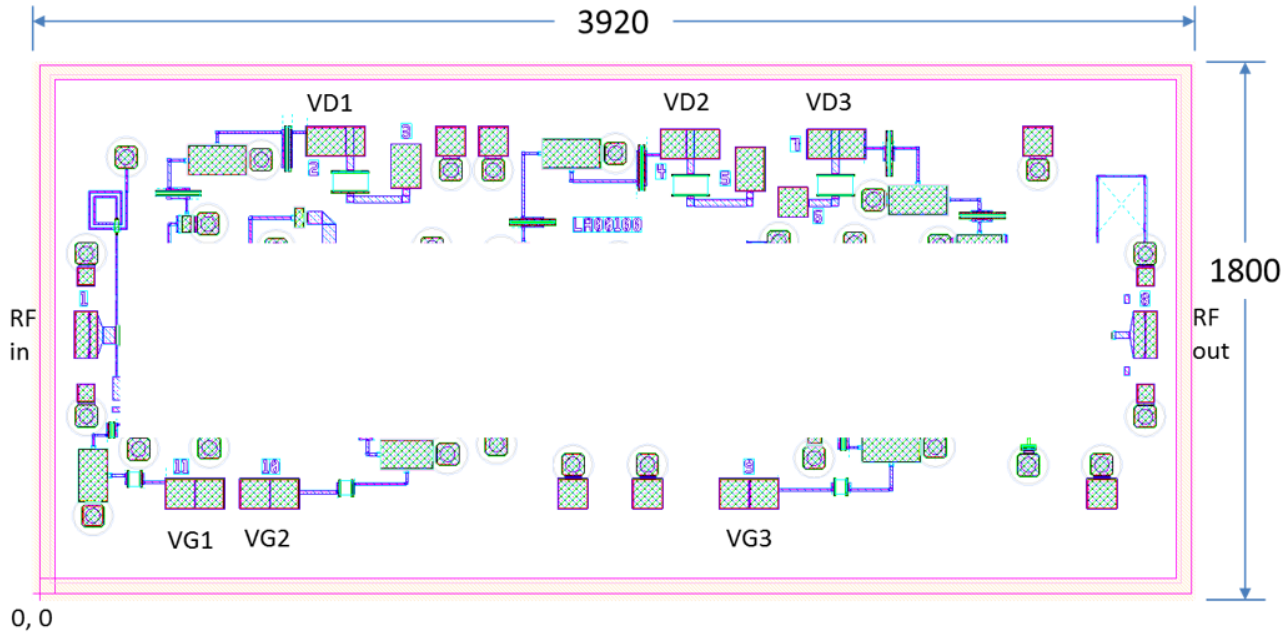
Application Circuit and Turn-on Procedure





1. Internal blocking capacitors on RF in/out ports (P1 and P2), but port 1 (RF input) is tied to ground through a series resistor-inductor, for ESD protection.
2. Gate Voltage (VG) must be applied prior to Drain Voltage (VD);
   Drain Voltage (VD) must be removed prior to Gate Voltage (VG)
3. Performance is optimized with VD set to near 4 V. Optimum gate voltage should be near -0.33 V.

Outline Drawing

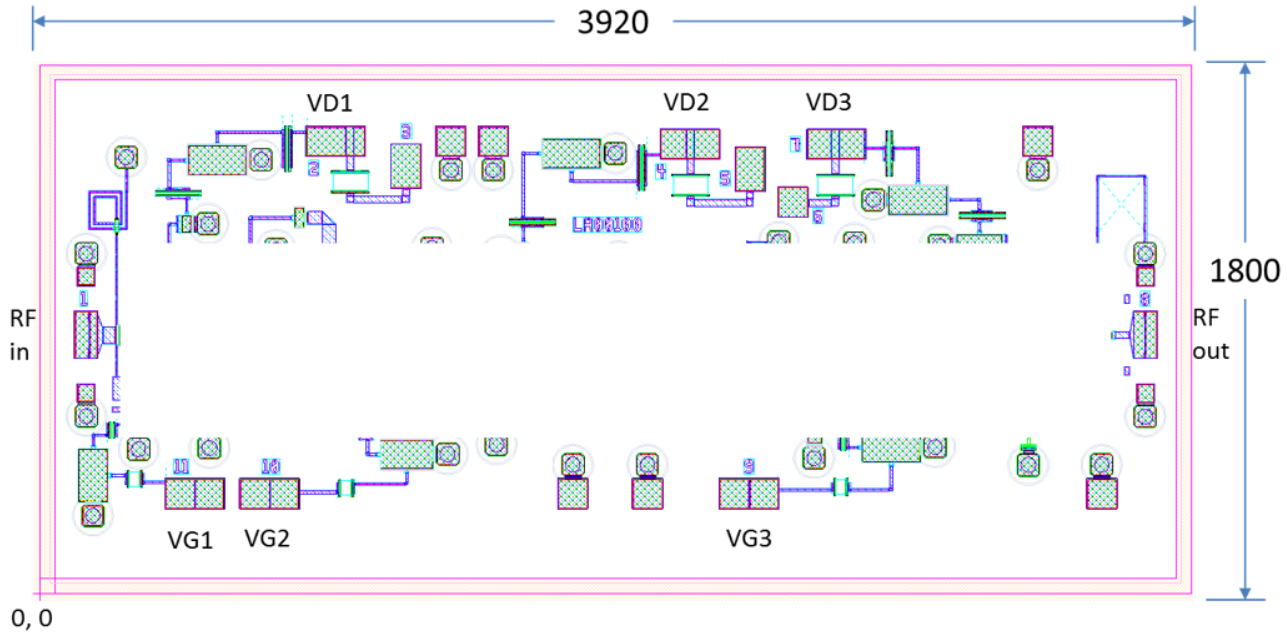


Bond Pad Dimensions

Pad	Pad Description	Length x-dim, (µm)	Width y-dim, (µm)	Length x-dim, (mils)	Width y-dim, (mils)
1	RF input (port 1)	75	160	3.0	6.3
2	VD1 stage 1 drain bias	200	100	7.9	3.9
3	option 50 ohm to VD1	100	150	3.9	5.9
4	VD2 stage 2 drain bias	200	100	7.9	3.9
5	option 50 ohm to VD2	100	150	3.9	5.9
6	option 50 ohm to VD3	100	100	3.9	3.9
7	VD3 stage 3 drain bias	200	100	7.9	3.9
8	RF output (port 2)	80	160	3.1	6.3
9	VG3 stage 3 gate bias	200	100	7.9	3.9
10	VG2 stage 2 gate bias	200	100	7.9	3.9
11	VG1 stage 1 gate bias	200	100	7.9	3.9

Notes:
All dimensions are given in both µm and mils.
Substrate thickness: 100 µm (0.004”).
Backside metallization is gold.
Bond pad metallization is gold.

Outline Drawing



Bonding Pad Center Point Locations

Pad	Pad Description	Length x-dim, (µm)	Width y-dim, (µm)	Length x-dim, (mils)	Width y-dim, (mils)
1	RF input (port 1)	156	881	6.1	34.7
2	VD1 stage 1 drain bias	1007	1541	39.6	60.7
3	option 50 ohm to VD1	1246	1546	49.1	60.9
4	VD2 stage 2 drain bias	2213	1530	87.1	60.2
5	option 50 ohm to VD2	2417	1546	95.2	60.9
6	option 50 ohm to VD3	2564	1332	100.9	52.4
7	VD3 stage 3 drain bias	2707	1530	106.6	60.2
8	RF output (port 2)	3762	881	148.1	34.7
9	VG3 stage 3 gate bias	2414	340	95.0	13.4
10	VG2 stage 2 gate bias	782	340	30.8	13.4
11	VG1 stage 1 gate bias	527	340	20.7	13.4

Notes:
All dimensions are given in both µm and mils.
Substrate thickness: 100 µm (0.004”).
Backside metallization is gold.
Bond pad metallization is gold.