Features

- Wideband Performance
- Low Noise Figure: 2.3 dB
- Gain: 11 dB, @ 2 - 3 V, 80 mA bias
- Good I/O Return Loss: 14 dB
- Self-Biased (single supply voltage)
- Die Size:
  - 2.80 x 1.80 x 0.1 mm
  - 0.110 x 0.071 x 0.004 inch
- RoHS* Compliant

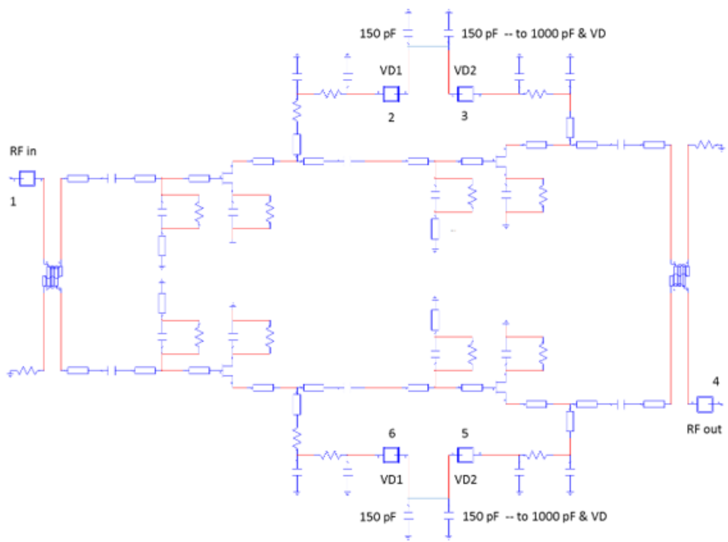
Applications

- Military EW & SIGINT
- Receiver or Transmitter
- Telecom Infrastructure
- Space Hybrids
- Test & Measurement Systems

Description

The ENGLA00096C is a wideband low noise amplifier (LNA) operating across 18 to 50 GHz. The design is 50 ohm matched and includes on board bias circuitry. The amplifier offers 11 dB gain, 2.3 dB noise figure, and 23 dBm output third-order intercept point (OIP3) above 40 GHz, at room temperature. The GaAs MMIC has gold backside metallization and is designed to be silver epoxy or gold-tin solder attached. The RF interconnects are designed to account for wire bonds and external microstrip flares for optimal integrated return loss. No additional ground interconnects are required.

Functional Block Diagram



Ordering Information

Part Number	Package
ENGLA00096C	Die

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications:
Freq. = 18 - 50 GHz, T_A = +25°C, V_D = 3 V, Z_0 = 50 Ω

Parameter	Units	Min.	Typ.	Max.
Gain	dB	9.5	11.5	—
Noise Figure	dB	—	2.3 (20 – 50 GHz)	3.3 (20 – 50 GHz)
Input Return Loss	dB	11	15	—
Output Return Loss	dB	11	14	—
Output P1dB	dBm	—	-7 (18 GHz) to +12 (51 GHz) (-4 to +16 dBm at 4 V bias)	—
Output IP3	dBm	—	+6 (18 GHz) to +25 (51 GHz) (+9 to +25 dBm at 4 V bias)	—
Output IP2	dBm	—	+14 (18 GHz) to +45 (51 GHz) (+17 to +45 dBm at 4 V bias)	—
Supply Current	mA	55	60 - 120	140
Thermal Resistance*	ºC/W	—	115 * includes 25-µm thick AuSn solder mount	—

Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Units
Drain Voltage	1.5	2 - 4	4.5	V
Gate Voltage	—	Self-Bias	—	V
Drain Current	55	60 - 120	140	mA

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

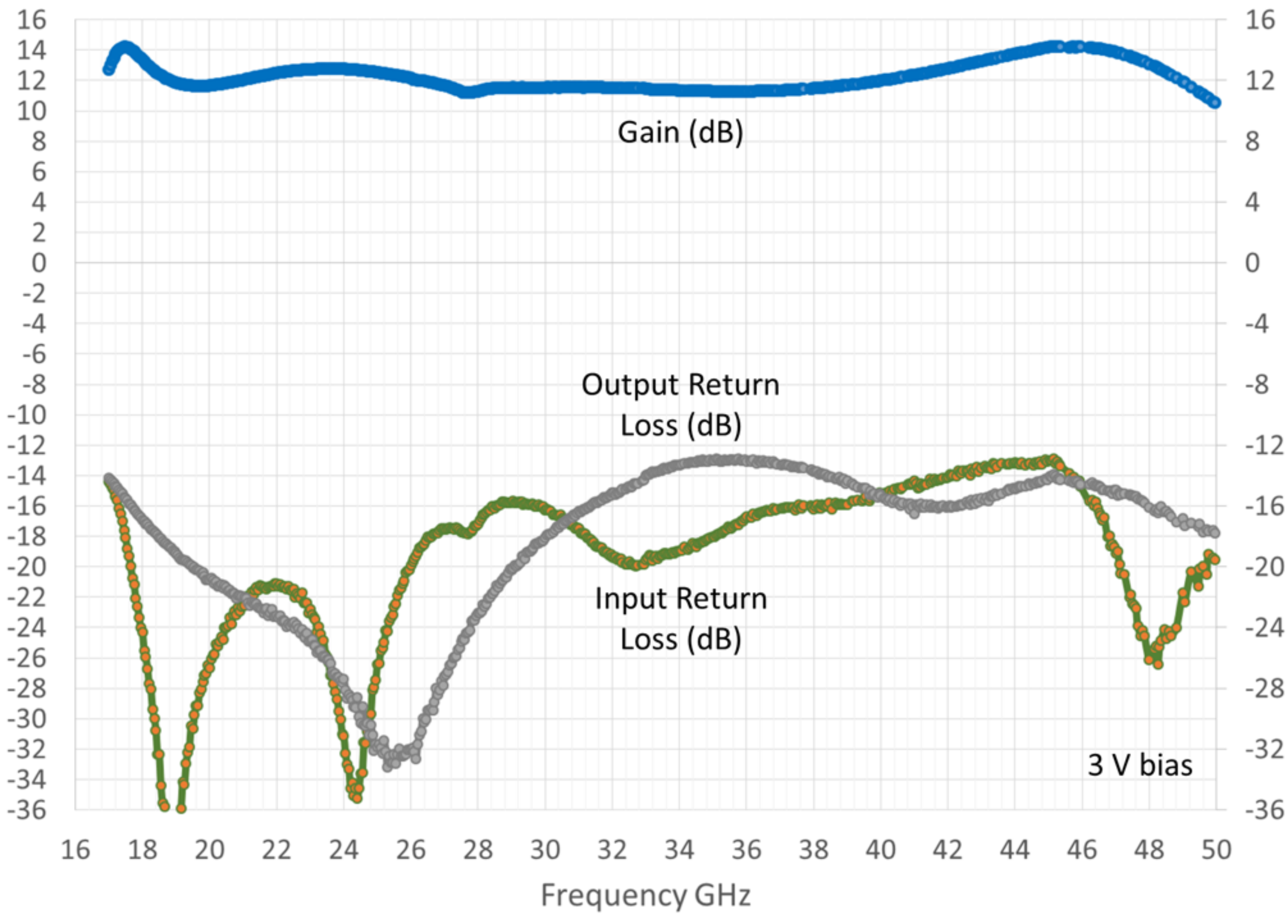
Absolute Maximum Ratings[1,2]

Parameter	Absolute Maximum
Drain Voltage	5.5 V
Gate Voltage	N/A; Self Biased
RF Input Power	17 dBm
Junction Temperature	+165°C
Operating Temperature	-55°C to +100°C
Storage Temperature	-65°C to +150°C

1. Exceeding any one or combination of these limits may cause permanent damage to this device.
2. MACOM does not recommend sustained operation near these survivability limits.

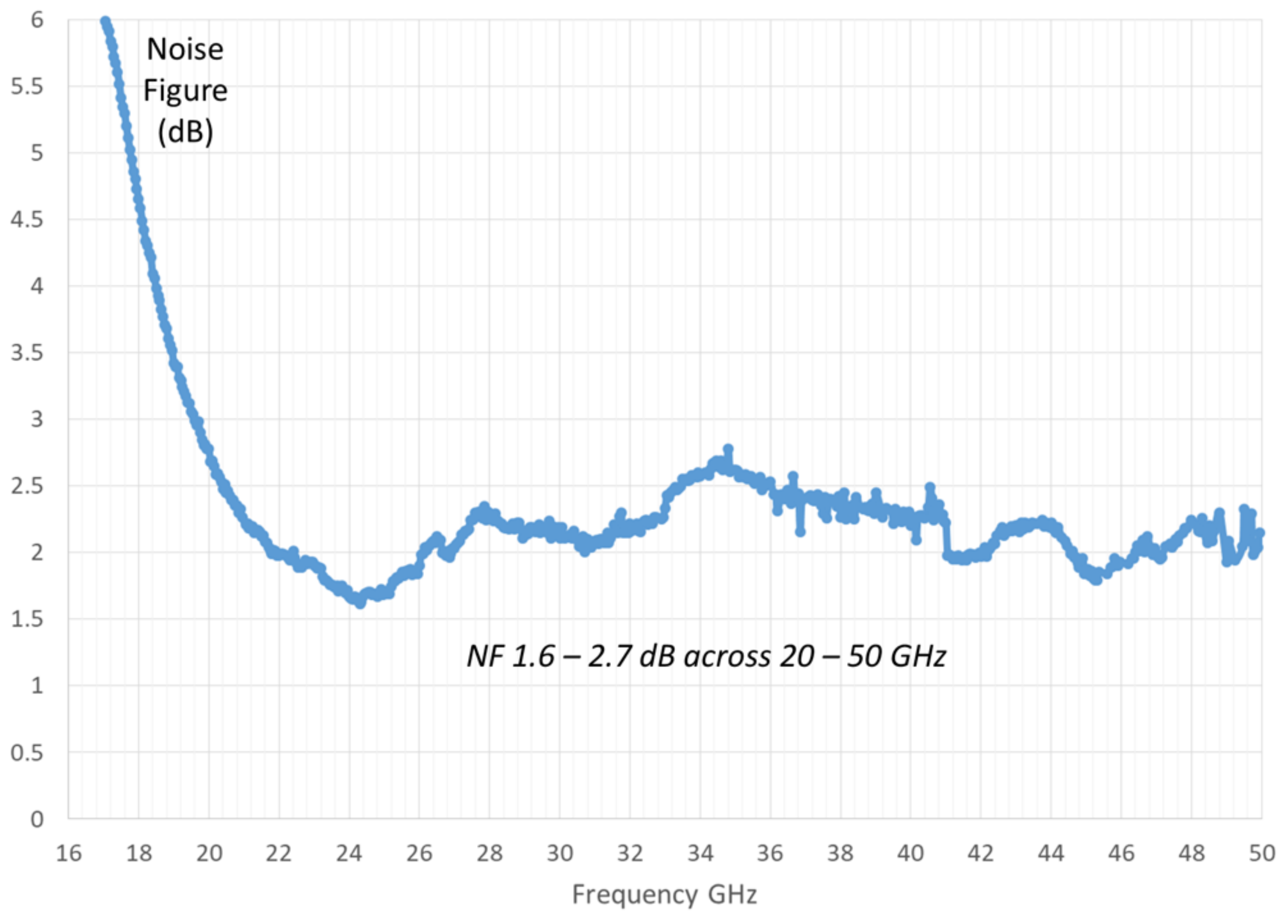
Measured RF Data: With Wirebonds to External 50 Ω Microstrip Lines

Gain and In / Out Return Loss: V_D = 3 V; I_D = 72 mA, T_A = 25°C



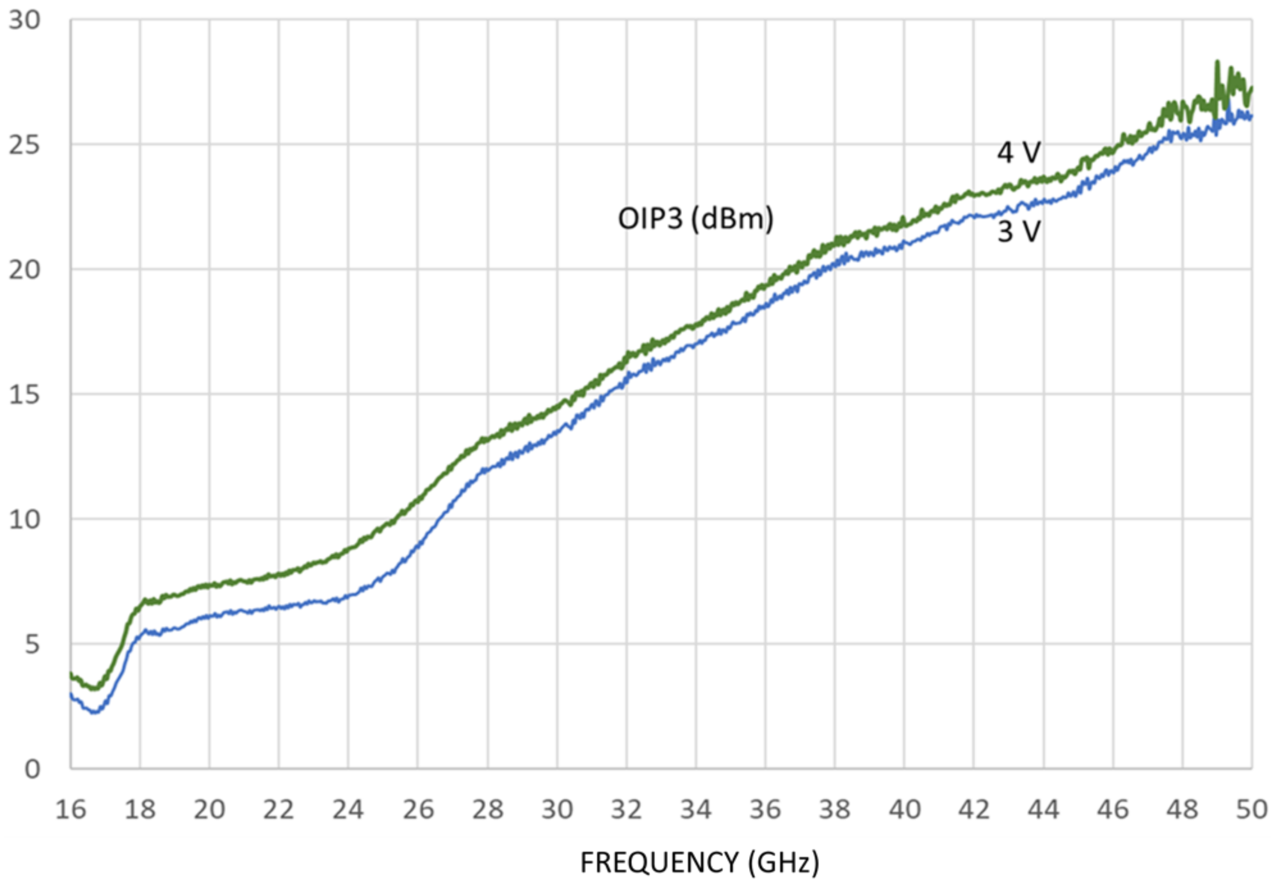
Measured RF Data: With Wirebonds to External 50 Ω Microstrip Lines

Noise Figure: V_D ***= 3 V;*** I_D ***= 72 mA,*** T_A ***= 25°C***



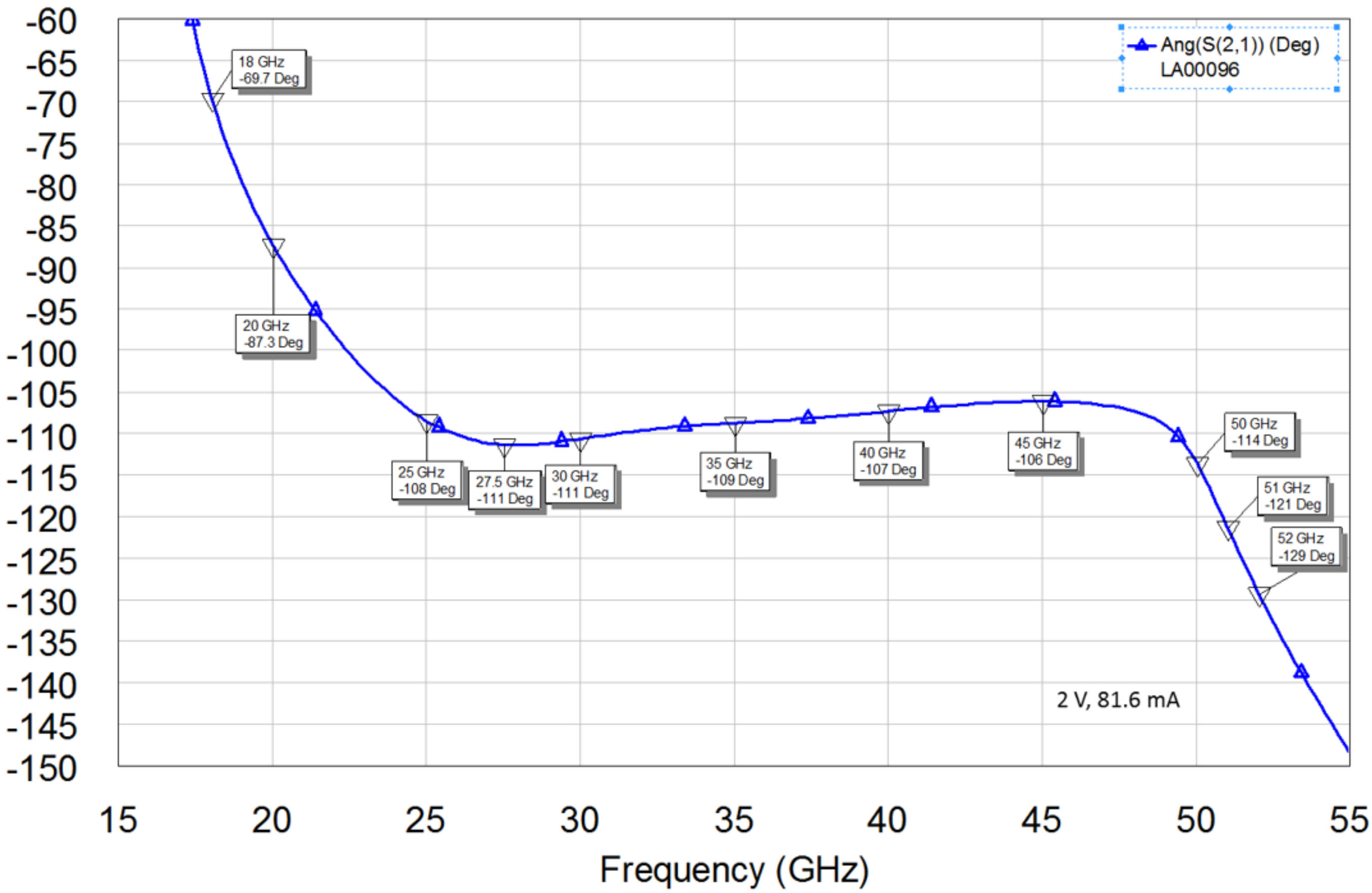
Measured RF Data: With Wirebonds to External 50 Ω Microstrip Lines

Output Third-Order Intercept: V_D = 3 V; I_D = 72 mA, T_A = 25°C, 10 MHz spacing, -20 dBm/tone



Predicted Deviation from Linear Phase (degrees), referenced to an ideal 50 Ω transmission line 240 degrees long at 10 GHz

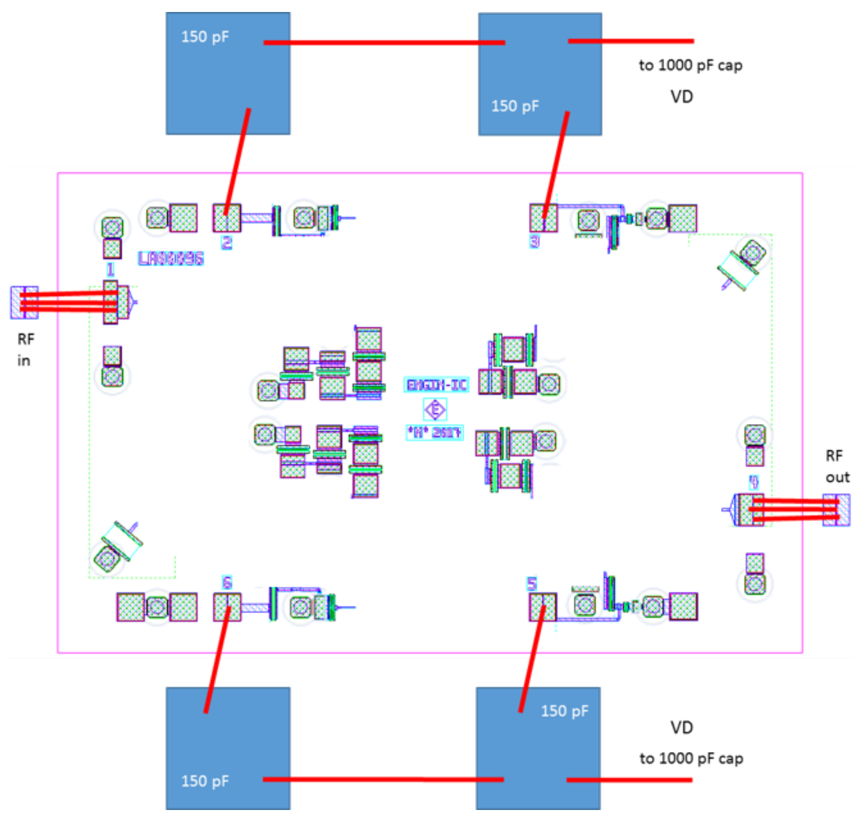
Predicted Deviation: V_D = 2 V; I_D = 81.6 mA, T_A = 25°C, Linear Model



External I/O Microstrip Flare Dimensions (on 5-mil Alumina) and I/O Bond Wire Inductances for Optimum Insertion and Return Loss Performance

S-parameters can be supplied at DIE level such that optimal flare dimensions can be made for the substrate connection medium used (if different from 5-mil Alumina).

Pad Flare Dimension	Flare Width x-dim, (µm)	Flare Length y-dim, (µm)	Wire Inductance (nH)	Wire Length (µm)	Wire Length (mils)	# of Wires
RF Input	120	no flare	0.65	254	10	3
RF Output	120	no flare	0.65	254	10	3

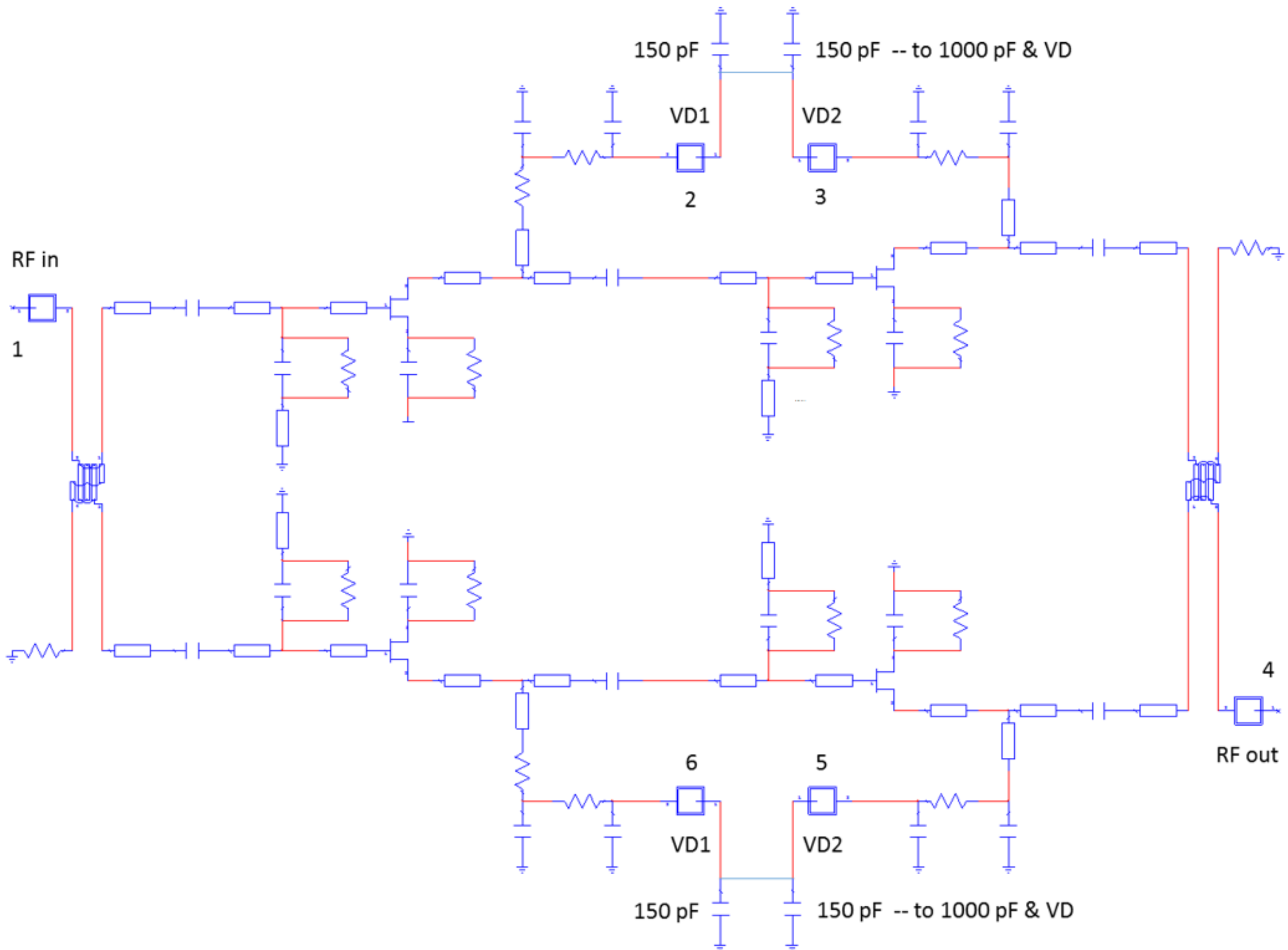


Notes:
1. To achieve bond wire inductance noted, bond the number of wires shown in parallel from each external flare to each associated MMIC RF bond pad as shown above.
2. Gold Wire Details:
   Diameter: 25.4 µm (1 mil)
   Spacing: 4 mils (~ 100 µm) typical
   Height above Ground: 8 mils (~ 200 µm) typical (wedge bonds)
3. Wire Length is total length if the wire were made perfectly straight.

Assembly Guidelines

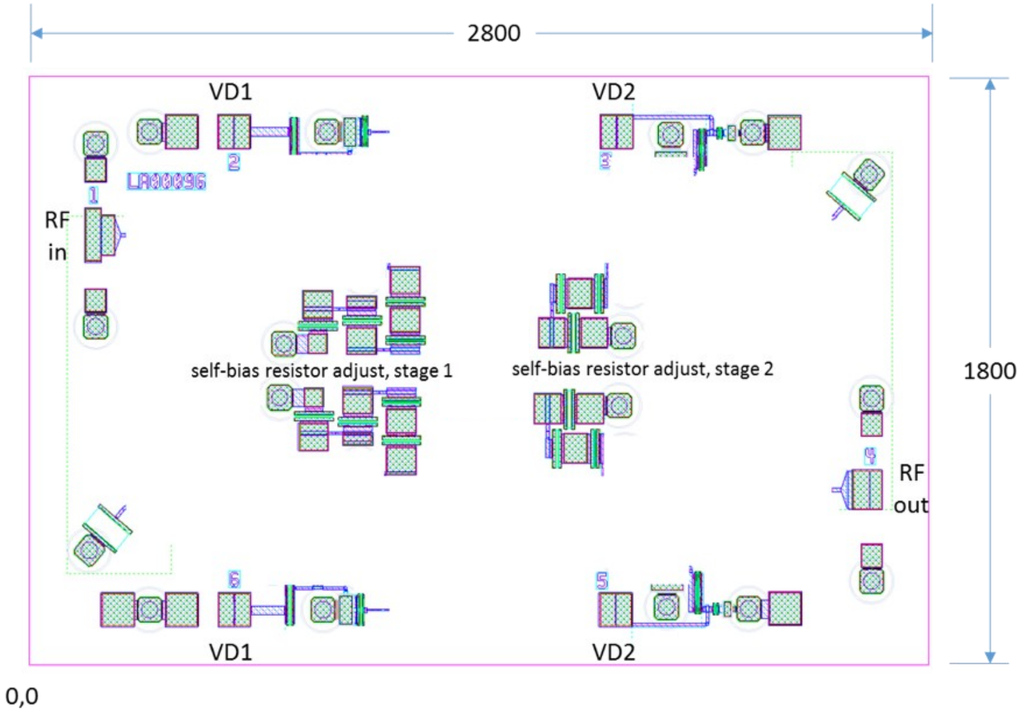
The backside metallization is RF/DC ground. Attachment should be accomplished with electrically and thermally conductive epoxy, or with gold-tin (AuSn) solder. This device supports high frequency performance. Care should be made to following the wirebond dimensions as shown in the flare diagram.

Application Circuit and Turn-on Procedure



1. Internal blocking capacitors on RF in/out ports (P1 and P2).
2. Performance is optimized for noise figure with VD set near 2.0 V. Output power at 1-dB gain compression can be increased by increasing VD to 3 or 4 V.

Outline Drawing



Bond Pad Dimensions

Pad	Pad Description	Length x-dim, (µm)	Width y-dim, (µm)	Length x-dim, (mils)	Width y-dim, (mils)
1	RF Input (port 1)	120	90	4.7	3.5
2	VD1 stage 1 upper	100	100	3.9	3.9
3	VD2 stage 2 upper	100	100	3.9	3.9
4	RF Output (port 2)	120	90	4.7	3.5
5	VD2 stage 2 lower	100	100	3.9	3.9
6	VD1 stage 1 lower	100	100	3.9	3.9
	Self-bias adjust pads	75	75	3.0	3.0

Bond Pad Center Point Location

Pad	Pad Description	Length x-dim, (µm)	Width y-dim, (µm)	Length x-dim, (mils)	Width y-dim, (mils)
1	RF Input (port 1)	224	1314	8.8	51.7
2	VD1 stage 1 upper	636	1630	25.0	64.2
3	VD2 stage 2 upper	1827	1630	71.9	64.2
4	RF Output (port 2)	2607	536	102.6	21.1
5	VD2 stage 2 lower	1824	170	71.8	6.7
6	VD1 stage 1 lower	638	170	25.1	6.7

All dimensions are given in both µm and mils.
Substrate thickness: 100 µm (0.004”).
Backside metallization is gold.
Bond pad metallization is gold.