## Features
- N-channel enhancement mode device
- DMOS structure
- Lower capacitances for broadband operation
- High saturated output power
- Lower noise figure than bipolar devices
- RoHS Compliant

### ABSOLUTE MAXIMUM RATINGs AT 25°C

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Rating</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-Source Voltage</td>
<td>( V_{DS} )</td>
<td>65</td>
<td>V</td>
</tr>
<tr>
<td>Gate-Source Voltage</td>
<td>( V_{GS} )</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>Drain-Source Current</td>
<td>( I_{DS} )</td>
<td>16</td>
<td>A</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>( P_{D} )</td>
<td>206</td>
<td>W</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>( T_{J} )</td>
<td>200</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>( T_{STG} )</td>
<td>-65 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>Thermal Resistance</td>
<td>( \theta_{JC} )</td>
<td>0.85</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

### TYPICAL DEVICE IMPEDANCE

<table>
<thead>
<tr>
<th>( F ) (MHz)</th>
<th>( Z_{IN} (\Omega) )</th>
<th>( Z_{LOAD} (\Omega) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>30</td>
<td>5.4 - j4.4</td>
<td>5.7 + j4.7</td>
</tr>
<tr>
<td>50</td>
<td>2.5 - j4.4</td>
<td>3.4 + j3.5</td>
</tr>
<tr>
<td>100</td>
<td>1.6 - j3.4</td>
<td>2.4 + j2.4</td>
</tr>
<tr>
<td>175</td>
<td>0.7 - j1.2</td>
<td>1.7 + j0.8</td>
</tr>
</tbody>
</table>

\( V_{DD} = 28 \text{ V}, I_{DD} = 400 \text{ mA}, P_{OUT} = 80 \text{ W} \)

\( Z_{IN} \) is the series equivalent input impedance of the device from gate to source.

\( Z_{LOAD} \) is the optimum series equivalent load impedance as measured from drain to ground.

### ELECTRICAL CHARACTERISTICS AT 25°C

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-Source Breakdown Voltage</td>
<td>( BV_{DSS} )</td>
<td>65</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Drain-Source Leakage Current</td>
<td>( I_{DSS} )</td>
<td>-</td>
<td>4.0</td>
<td>mA</td>
</tr>
<tr>
<td>Gate-Source Leakage Current</td>
<td>( I_{GS} )</td>
<td>-</td>
<td>4.0</td>
<td>μA</td>
</tr>
<tr>
<td>Gate Threshold Voltage</td>
<td>( V_{G(S TH)} )</td>
<td>2.0</td>
<td>6.0</td>
<td>V</td>
</tr>
<tr>
<td>Forward Transconductance</td>
<td>( G_{M} )</td>
<td>2.0</td>
<td>-</td>
<td>S</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>( C_{ISS} )</td>
<td>-</td>
<td>180</td>
<td>pF</td>
</tr>
<tr>
<td>Output Capacitance</td>
<td>( C_{OSS} )</td>
<td>-</td>
<td>160</td>
<td>pF</td>
</tr>
<tr>
<td>Reverse Capacitance</td>
<td>( C_{RSS} )</td>
<td>-</td>
<td>32</td>
<td>pF</td>
</tr>
<tr>
<td>Power Gain</td>
<td>( G_{P} )</td>
<td>13</td>
<td>-</td>
<td>dB</td>
</tr>
<tr>
<td>Drain Efficiency</td>
<td>( r_{D} )</td>
<td>60</td>
<td>-</td>
<td>%</td>
</tr>
<tr>
<td>Load Mismatch Tolerance</td>
<td>( V_{SWR-T} )</td>
<td>-</td>
<td>30:1</td>
<td></td>
</tr>
</tbody>
</table>

\( V_{DD} = 28 \text{ V}, I_{DD} = 400 \text{ mA}, P_{OUT} = 60.0 \text{ W} \)

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RF Power MOSFET Transistor
80 W, 2 - 175 MHz, 28 V

TEST FIXTURE SCHEMATIC

VGS J3
VDS J4
R2
c12
c11
c10
L4
C12
C11
C10
L3
C7
C9
C8
L2
Q1
Q1
C2
C4
C5
C3
J1
RF IN
J2
RF OUT
VDS = 28 VOLTS
IDQ = 400mA

PARTS LIST
C1,C3 TRIMMER CAPACITOR 4-40pF
C2,C9,C10 CAPACITOR 50pF
C4,C11 CAPACITOR 1000pF
C5 MONOLITHIC CIRCUIT CAPACITOR 0.01µF
C6,C8 TRIMMER CAPACITOR 9-180pF
C7 CAPACITOR 15pF
C12 ELECTROLYTIC CAPACITOR 50µF 50 VOLT
L1 NO. 12 AWG COPPER WIRE X 1.18" (LOOP 0.5")
L2 NO. 12 AWG COPPER WIRE X 1" (LOOP 0.4")
L3,L4 8 TURNS OF NO. 18 AWG ENAMEL WIRE ON
Ø0.25", CLOSE WOUND
R1 RESISTOR 300 OHMS 0.5 WATT
R2 RESISTOR 2.7K OHMS 0.25 WATT
Q1 DU2880T
BOARD FR4 0.062"
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