CMPA9396025S

9.3 - 9.6 GHz, 25 W, Packaged GaN MMIC Power Amplifier

Description

The CMPA9396025S is a GaN MMIC designed specifically from 9.3 - 9.6 GHz to be compact and provide high-efficiency, which makes it ideal for marine radar amplifier applications. The MMIC delivers 25W at 100µsec pulse width and 10% duty cycle. The 50-ohm, 3-stage MMIC is available in a plastic surface-mount package.

Package Type: 6 x 6 QFN
PN: CMPA9396025S

Typical Performance Over 9.3 - 9.6 GHz (T_C = 25°C)

Parameter	9.3 GHz	9.4 GHz	9.5 GHz	9.6 GHz	Units
Small Signal Gain	36.0	35.9	35.9	36.2	dB
Output Power[1]	37.0	37.5	37.5	37.0	W
Power Gain[1]	26.7	26.7	26.7	26.7	dB
Power Added Efficiency[1]	41	42	42	41	%

Note:
[1] P_{IN} = 19 dBm, Pulse Width = 100µs; Duty Cycle = 10%, V_D = 40 V, I_{DQ} = 260 mA

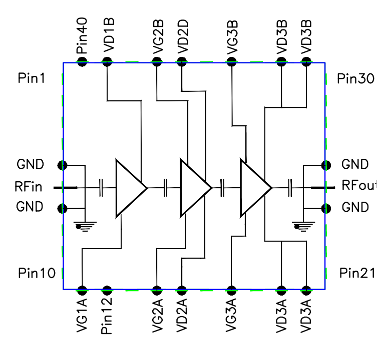
Features

- 9.3 - 9.6 GHz Operation
- 30 W Typical Output Power
- 27 dB Power Gain
- 50-ohm Matched for Ease of Use
- Plastic Surface-Mount Package, 6x6 mm QFN

Note: Features are typical performance across frequency under 25°C operation. Please reference performance charts for additional details.

Applications

- Marine radar
- Military radar



RoHS compliant

Rev. 1.0, 2022-8-23

Absolute Maximum Ratings (not simultaneous) at 25°C

Parameter	Symbol	Rating	Units	Conditions
Drain-source Voltage	V_{DSS}	120	V_{DC}	25˚C
Gate-source Voltage	V_{GS}	-10, +2		
Storage Temperature	T_{STG}	-65, +150	°C	
Maximum Forward Gate Current	I_G	8.6	mA	25˚C
Maximum Drain Current	I_{DMAX}		A	
Soldering Temperature	T_S	260	°C	

Electrical Characteristics (Frequency = 9.3 GHz to 9.6 GHz unless otherwise stated; T_C = 25°C)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Conditions
DC Characteristics[1]						
Gate Threshold Voltage	$V_{GS(th)}$	-3.6	–	-2.4	V	V_{DS} = 10 V, I_D = 8.6 mA
Gate Quiescent Voltage	$V_{GS(Q)}$	–	-2.65	–	V_{DC}	V_{DD} = 40 V, I_{DQ} = 260 mA
Saturated Drain Current[2]	I_{DS}	6.2	8.6	–	A	V_{DS} = 6.0 V, V_{GS} = 2.0 V
Drain-Source Breakdown Voltage	V_{BD}	100	–	–	V	V_{GS} = -8 V, I_D = 8.6 mA
RF Characteristics[3,4]						
Small Signal Gain at 9.3 GHz	$S21_1$	–	36.0	–	dB	V_{DD} = 40 V, I_{DQ} = 260 mA
Small Signal Gain at 9.6 GHz	$S21_2$	–	36.2	–		
Output Power at 9.3 GHz	P_{OUT1}	–	37.0	–	W	
Output Power at 9.6 GHz	P_{OUT2}	–		–		
Power Added Efficiency at 9.3 GHz	PAE_1	–	41	–	%	
Power Added Efficiency at 9.6 GHz	PAE_2	–		–		
Power Gain	G_P	–	26.0	–	dB	V_{DD} = 40 V, I_{DQ} = 260 mA, P_{IN} = 19 dBm
Input Return Loss	S11	–	-11.4	–		V_{DD} = 40 V, I_{DQ} = 260 mA
Output Return Loss	S22	–	-8.2	–		
Output Mismatch Stress	VSWR	–	–	3:1	Ψ	No damage at all phase angles, V_{DD} = 40 V, I_{DQ} = 260 mA, P_{IN} = 19 dBm

Notes:
[1] Measured on wafer prior to packaging
[2] Scaled from PCM data
[3] Measured in CMPA9396025S high volume test fixture at 9.3 and 9.6 GHz and may not show the full capability of the device due to source inductance and thermal performance.
[4] P_{IN} = 19 dBm, Pulse Width = 25µs; Duty Cycle = 1%

Thermal Characteristics

Parameter	Symbol	Rating	Units	Conditions
Operating Junction Temperature	T_J	225	°C	
Thermal Resistance, Junction to Case (packaged)[1]	$R_{\theta JC}$	1.94	°C/W	Pulse Width = 100µs, Duty Cycle =10%

Notes:
[1] Measured for the CMPA9396025S at P_{DISS} = 28.6 W

Typical Performance of the CMPA9396025S

Test conditions unless otherwise noted: V_D = 40 V, I_{DQ} = 260 mA, PW = 100µs, DC = 10%, P_{IN} = 19 dBm, T_{BASE} = +25°C

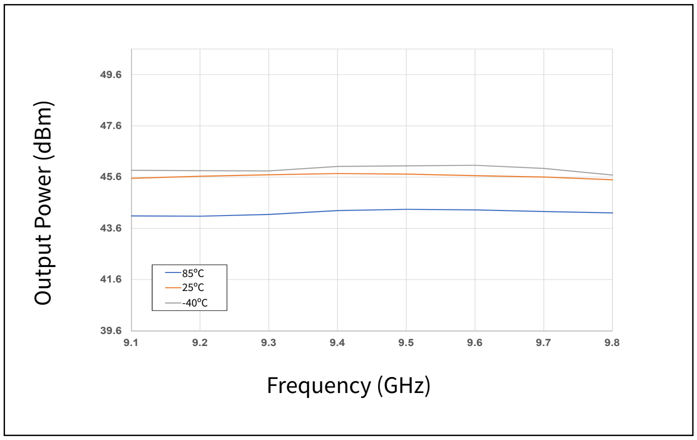


Figure 1. Output Power vs Frequency as a Function of Temperature

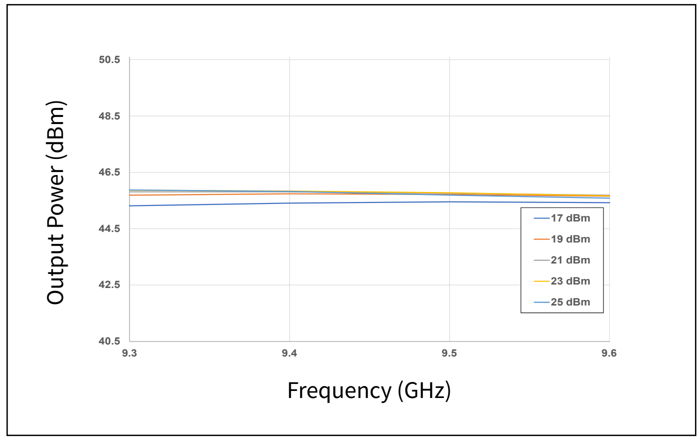


Figure 2. Output Power vs Frequency as a Function of Input Power

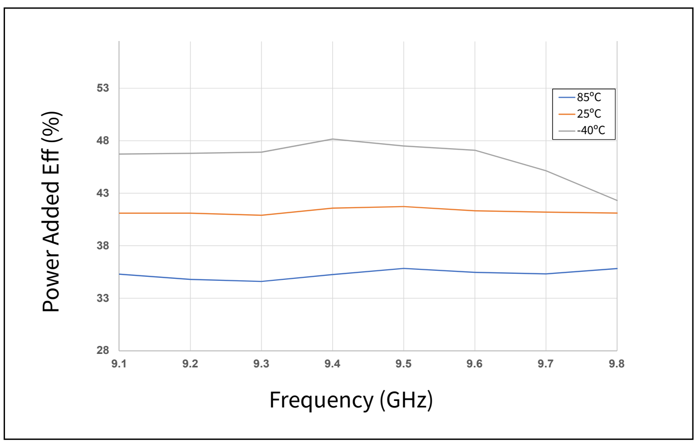


Figure 3. Power Added Eff. vs Frequency as a Function of Temperature

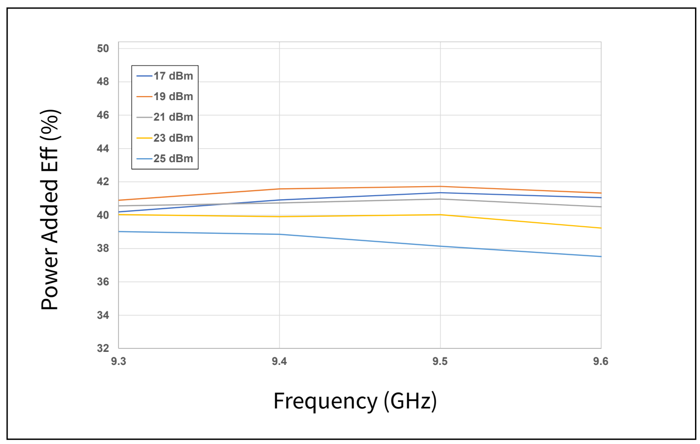


Figure 4. Power Added Eff. vs Frequency as a Function of Input Power

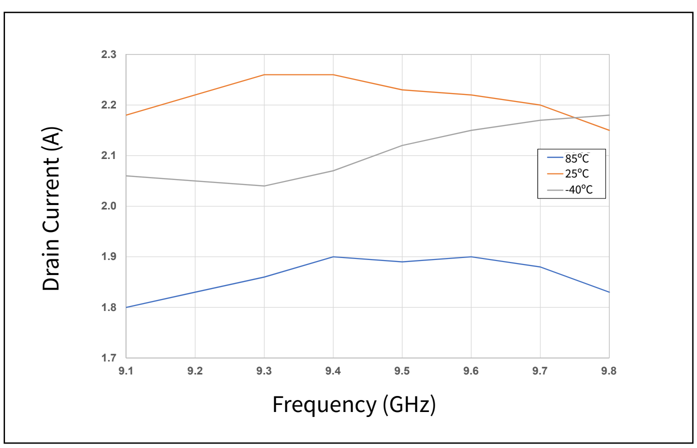


Figure 5. Drain Current vs Frequency as a Function of Temperature

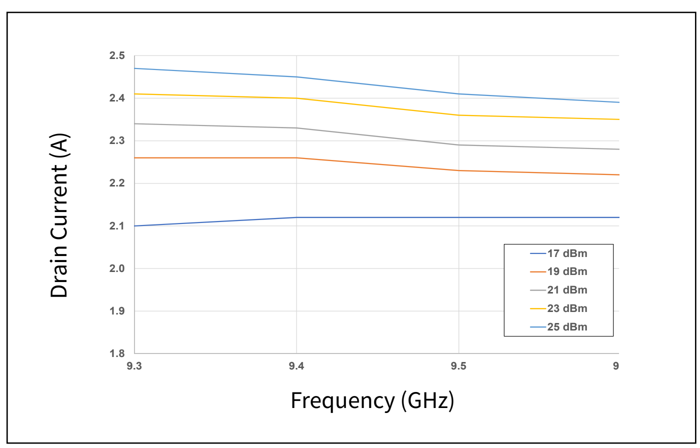


Figure 6. Drain Current vs Frequency as a Function of Input Power

Typical Performance of the CMPA9396025S

Test conditions unless otherwise noted: V_D = 40 V, I_{DQ} = 260 mA, PW = 100µs, DC = 10%, P_{IN} = 19 dBm, T_{BASE} = +25°C

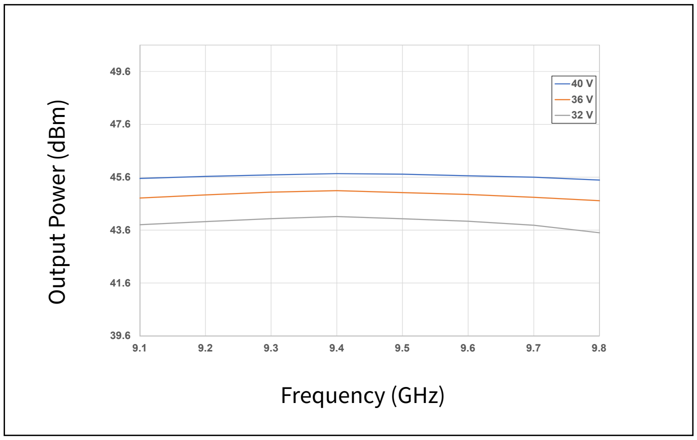


Figure 7. Output Power vs Frequency as a Function of V_D

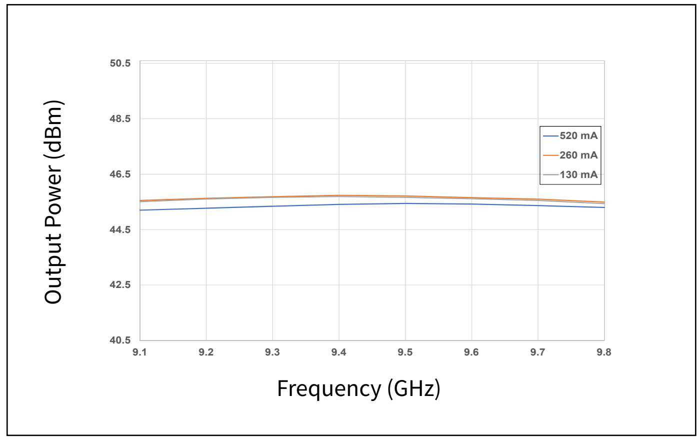


Figure 8. Output Power vs Frequency as a Function of I_{DQ}

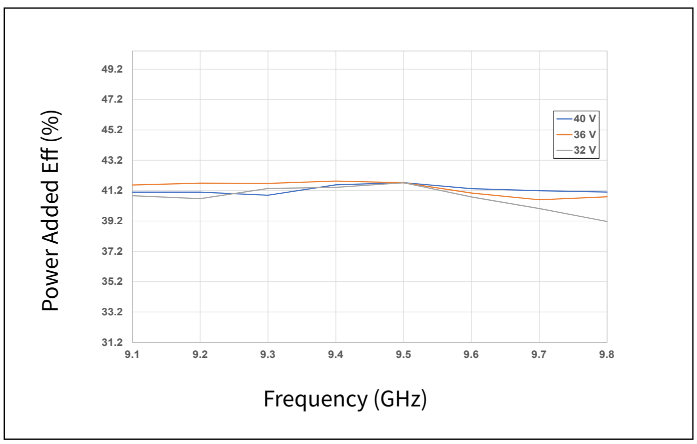


Figure 9. Power Added Eff. vs Frequency as a Function of V_D

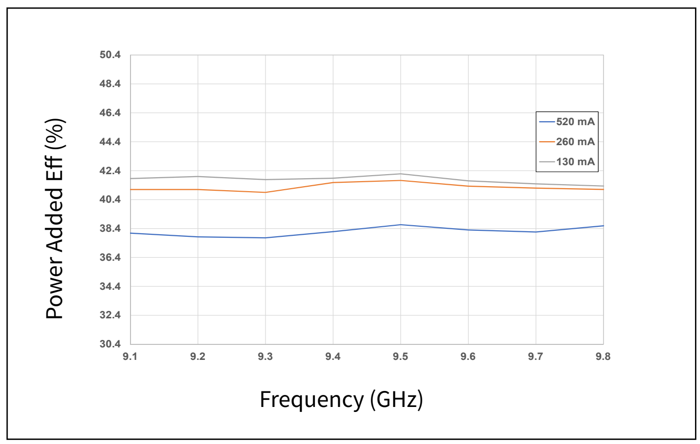


Figure 10. Power Added Eff. vs Frequency as a Function of I_{DQ}

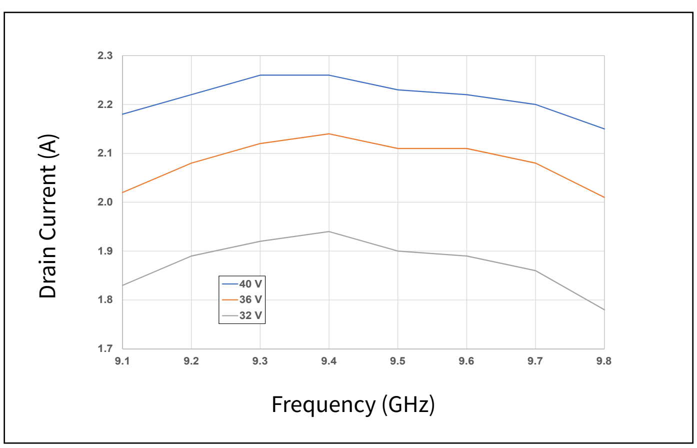


Figure 11. Drain Current vs Frequency as a Function of V_D

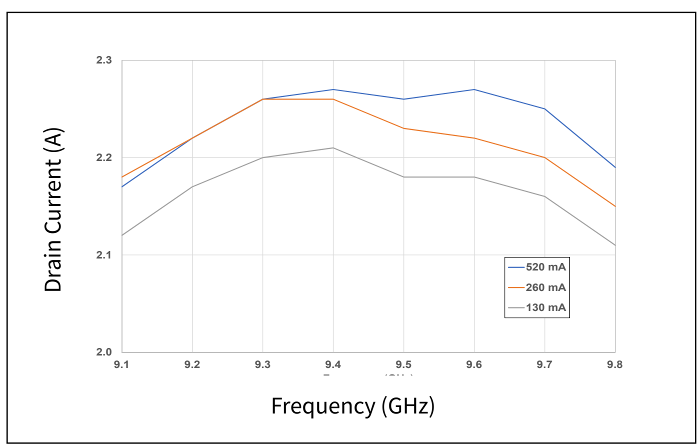


Figure 12. Drain Current vs Frequency as a Function of I_{DQ}

Typical Performance of the CMPA9396025S

Test conditions unless otherwise noted: V_D = 40 V, I_{DQ} = 260 mA, PW = 100µs, DC = 10%, P_{IN} = 19 dBm, T_{BASE} = +25°C

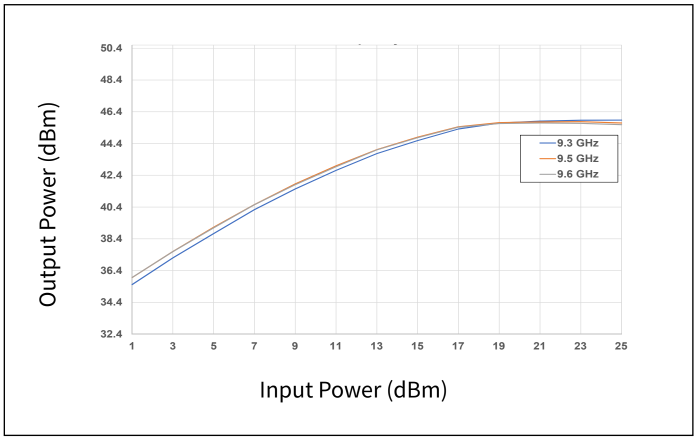


Figure 13. Output Power vs Input Power as a Function of Frequency

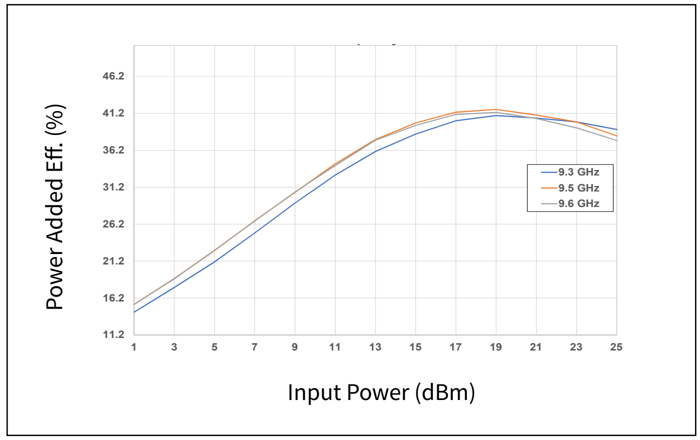


Figure 14. Power Added Eff. vs Input Power as a Function of Frequency

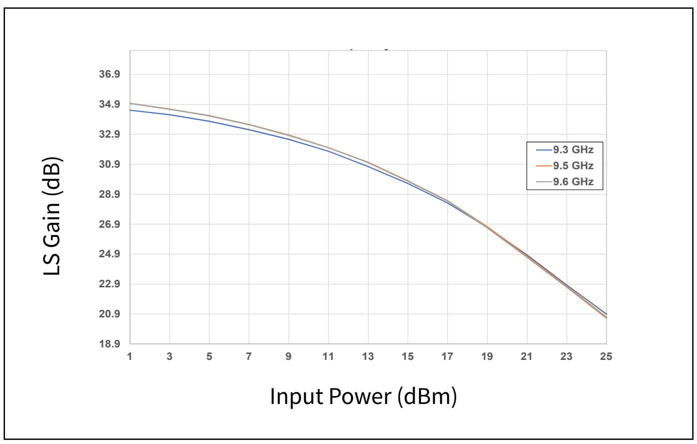


Figure 15. Large Signal Gain vs Input Power as a Function of Frequency

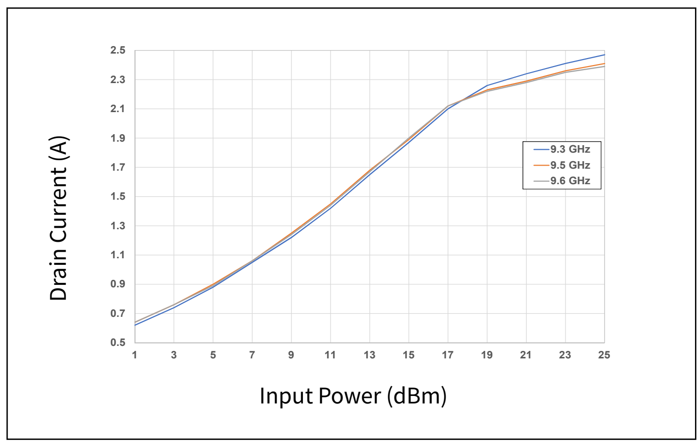


Figure 16. Drain Current vs Input Power as a Function of Frequency

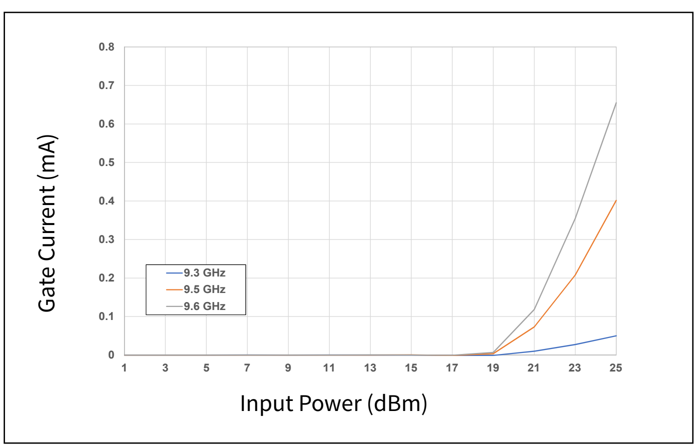


Figure 17. Gate Current vs Input Power as a Function of Frequency

Typical Performance of the CMPA9396025S

Test conditions unless otherwise noted: V_D = 40 V, I_{DQ} = 260 mA, PW = 100µs, DC = 10%, P_{IN} = 19 dBm, T_{BASE} = +25°C

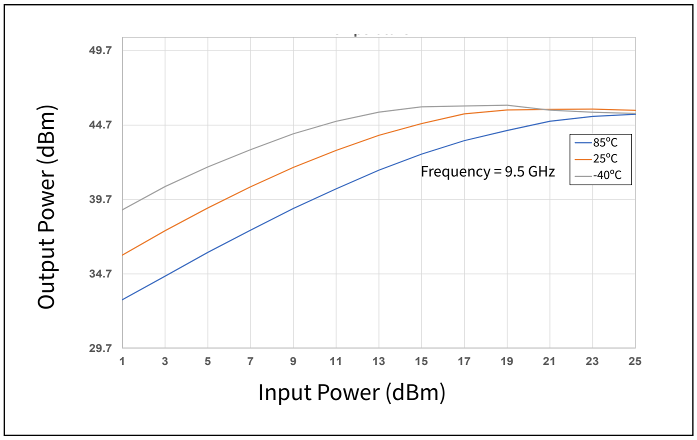


Figure 18. Output Power vs Input Power as a Function of Temperature

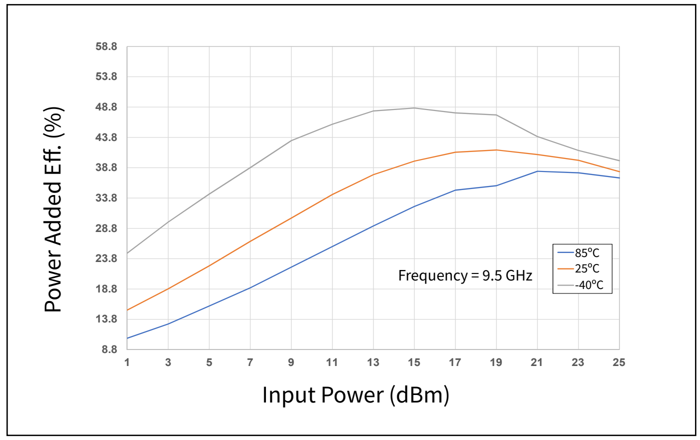


Figure 19. Power Added Eff. vs Input Power as a Function of Temperature

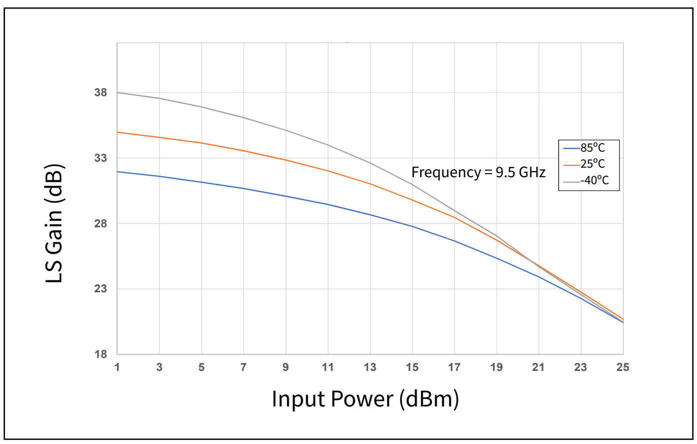


Figure 20. Large Signal Gain vs Input Power as a Function of Temperature

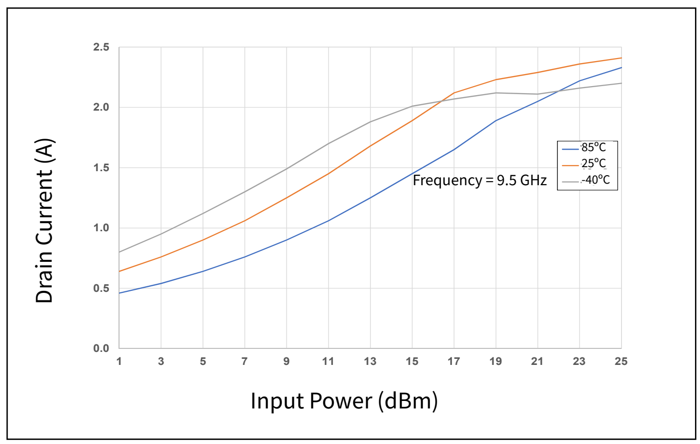


Figure 21. Drain Current vs Input Power as a Function of Temperature

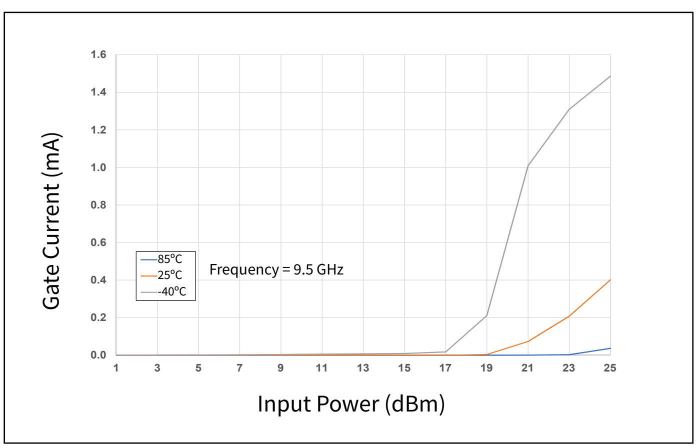


Figure 22. Gate Current vs Input Power as a Function of Temperature

Typical Performance of the CMPA9396025S

Test conditions unless otherwise noted: V_D = 40 V, I_{DQ} = 260 mA, PW = 100µs, DC = 10%, P_{IN} = 19 dBm, T_{BASE} = +25°C

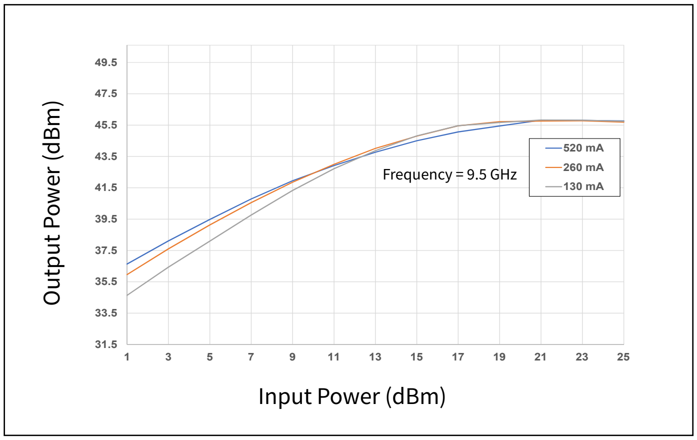


Figure 23. Output Power vs Input Power as a Function of I_{DQ}

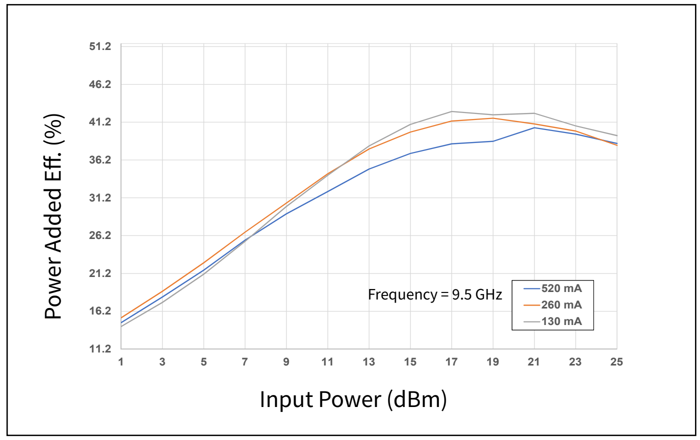


Figure 24. Power Added Eff. vs Input Power as a Function of I_{DQ}

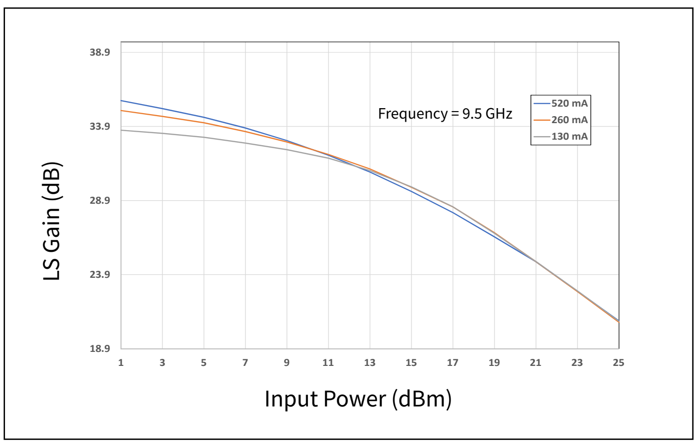


Figure 25. Large Signal Gain vs Input Power as a Function of I_{DQ}

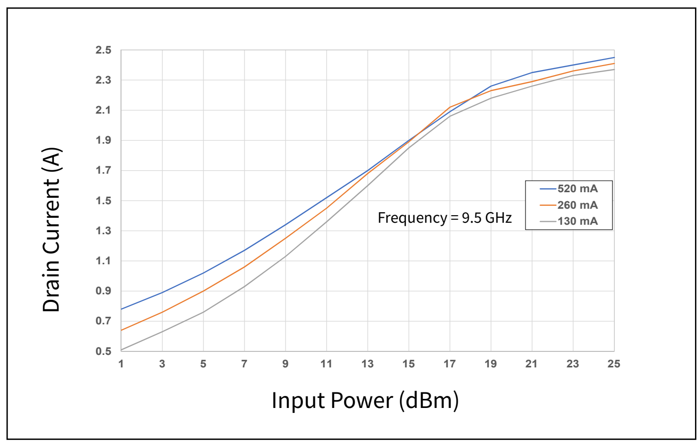


Figure 26. Drain Current vs Input Power as a Function of I_{DQ}

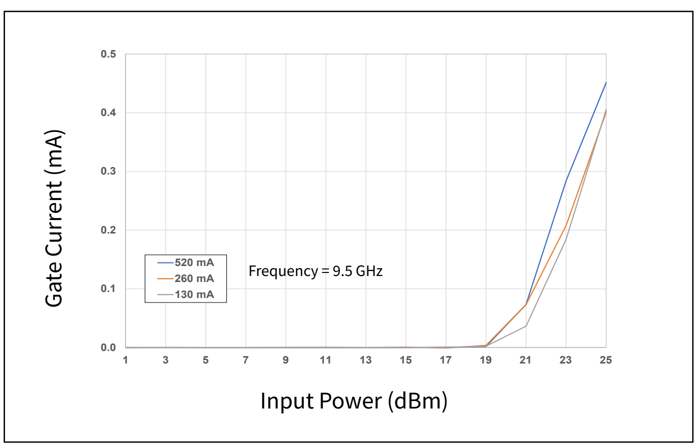


Figure 27. Gate Current vs Input Power as a Function of I_{DQ}

Typical Performance of the CMPA9396025S

Test conditions unless otherwise noted: V_D = 40 V, I_{DQ} = 260 mA, PW = 100µs, DC = 10%, P_{IN} = 19 dBm, T_{BASE} = +25°C

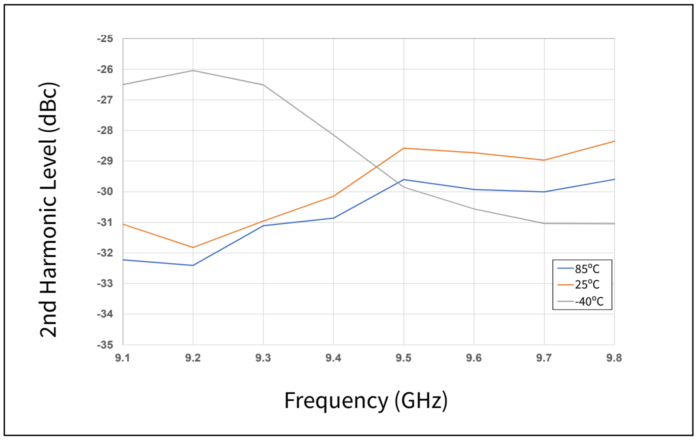


Figure 28. 2nd Harmonic vs Frequency as a Function of Temperature

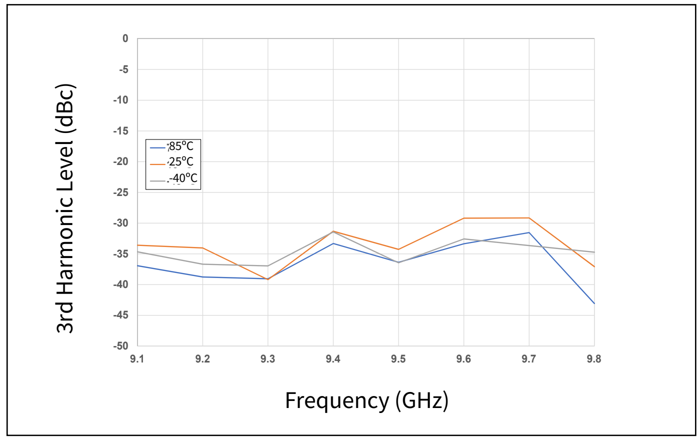


Figure 29. 3rd Harmonic vs Frequency as a Function of Temperature

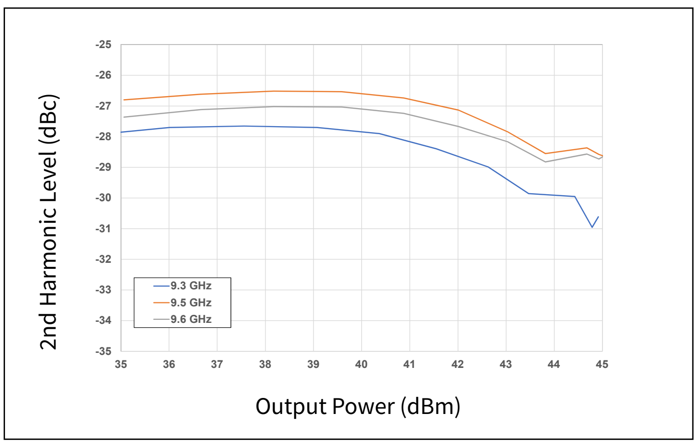


Figure 30. 2nd Harmonic vs Output Power as a Function of Frequency

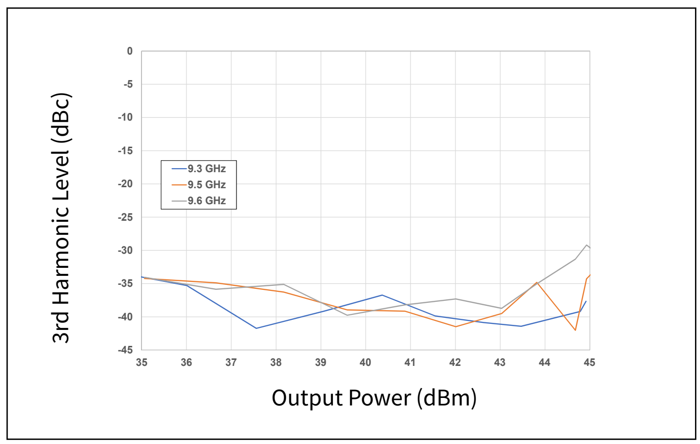


Figure 31. 3rd Harmonic vs Output Power as a Function of Frequency

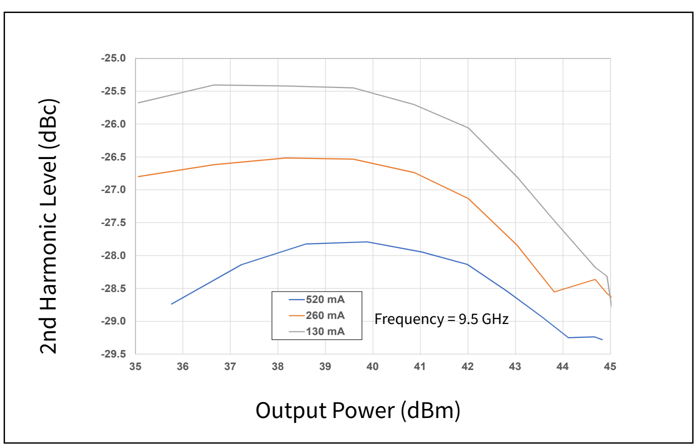


Figure 32. 2nd Harmonic vs Output Power as a Function of I_{DQ}

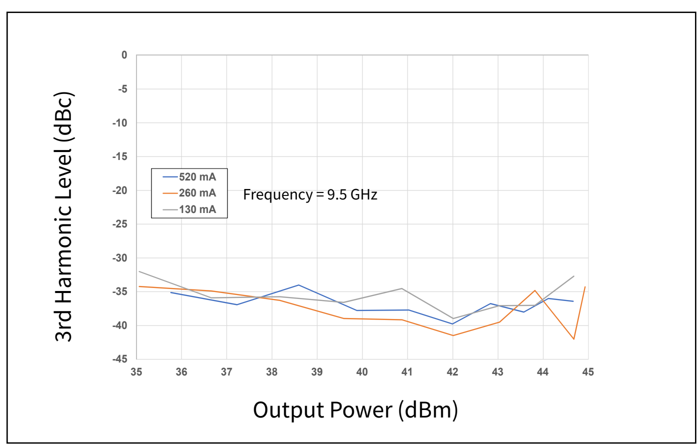


Figure 33. 3rd Harmonic vs Output Power as a Function of I_{DQ}

Typical Performance of the CMPA9396025S

Test conditions unless otherwise noted: V_D = 40 V, I_{DQ} = 260 mA, P_{IN} = -30 dBm, T_{BASE} = +25°C

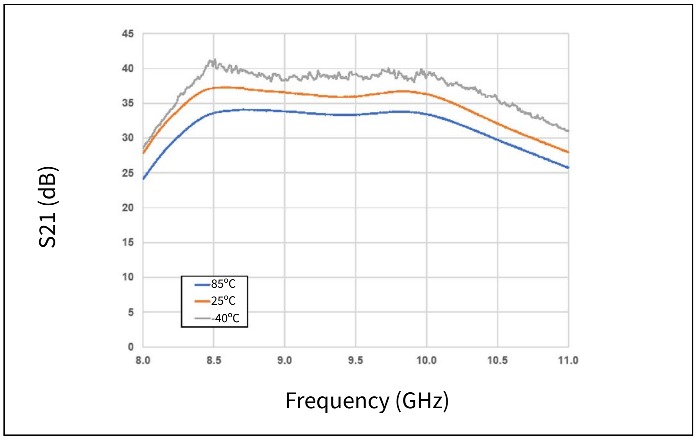


Figure 34. Gain vs Frequency as a Function of Temperature

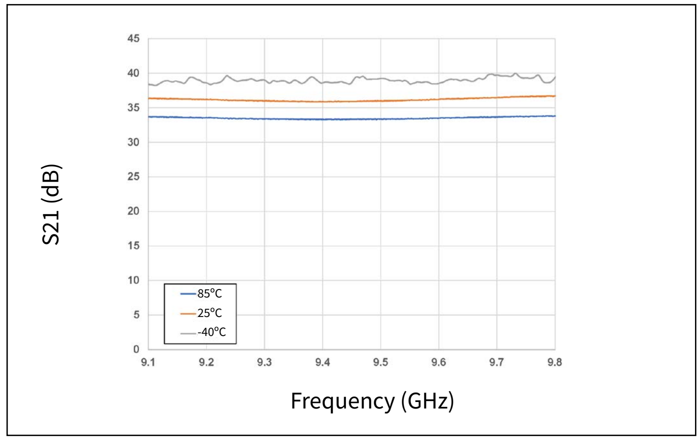


Figure 35. Gain vs Frequency as a Function of Temperature

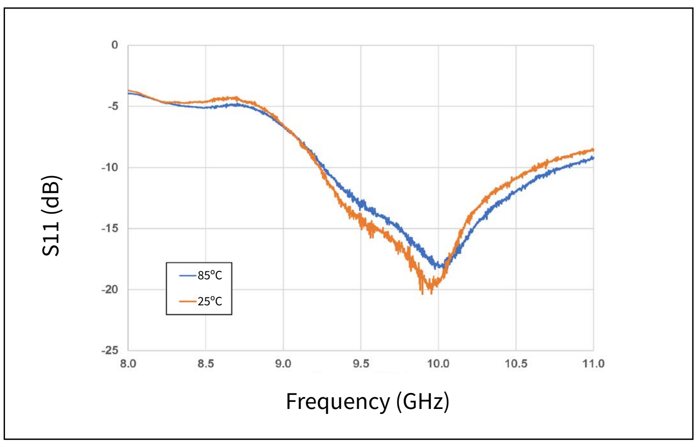


Figure 36. Input RL vs Frequency as a Function of Temperature

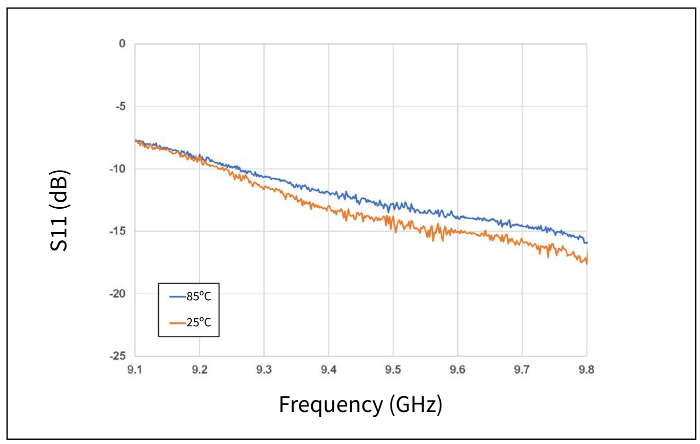


Figure 37. Input RL vs Frequency as a Function of Temperature

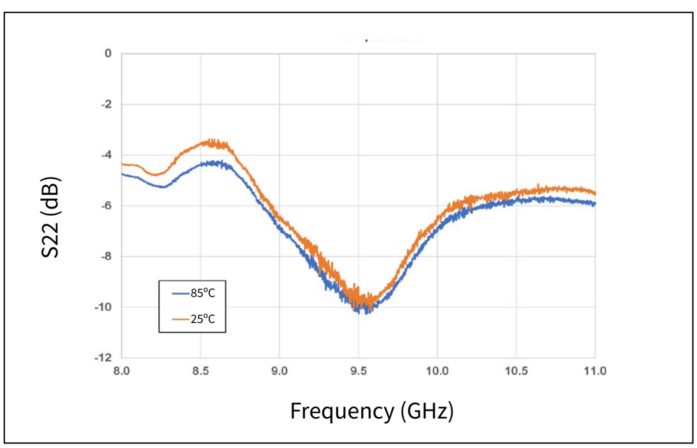


Figure 38. Output RL vs Frequency as a Function of Temperature

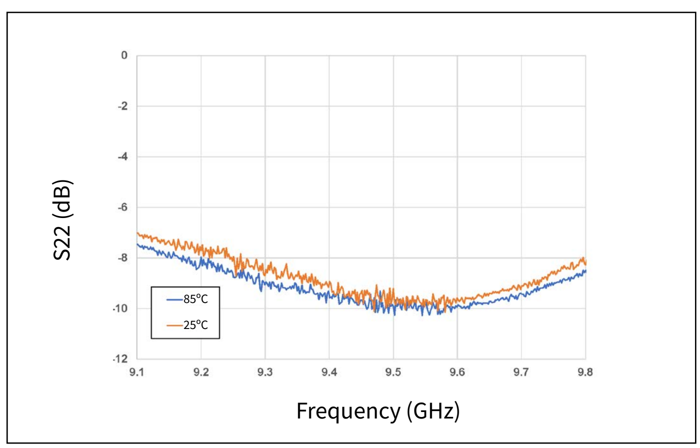


Figure 39. Output RL vs Frequency as a Function of Temperature

Typical Performance of the CMPA9396025S

Test conditions unless otherwise noted: V_D = 40 V, I_{DQ} = 260 mA, P_{IN} = -30 dBm, T_{BASE} = +25°C

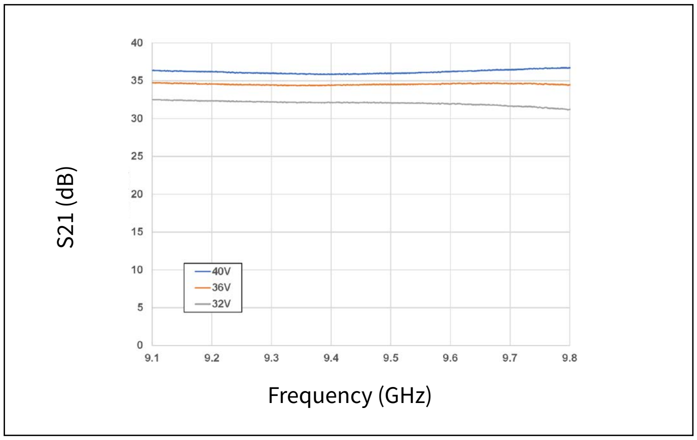


Figure 40. Gain vs Frequency as a Function of Voltage

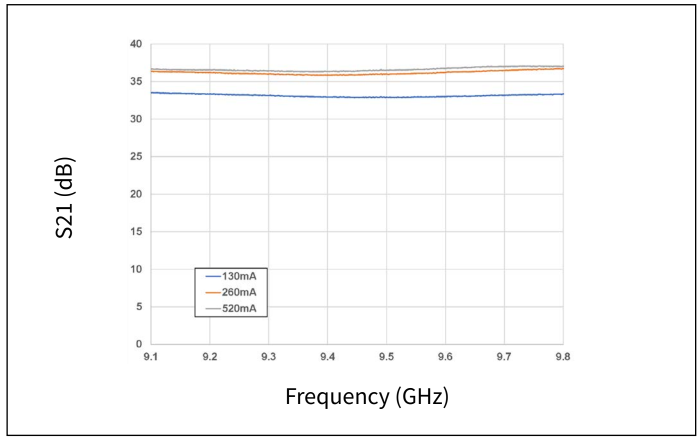


Figure 41. Gain vs Frequency as a Function of I_{DQ}

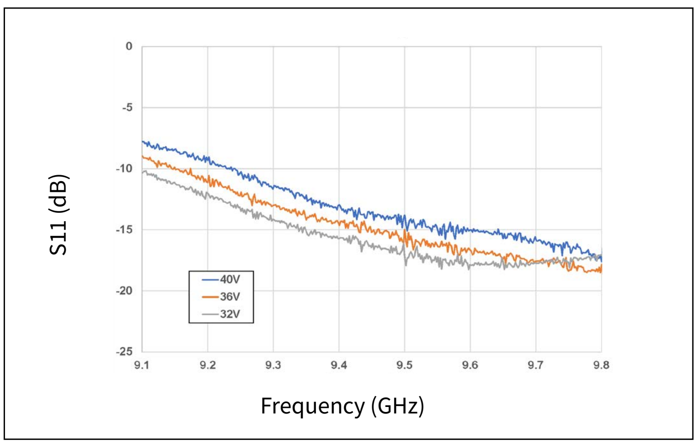


Figure 42. Input RL vs Frequency as a Function Voltage

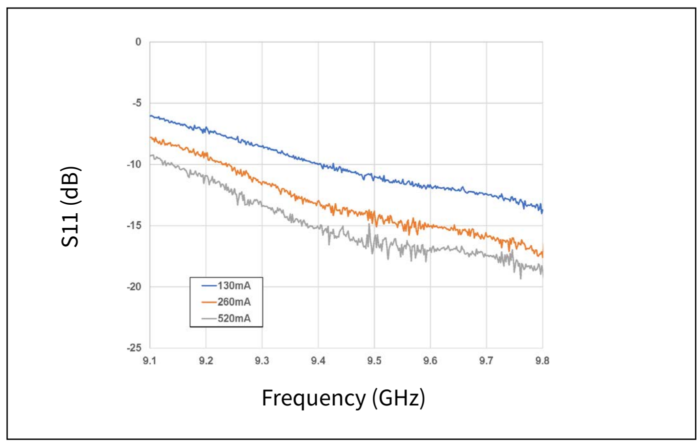


Figure 43. Input RL vs Frequency as a Function of I_{DQ}

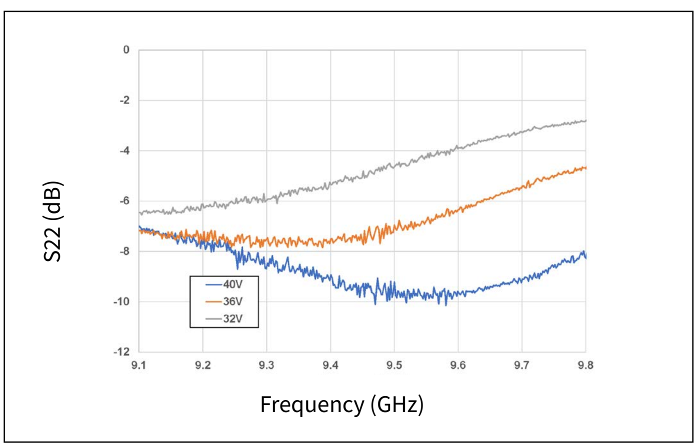


Figure 44. Output RL vs Frequency as a Function of Voltage

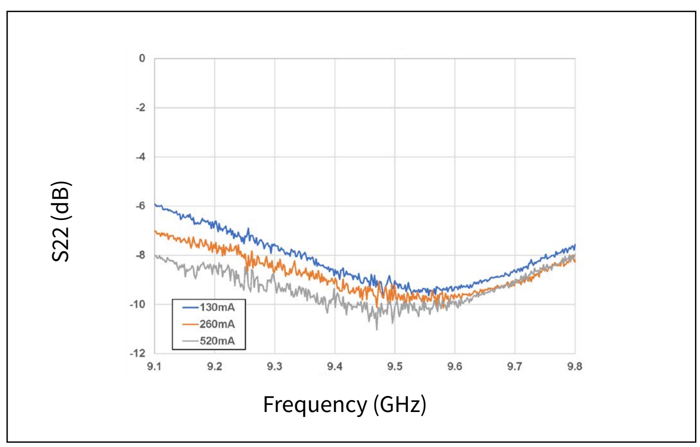
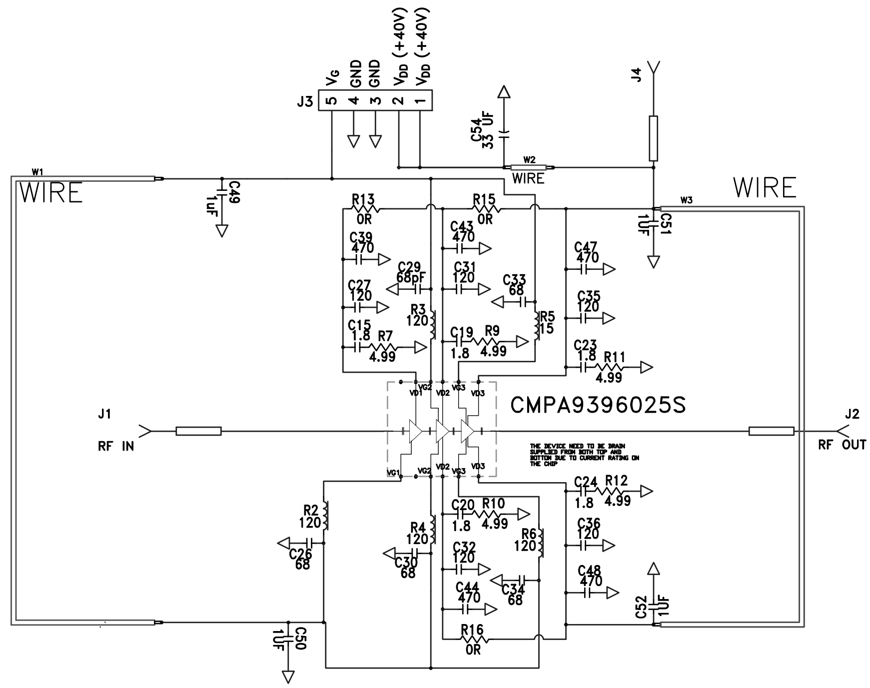
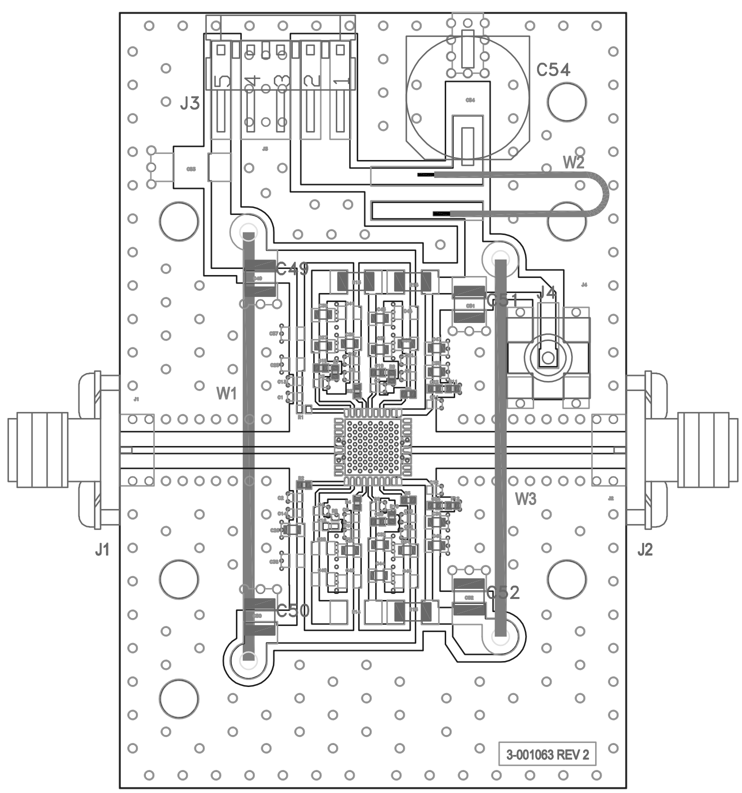


Figure 45. Output RL vs Frequency as a Function of I_{DQ}

CMPA9396025S-AMP1 Application Circuit



CMPA9396025S-AMP1 Evaluation Board Layout



CMPA9396025S-AMP1 Evaluation Board Bill of Materials

Designator	Description	Qty
C54	CAP, 33µF, 20%, G_{CASE}	1
C49, C50, C51, C52	CAP, 1.0µF, 100V, 10%, X7R, 1210	4
C39, C43, C44, C47, C48	CAP, 470pF, 5%, 100V, 0603, X7R	5
C26, C29, C30, C33, C34	CAP, 68pF, +/-5%pF, 0603, ATC	5
C27, C31, C32, C35, C36	CAP, 120pF, +/-5%, C0G, 0603, 100V	5
C15, C19, C20, C23, C24	CAP, 1.8pF, +/-0.05pF, ATC 600L, 0402	5
R2-R6	Ferrite bead, 120 OHM, 600mA, 0402	5
R7, R9-R12	RES 4.99 OHM, +/-1%, 1/16W, 0402	5
R13, R15, R16	RES 0.0 OHM, 1/16W, 1206 SMD	3
J1, J2	CONN, SMA, PANEL MOUNT JACK, FLANGE, 4-HOLE, BLUNT POST, 20MIL	2
J3	HEADER RT>PLZ .1CEN LK 5POS	1
J4	CONN, SMB, STRAIGHT JACK RECEPTACLE, SMT, 50 OHM, Au PLATED	1
W1	WIRE, BLACK, 20 AWG ~ 1.5”	1
W2	WIRE, BLACK, 20 AWG ~ 1.3”	1
W3	WIRE, BLACK, 20 AWG ~ 1.5”	1
	PCB, TEST FIXTURE, RF35, 0.010", 6X6 3-STAGE, QFN	1
	HEATSINK, 6X6 QFN, 3-STAGE 2.600 X 1.700 X 0.250	1
	2-56 SOC HD SCREW 3/16 SS	4
	#2 SPLIT LOCKWASHER SS	4
Q1	CMPA9396025S	1

Electrostatic Discharge (ESD) Classifications

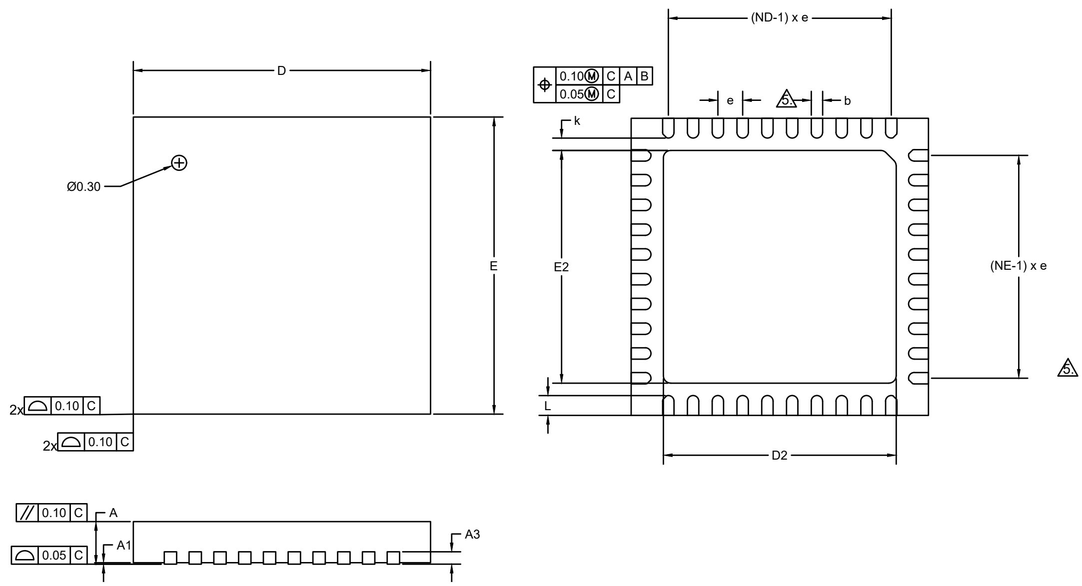
Parameter	Symbol	Class	Classification Level	Test Methodology
Human Body Model	HBM	1A	ANSI/ESDA/JEDEC JS-001 Table 3	JEDEC JESD22 A114-D
Charge Device Model	CDM	C0b	ANSI/ESDA/JEDEC JS-002 Table 3	JEDEC JESD22 C101-C

Moisture Sensitivity Level (MSL) Classification

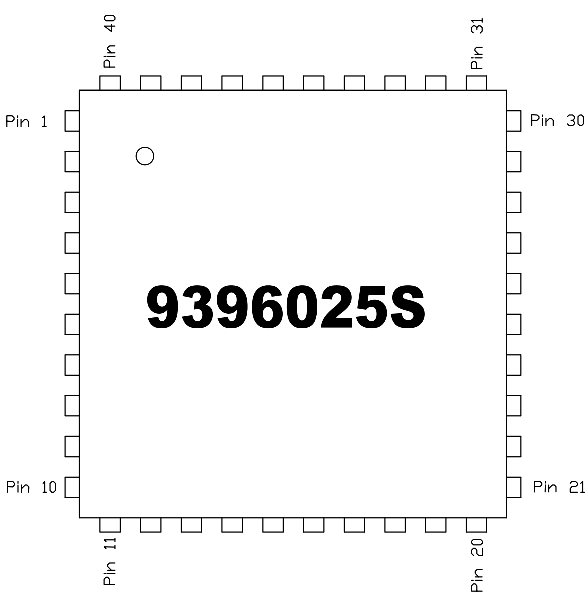
Parameter	Symbol	Level	Test Methodology
Moisture Sensitivity Level	MSL	3 (168 hours)	IPC/JEDEC J-STD-20

Product Dimensions CMPA9396025S (Package 6 x 6 QFN)

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M. - 1994
2. ALL DIMENSIONS ARE IN MILLIMETERS, 0 IS IN DEGREES
3. N IS THE TOTAL NUMBER OF TEMRINALS
4. DIMENSION b APPLIES TO THE METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP
5. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY
6. MAX. PACKAGE WARPAGE IS 0.05mm
7. MAXIMUM ALLOWABLE BURRS IS 0.076mm IN ALL DIRECTIONS
8. PIN #1 ID ON TOP WILL BE LASER MARKED
9. B ILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS
10. THIS DRAWING CONFORMS TO JEDEC REGISTERED OUTLINE MO-220
11. ALL PLATED SURFACES ARE TIN 0.010mm +/- 0.005mm



SYM	MIN	NOM	MAX	NOTE
A	0.80	0.86	0.91	
A1	0.00	0.03	0.06	
A3		0.25 REF		
k		0.15 MIN		
D		6.0 BSC		
E		6.0 BSC		
e		0.50 BSC		
N		40		3
ND		10		5
NE		10		5
L	0.35	0.40	0.46	
b	0.20	0.23	0.28	4
D2	4.60	4.70	4.80	
E2	4.60	4.70	4.80	



PIN	DESC.	PIN	DESC.	PIN	DESC.
1	NC	15	VD2A	29	NC
2	NC	16	NC	30	NC
3	NC	17	VG3A	31	VD3B
4	NC	18	NC	32	VD3B
5	RFGND	19	VD3A	33	NC
6	RFIN	20	VD3A	34	VG3B
7	RFGND	21	NC	35	NC
8	NC	22	NC	36	VD2B
9	NC	23	NC	37	VG2B
10	NC	24	RFGND	38	NC
11	VG1A	25	RFOUT	39	VD1B
12	NC	26	RFGND	40	NC
13	NC	27	NC		
14	VG2A	28	NC		

Part Number System

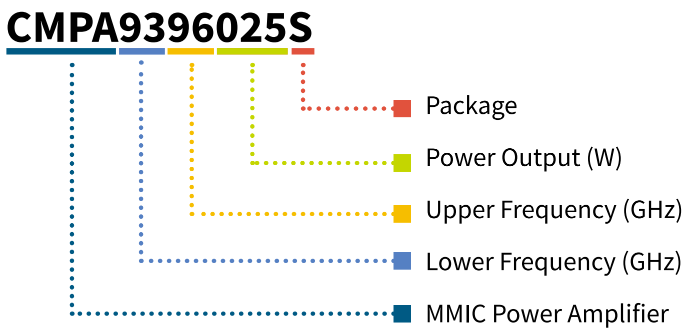


Table 1.

Parameter	Value	Units
Lower Frequency	9.3	GHz
Upper Frequency	9.6	
Power Output	25	W
Package	Surface Mount	–

Note:
[1] Alpha characters used in frequency code indicate a value greater than 9.9 GHz. See Table 2 for value.

Table 2.

Character Code	Code Value
A	0
B	1
C	2
D	3
E	4
F	5
G	6
H	7
J	8
K	9
Examples	1A = 10.0 GHz 2H = 27.0 GHz

Product Ordering Information

Order Number	Description	Unit of Measure	Image
CMPA9396025S	Packaged GaN MMIC PA	Each	
CMPA9396025S-AMP1	Evaluation Board with GaN MMIC Installed	Each	

Notes & Disclaimer

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