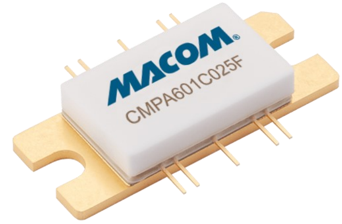
GaN High Power Amplifier, 40 W
6 - 12 GHz

CMPA601C025F
Rev. V1

Features
- Saturated Power: 40 W
- Power Added Efficiency: 30%
- Large Signal Gain: 24 dB
- Small Signal Gain: 34 dB
- Input Return Loss: -5 dB
- Output Return Loss: -5 dB
- CW Operation

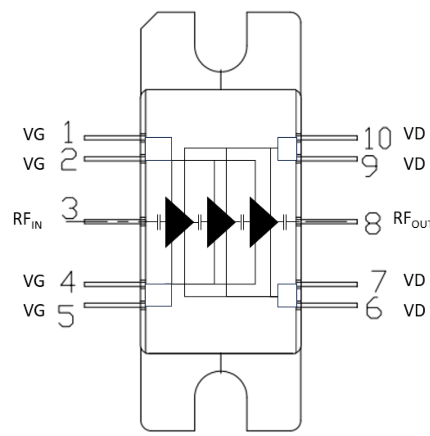


Applications
- Electronic Warfare
- X-band Radar

Description
The CMPA601C025F is a 40 W package MMIC HPA utilizing a high performance, 0.25 µm GaN-on-SiC production process. The CMPA601C025F operates from 6 - 12 GHz and supports a variety of both defense and commercial related applications. The CMPA601C025F achieves 40 W of saturated output power with 24 dB of large signal gain and typically 30% power-added efficiency under CW operation.

Packaged in a bolt-down, flange package, the CMPA601C025F provides superior RF performance and thermal management allowing customers to improve SWaP-C benchmarks in their next generation systems.

Functional Schematic



Ordering Information

Part Number	Package (MOQ/ Mult)
CMPA601C025F	Tray (10/10)
CMPA601C025F-AMP	Sample Board (1/1)

Pin Configuration[1]

Pin #	Function
1, 2, 4, 5	Gate Bias
6, 7, 9, 10	Drain Bias
3	RF Input
8	RF Output

1. The base of the package bottom must be connected to RF, DC and thermal ground.

DC-0030738

RF Electrical Specifications: V_D = 28 V, I_{DQ} = 2 A, CW, T_C = 25°C, Z_0 = 50 Ω

Parameter	Test Conditions	Frequency (GHz)	Units	Min.	Typ.	Max.
Output Power	P_{IN} = 22 dBm	6 9.5 12	dBm	45.5 45.5 43.0	46.0 46.5 45.5	—
Power Added Efficiency		6 9.5 12	%	23.0 26.0 15.5	25.0 33.0 28.0	—
Large Signal Gain		6 9.5 12	dB	—	24.0 24.5 23.5	—
Small Signal Gain	P_{IN} = -20 dBm	6 9.5 12	dB	28 28 25	35 35 30	—
Input Return Loss		6 - 12	dB	—	-5	—
Output Return Loss		6 - 12	dB	—	-5	—

DC Electrical Specifications

Parameter	Units	Min.	Typ.	Max.
Drain Voltage	V	—	28	—
Gate Voltage	V	—	-2.45	—
Quiescent Drain Current	A	—	2	—
Saturated Drain Current	A	—	5.0	—

Recommended Operating Conditions

Parameter	Symbol	Unit	Min.	Typ.	Max.
Input Power	P_{IN}	dBm	—	22	—
Drain Voltage	V_D	V	—	28	—
Gate Voltage	V_G	V	—	-2.45	—
Quiescent Drain Current	I_{DQ}	A	—	2	—
Operating Temperature	T_C	°C	-40	—	+85

Absolute Maximum Ratings[2,3]

Parameter	Symbol	Unit	Min.	Max.
Input Power	P_{IN}	dBm	—	24
Drain to Source Voltage	V_{DS}	V	—	84
Drain Voltage	V_D	V	—	28
Gate Voltage	V_G	V	-8	+2
Drain Current	I_D	A	—	7.1
Gate Current	I_G	mA	—	23
Dissipated Power @ +85°C	P_{DISS}	W	—	164.7
VSWR			—	7:1
Junction Temperature (MTTF > 1E6 Hrs)	T_J	°C	—	+225
Storage Temperature	T_{STG}	°C	-55	+150
Mounting Temperature (30 seconds)	T_M	°C	—	+260
Screw Torque	τ	in-oz	—	40

2. Exceeding any one or combination of these limits may cause permanent damage to this device.
3. MACOM does not recommend sustained operation near these survivability limits.

Handling Procedures

Please observe the following precautions to avoid damage:

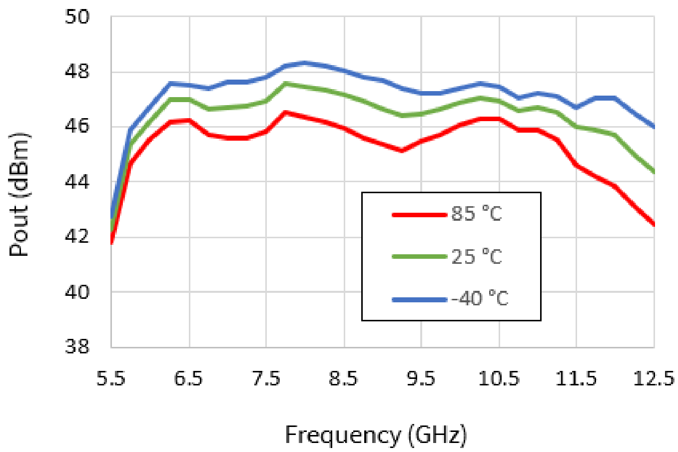
Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM class 1A and CDM class C3 devices.

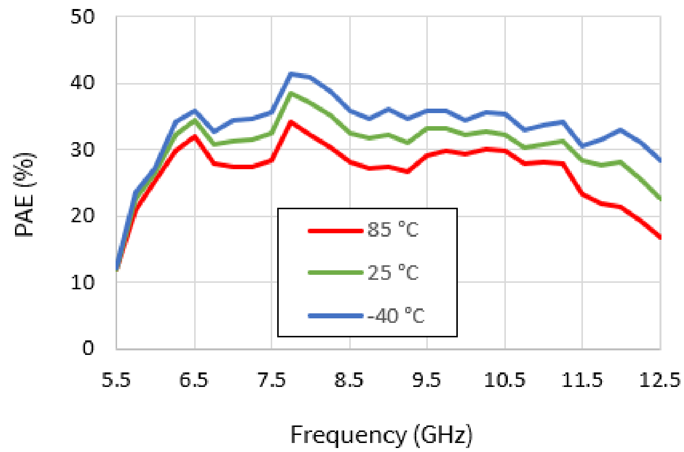
Typical Performance Curves - Large Signal over Temperature

V_D = 28 V, I_{DQ} = 2.0 A, CW, P_{IN} = 22 dBm

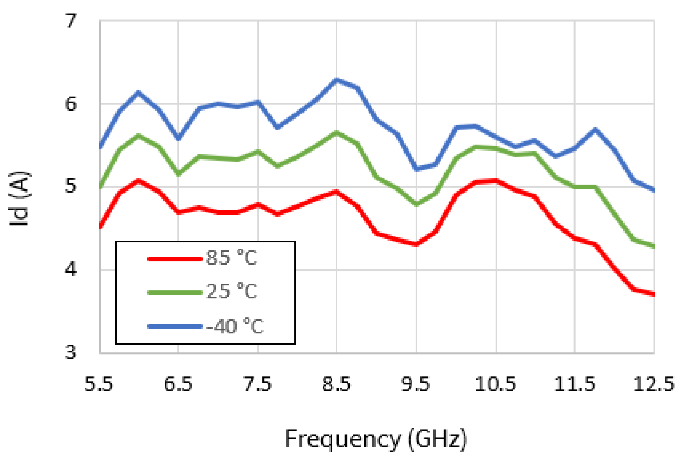
Output Power vs. Frequency



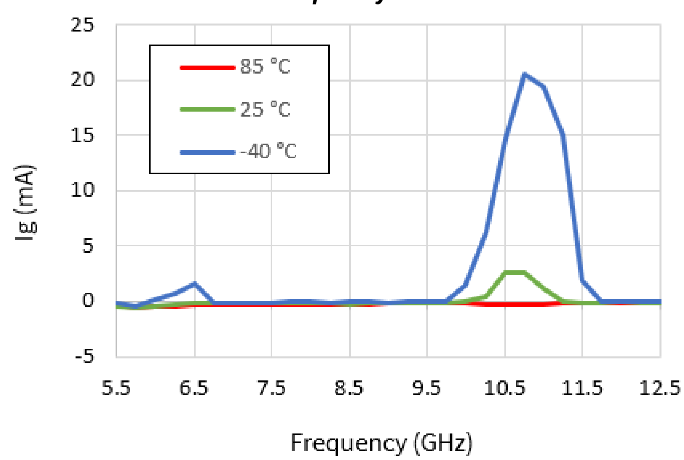
Power Added Efficiency vs. Frequency



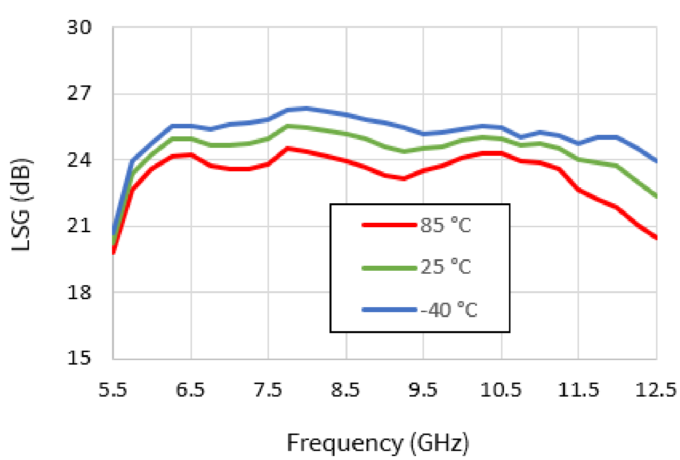
Drain Current vs. Frequency



Gate Current vs. Frequency



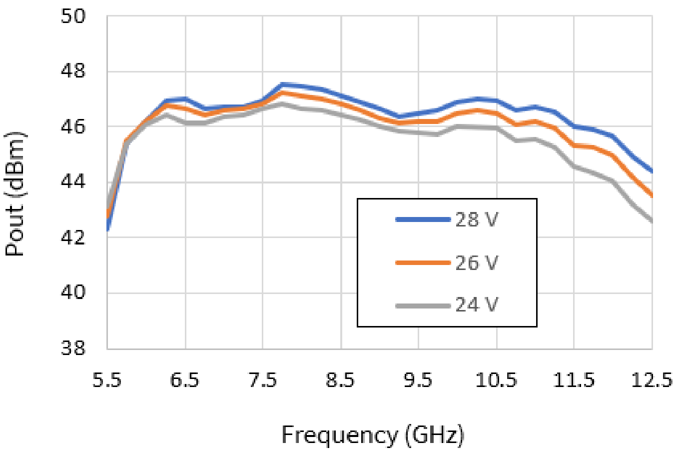
Large Signal Gain vs. Frequency



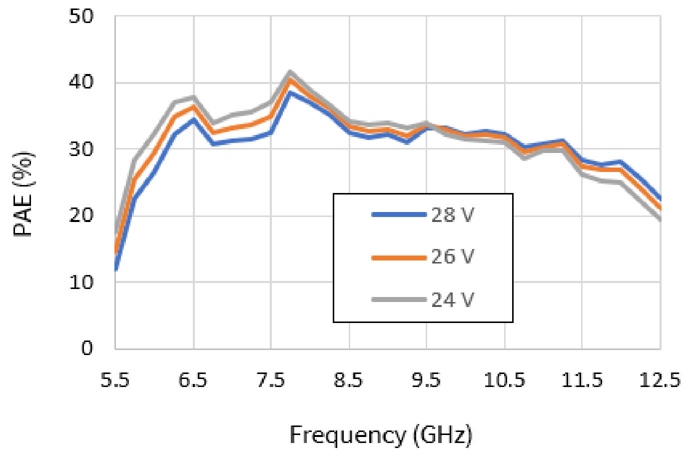
Typical Performance Curves - Large Signal over V_D

I_{DQ} = 2.0 A, CW, P_{IN} = 22 dBm, T_C = 25°C

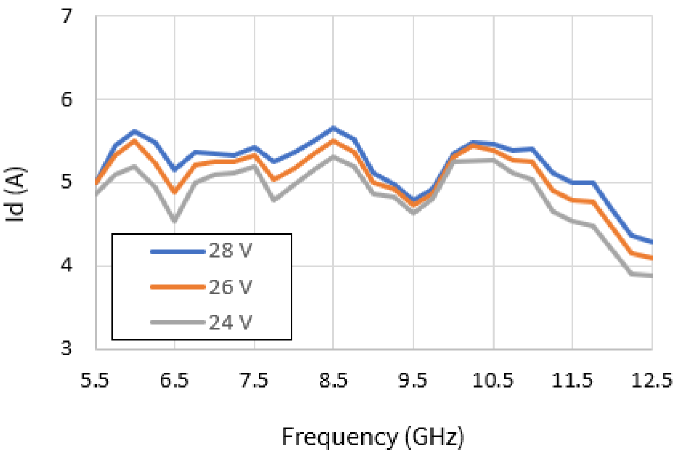
Output Power vs. Frequency



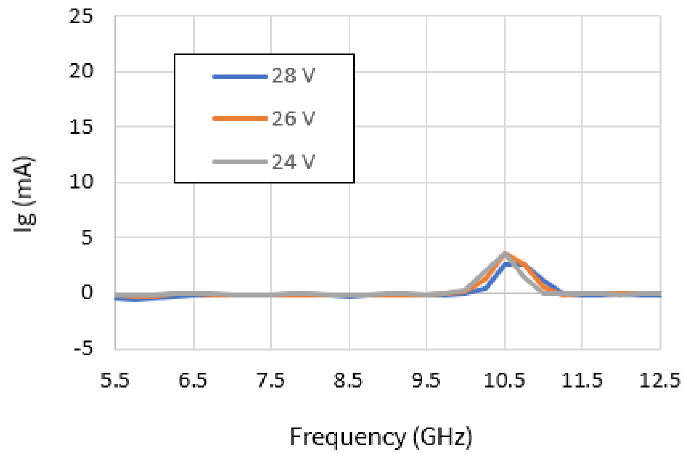
Power Added Efficiency vs. Frequency



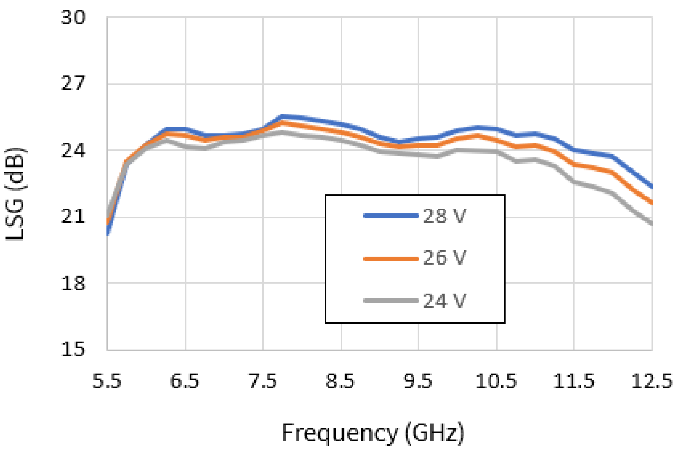
Drain Current vs. Frequency



Gate Current vs. Frequency



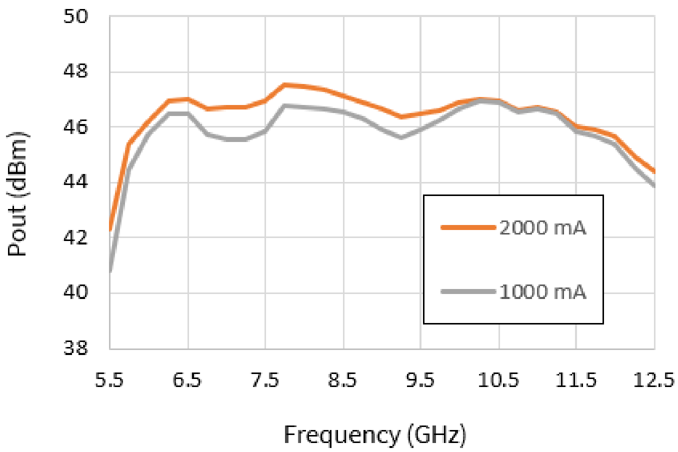
Large Signal Gain vs. Frequency



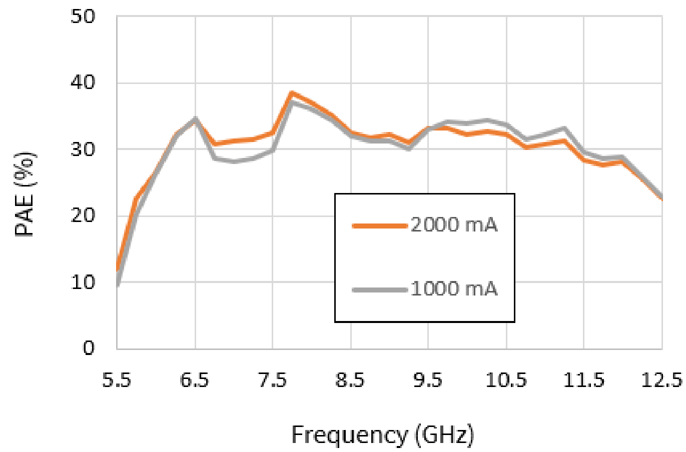
Typical Performance Curves - Large Signal over I_{DQ}

V_D = 28 V, CW, P_{IN} = 22 dBm, T_C = 25°C

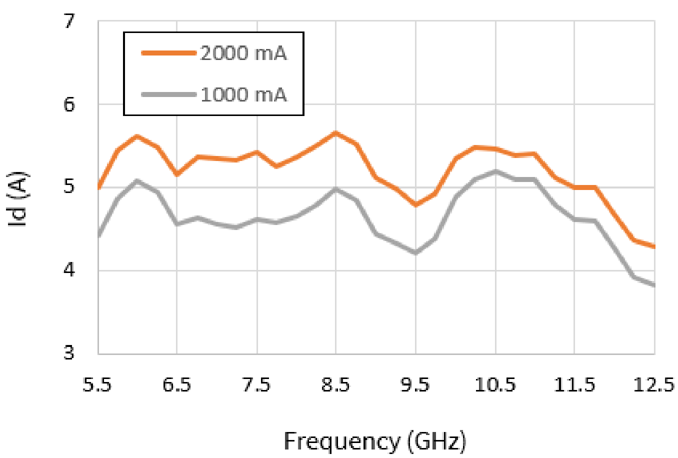
Output Power vs. Frequency



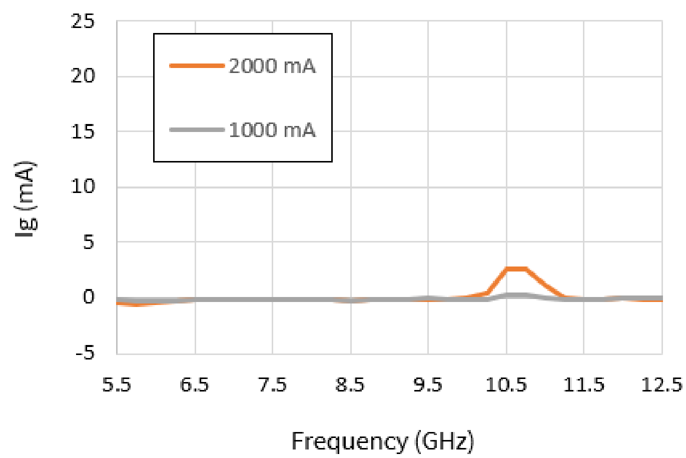
Power Added Efficiency vs. Frequency



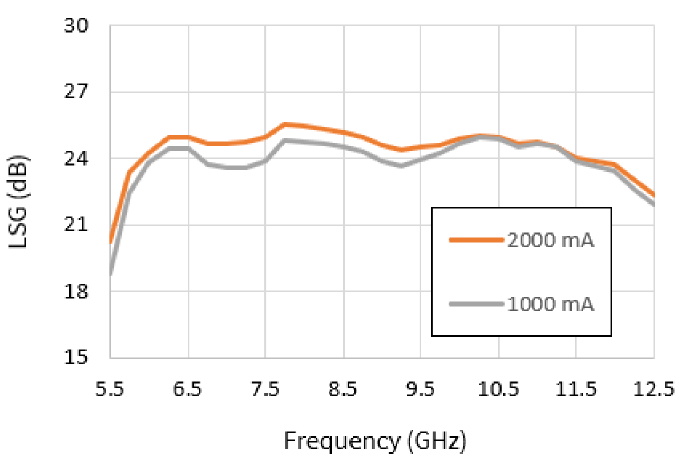
Drain Current vs. Frequency



Gate Current vs. Frequency



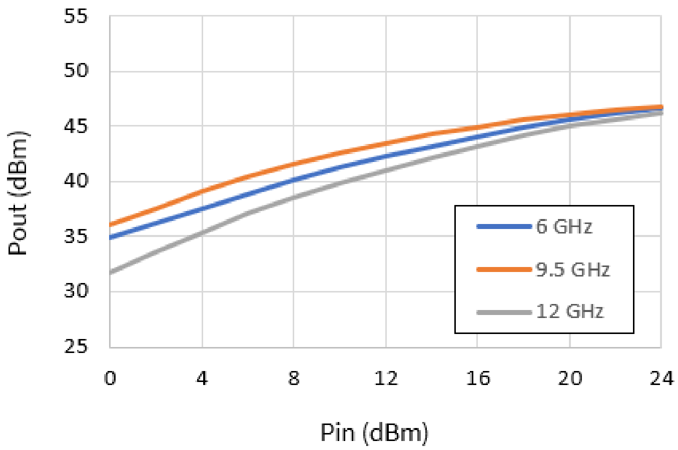
Large Signal Gain vs. Frequency



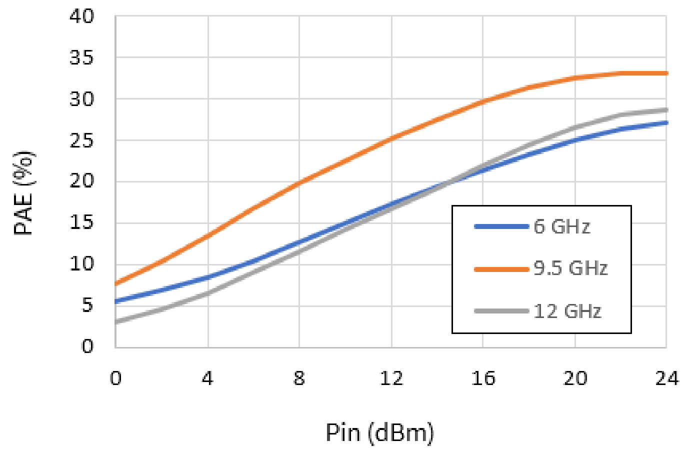
Typical Performance Curves - Drive-Up over Frequency

V_D = 28 V, I_{DQ} = 2.0 A, CW, T_C = 25°C

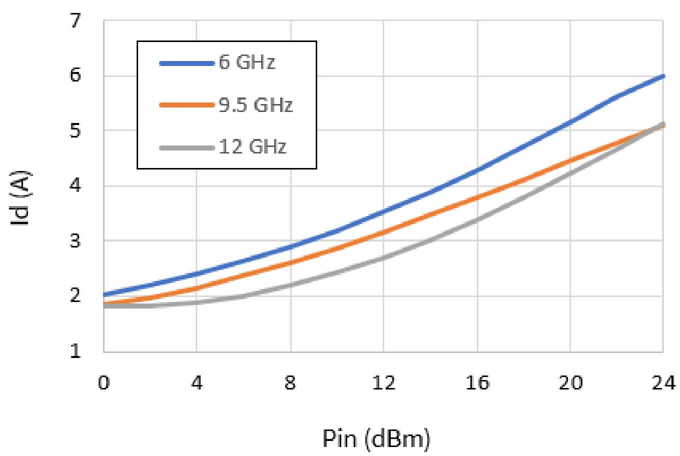
Output Power vs. Input Power



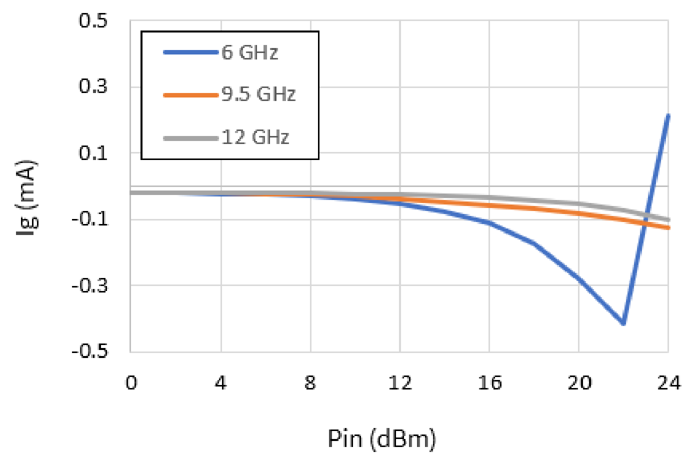
Power Added Efficiency vs. Input Power



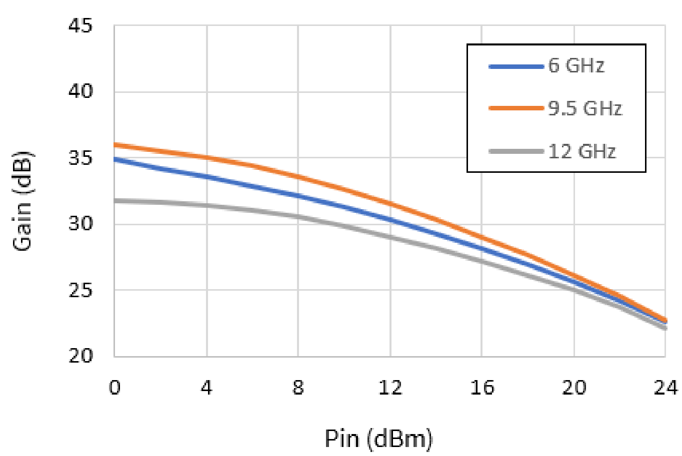
Drain Current vs. Input Power



Gate Current vs. Input Power



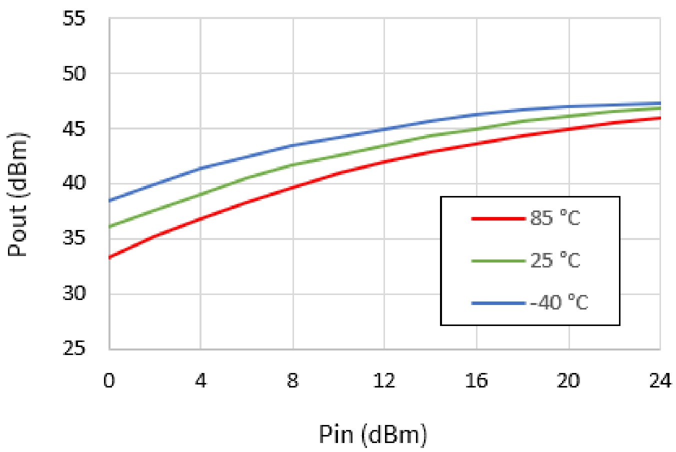
Gain vs. Input Power



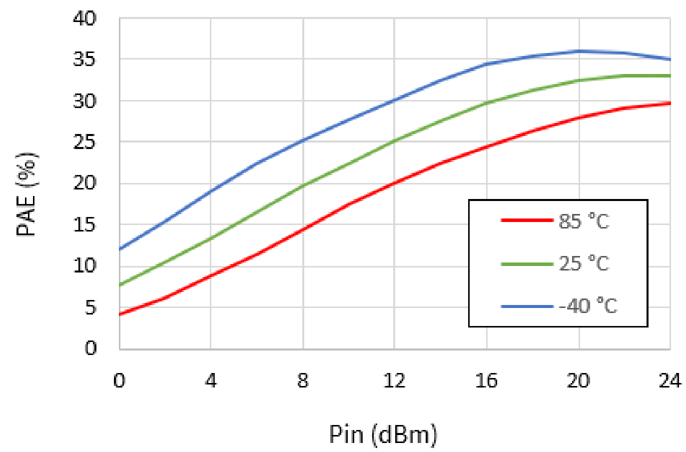
Typical Performance Curves - Drive-Up over Temperature

V_D = 28 V, I_{DQ} = 2.0 A, CW, Frequency = 9.5 GHz

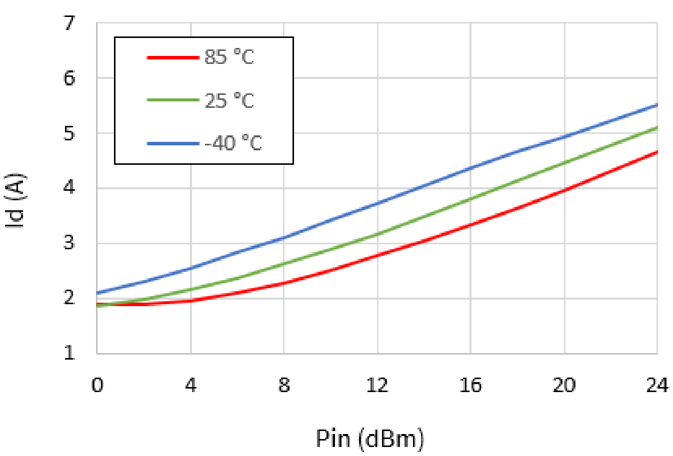
Output Power vs. Input Power



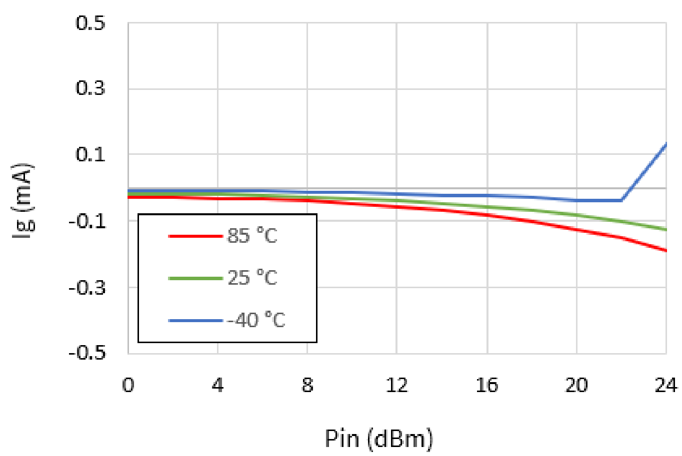
Power Added Efficiency vs. Input Power



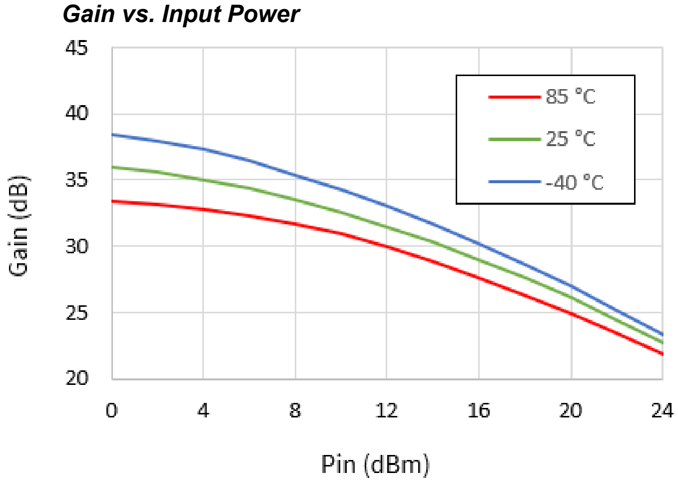
Drain Current vs. Input Power



Gate Current vs. Input Power



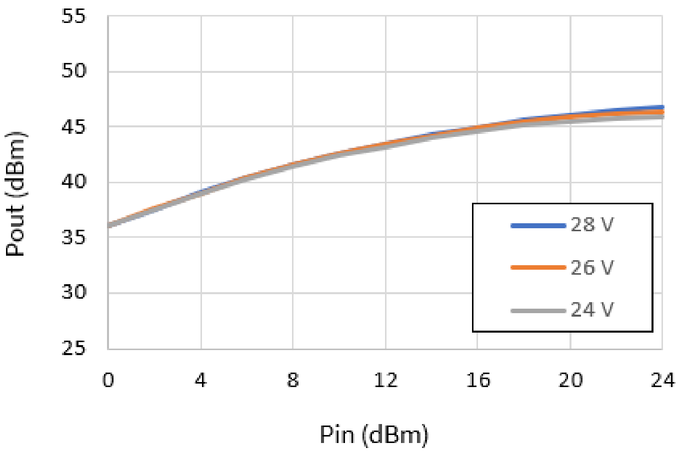
Gain vs. Input Power



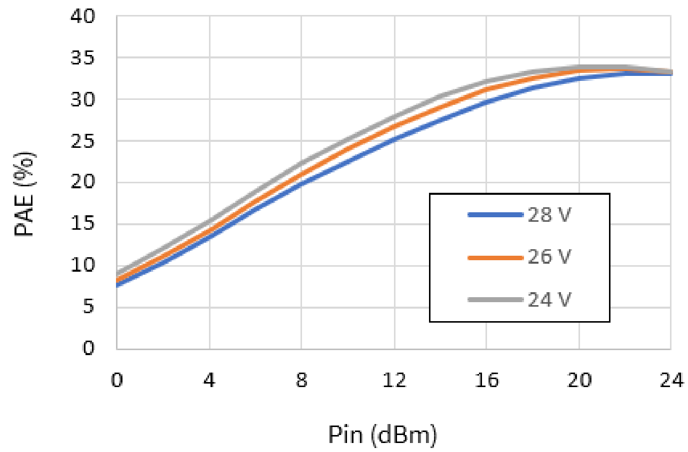
Typical Performance Curves - Drive-Up over V_D

I_{DQ} = 2.0 A, CW, Frequency = 9.5 GHz, T_C = 25°C

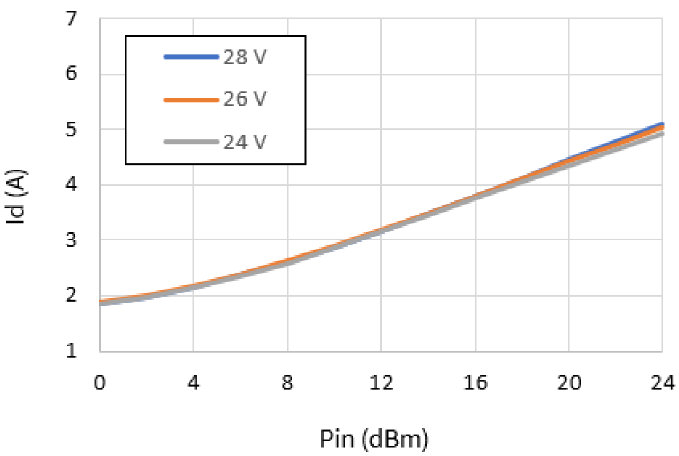
Output Power vs. Input Power



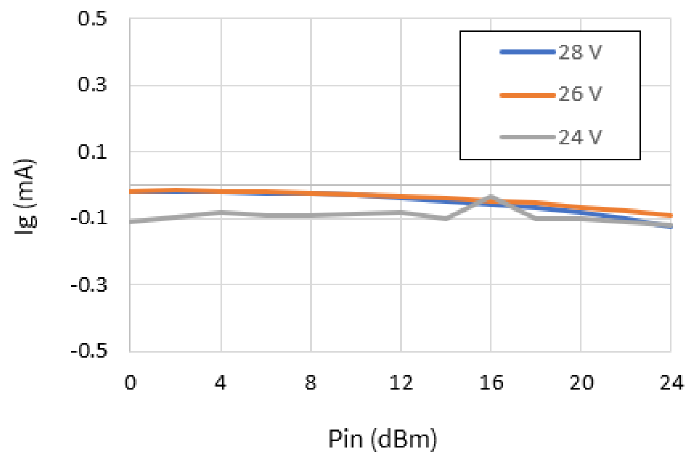
Power Added Efficiency vs. Input Power



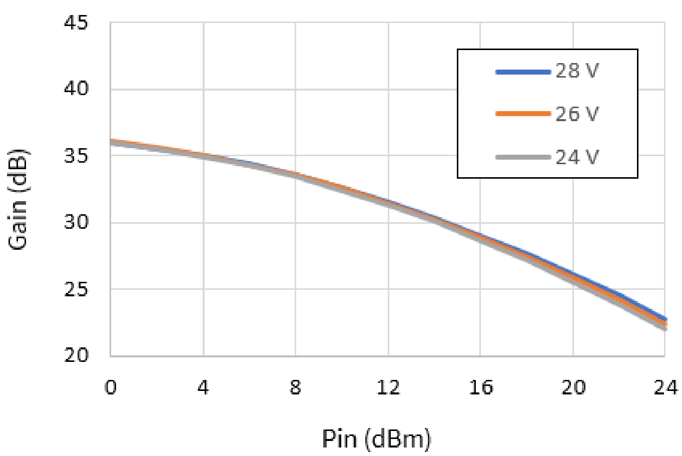
Drain Current vs. Input Power



Gate Current vs. Input Power



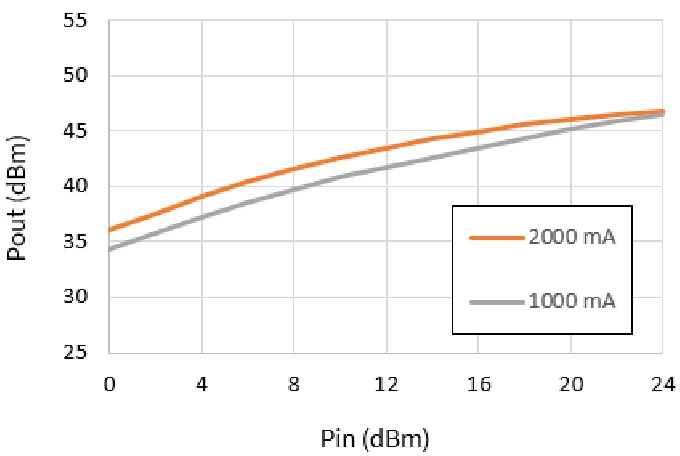
Gain vs. Input Power



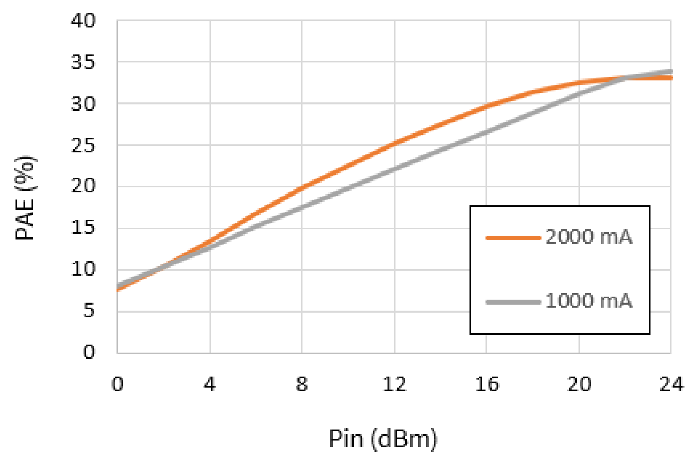
Typical Performance Curves - Drive-Up over I_{DQ}

V_D = 28 V, CW, Frequency = 9.5 GHz, T_C = 25°C

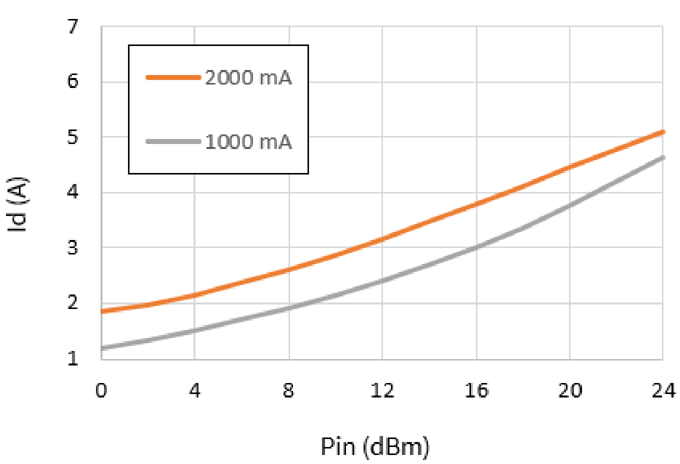
S21 vs. Frequency over Temperature @ V_D = 28 V



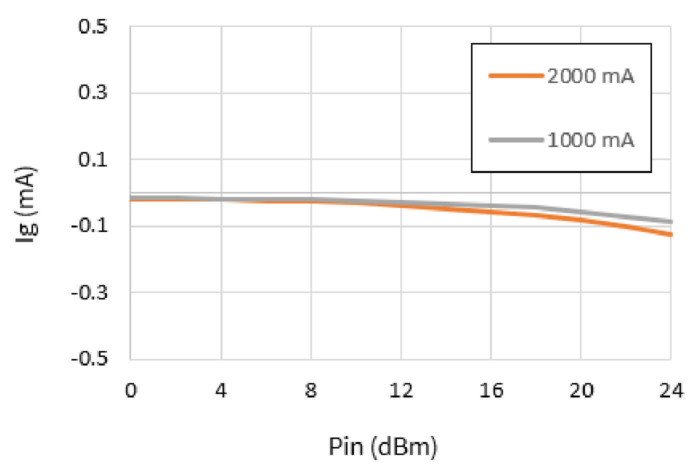
S21 vs. Frequency over V_D @ 25°C



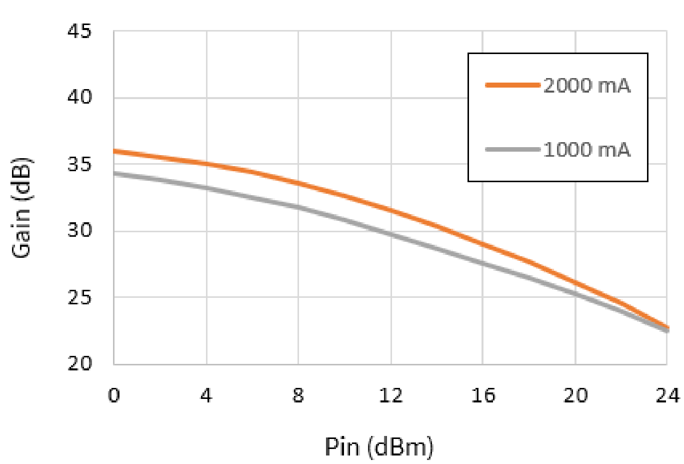
S11 vs. Frequency over Temperature @ V_D = 28 V



S11 vs. Frequency over V_D @ 25°C



S22 vs. Frequency over Temperature @ V_D = 28 V

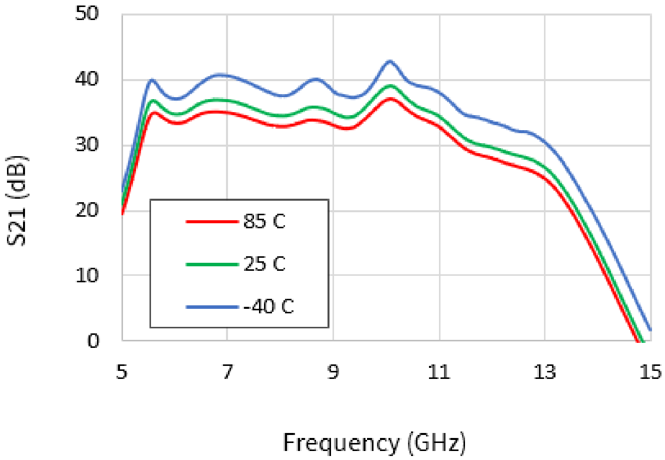


S22 vs. Frequency over V_D @ 25°C

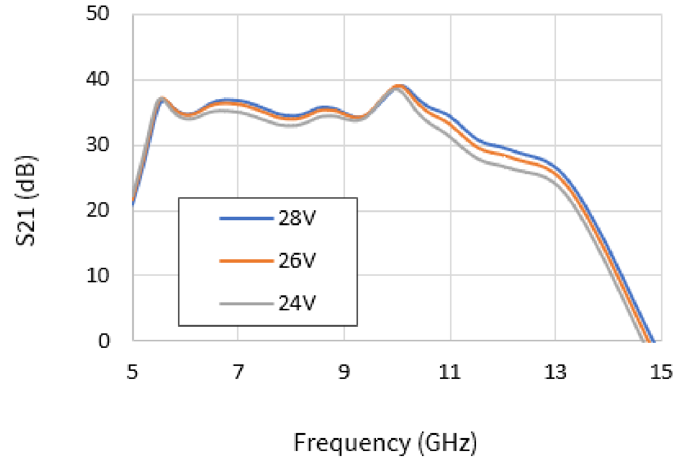
Typical Performance Curves - Small Signal over Temperature and V_D

I_{DQ} = 2.0 A, CW, P_{IN} = -20 dBm

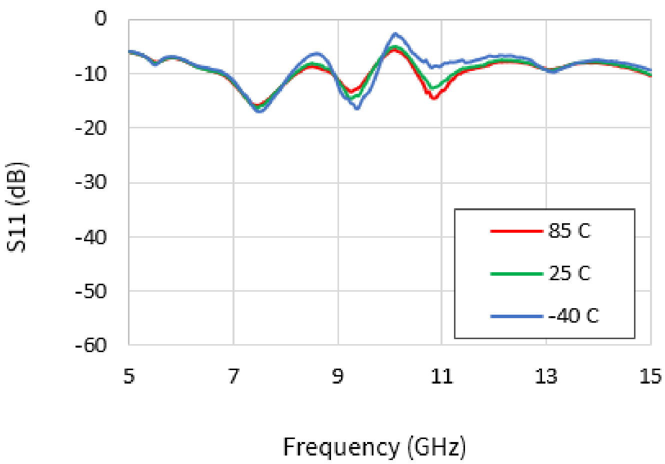
S21 vs. Frequency over Temperature @ V_D = 22 V



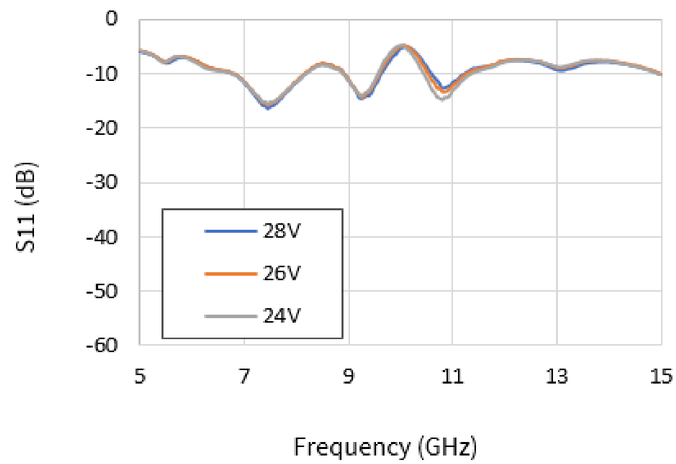
S21 vs. Frequency over V_D @ 25°C



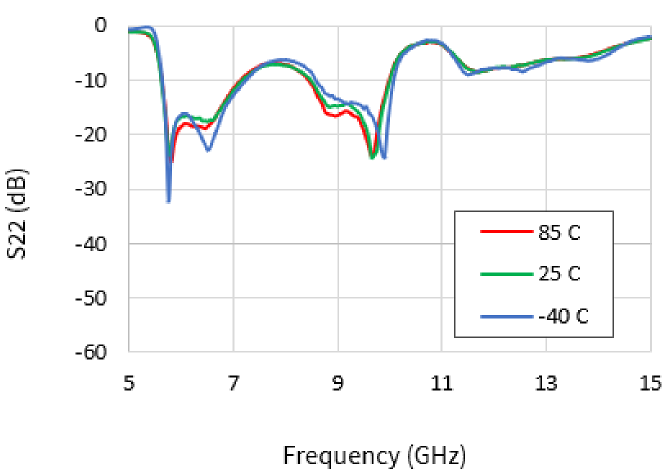
S11 vs. Frequency over Temperature @ V_D = 22 V



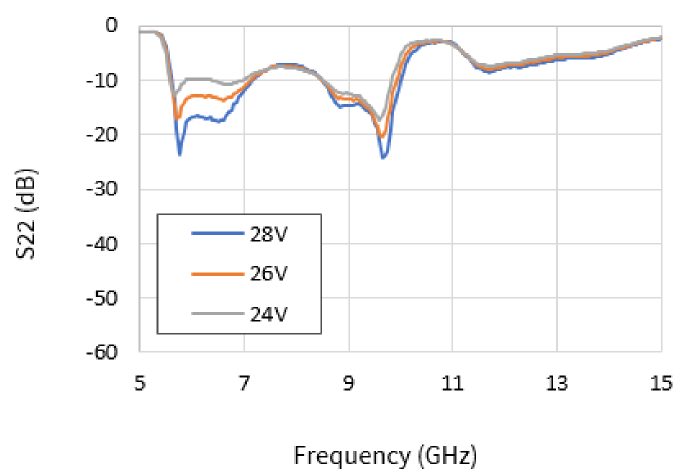
S11 vs. Frequency over V_D @ 25°C



S22 vs. Frequency over Temperature @ V_D = 22 V



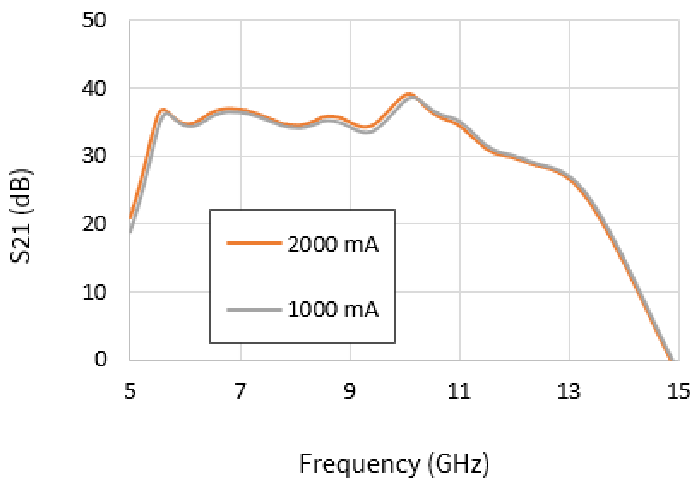
S22 vs. Frequency over V_D @ 25°C



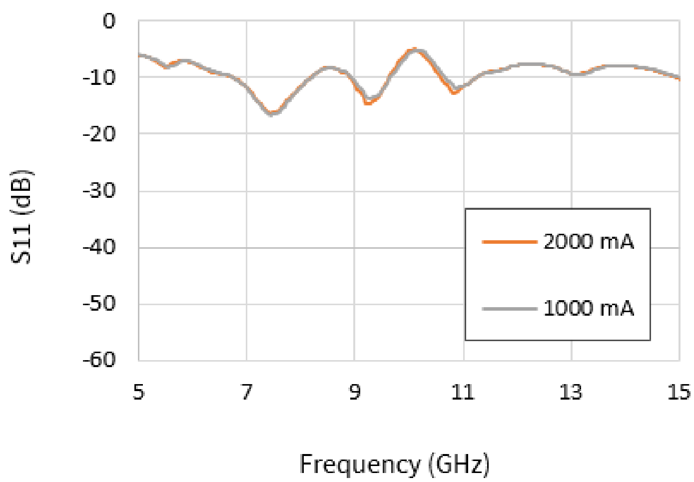
Typical Performance Curves - Small Signal over I_{DQ}

V_D = 28 V, CW, P_{IN} = -20 dBm, T_C = 25°C

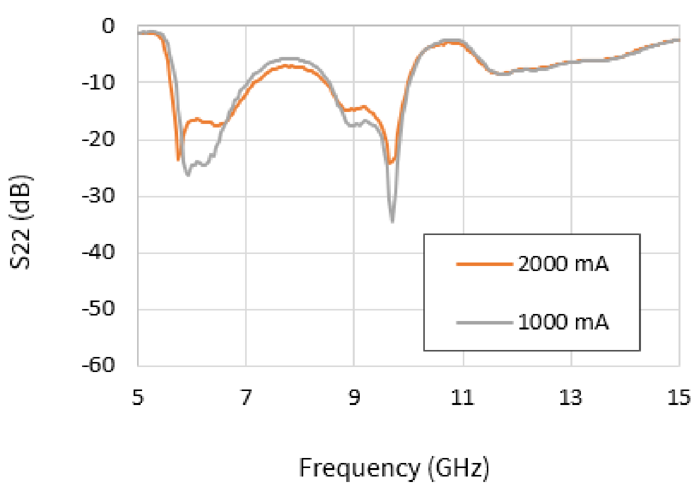
S21 vs. Frequency over I_{DQ}



S11 vs. Frequency over I_{DQ}



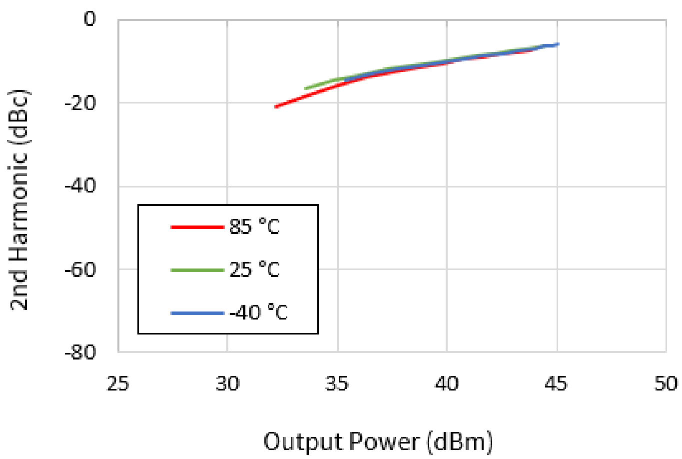
S22 vs. Frequency over I_{DQ}



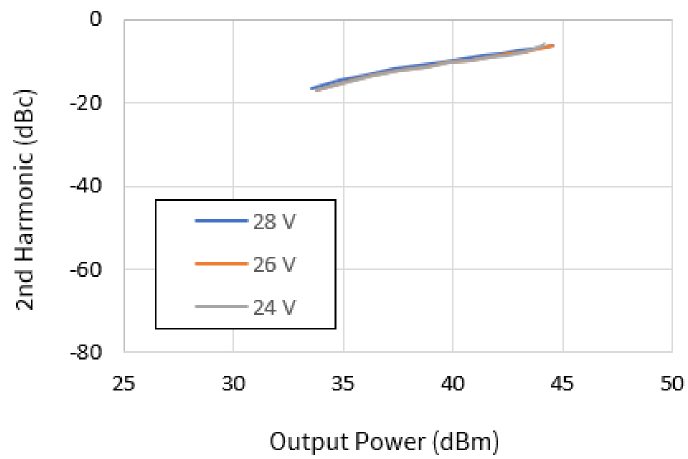
Typical Performance Curves - Harmonics over Temperature and V_D

V_D = 28 V, I_{DQ} = 2.0 A, CW, T_C = 25°C (unless otherwise noted)

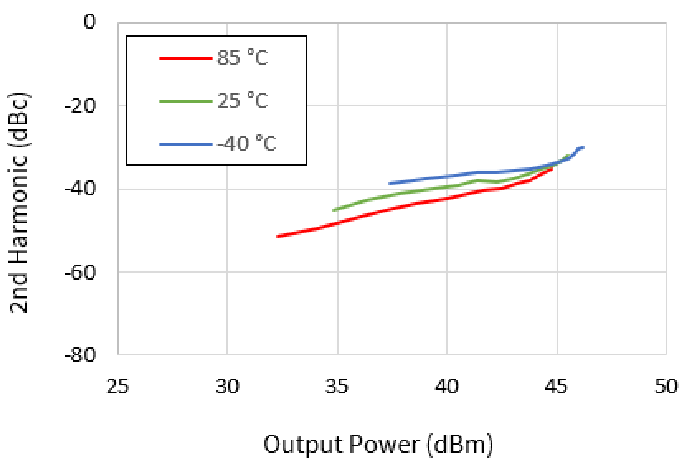
2f vs. Output Power over Temperature @ 6.0 GHz



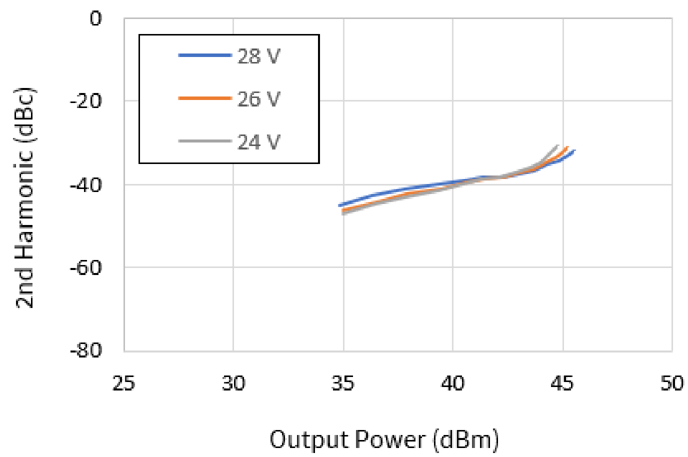
2f vs. Output Power over V_D @ 6.0 GHz



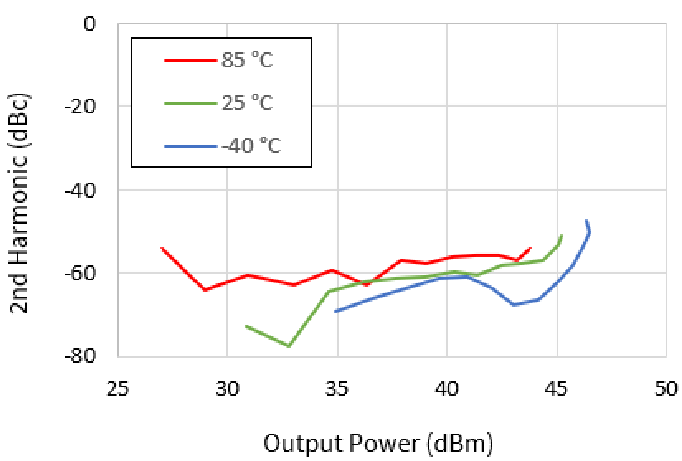
2f vs. Output Power over Temperature @ 9.5 GHz



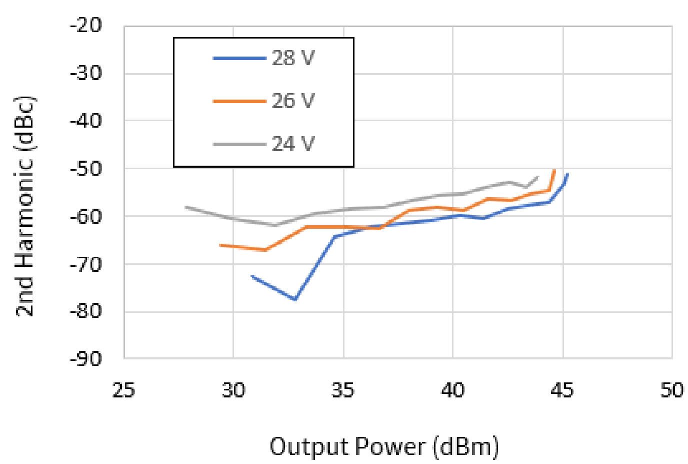
2f vs. Output Power over V_D @ 9.5 GHz



2f vs. Output Power over Temperature @ 12.0 GHz



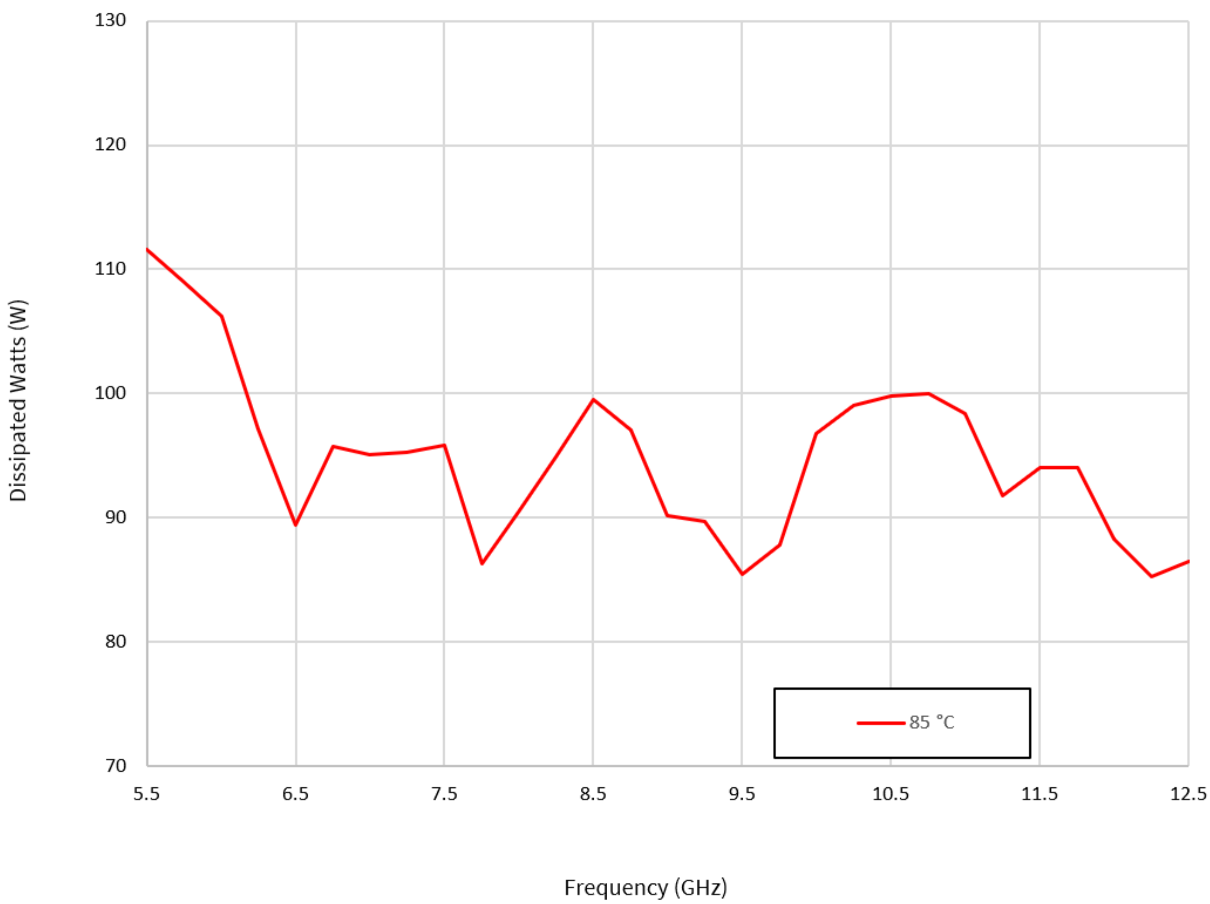
2f vs. Output Power over V_D @ 12.0 GHz



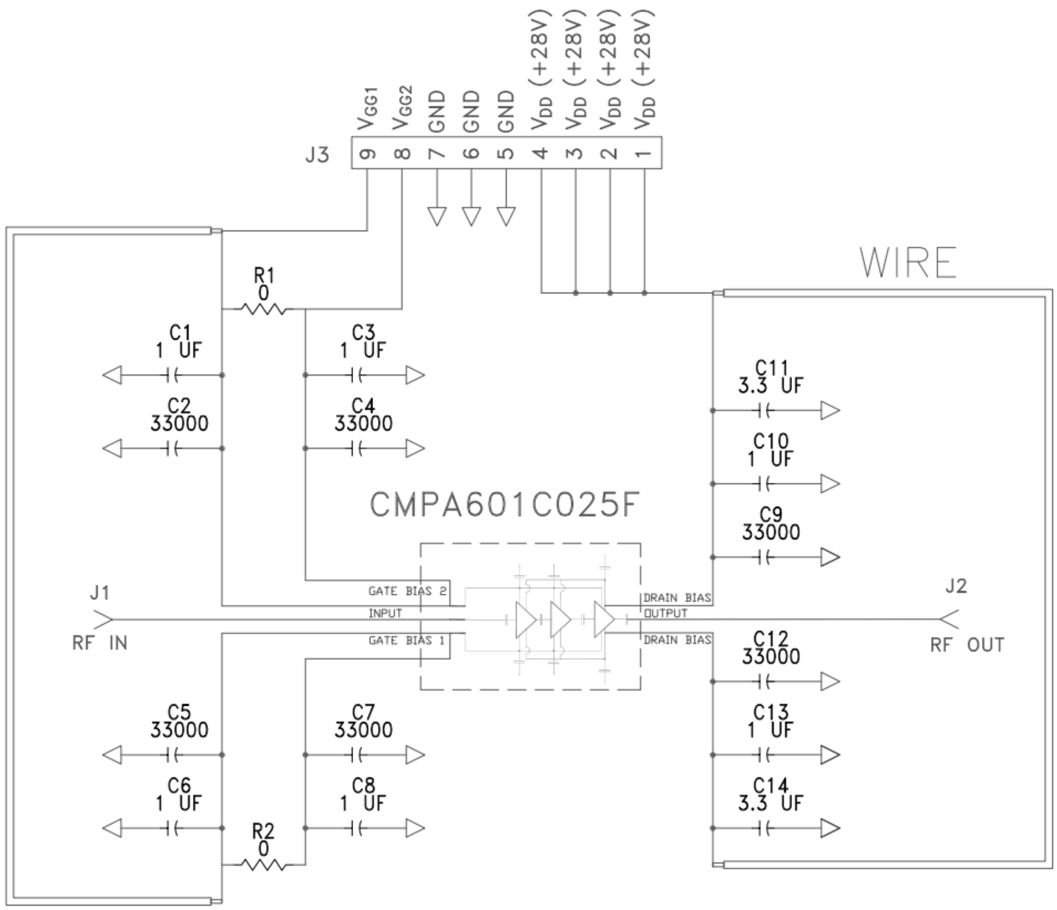
Thermal Characteristics

Parameter	Operating Conditions	Value
Operating Junction Temperature (T_J)	Freq = 9.5 GHz, V_D = 28 V, I_{DQ} = 2.0 A, I_{DRIVE} = 4.30 A, P_{IN} = 22 dBm, P_{OUT} = 45.45 dBm, P_{DISS} = 84.42 W, T_{CASE} =85°C, CW	156.8ºC
Thermal Resistance, Junction to Case ($R_{θJC}$)		0.85

Power Dissipation vs. Frequency (T_C = 85°C)



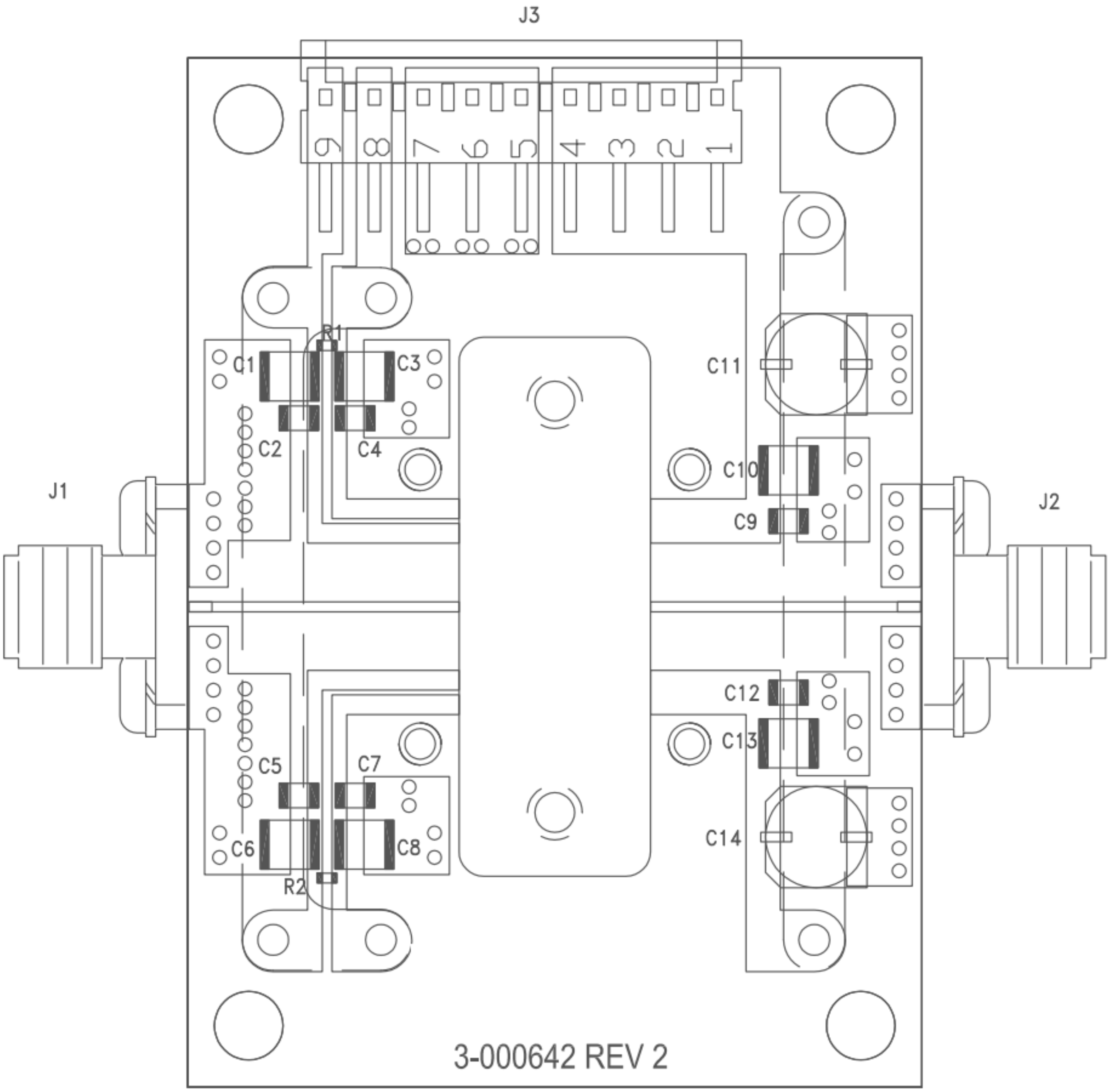
Evaluation Board Schematic (CMPA601C025F-AMP)



Parts List

Part	Value	Qty.
C2, C4, C5, C7, C9, C12	CAP, 33000 pF, 0805, 100V, X7R	6
C1, C3, C6, C8, C10, C13	CAP, 1 µF, 100V, 10%, X7R, 1210	6
C11, C14	CAP ELECT 3.3 µF 80V FK SMD	2
R1, R2	RES 0.0 OHM 1/16W 0402 SMD	2
J1, J2	CONN, SMA, PANEL MOUNT JACK, FLANGE, 4-HOLE, BLUNT POST, 20MIL	2
J3	HEADER RT>PLZ .1CEN LK 9POS	1
W1	WIRE, BLACK, 22 AWG ~ 1.50”	1
W2	WIRE, BLACK, 22 AWG ~ 1.75”	1
Q1	CMPA601C025F	1

Evaluation Board Assembly Drawing (CMPA601C025F-AMP)



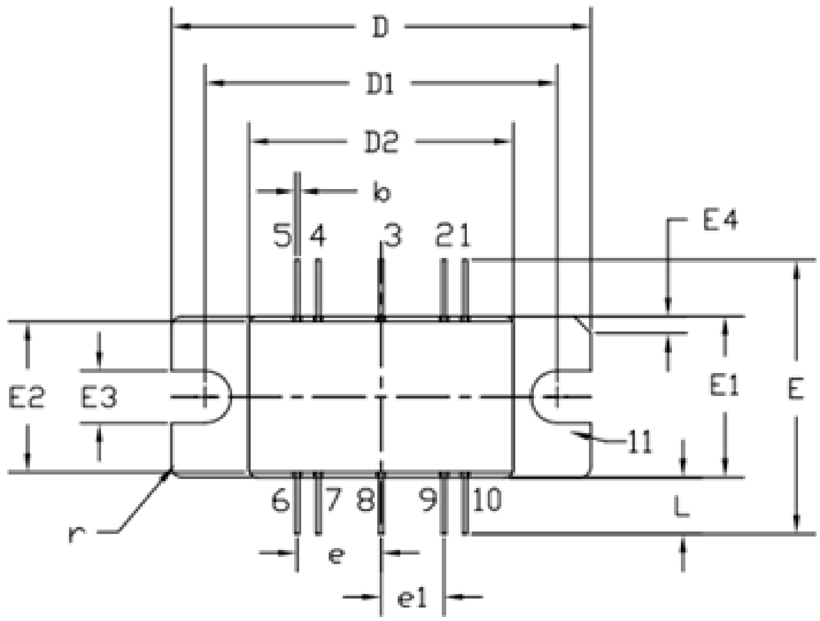
Bias On Sequence

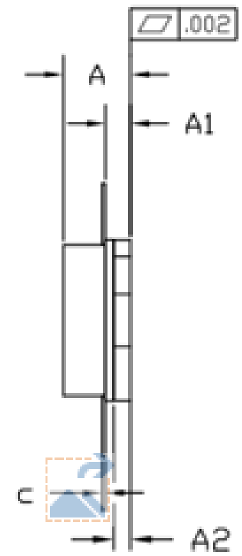
1. Ensure RF is turned-off
2. Apply pinch-off voltage of -5 V to the gate (V_G)
3. Apply nominal drain voltage (V_D)
4. Adjust Vg to obtain desired quiescent drain current (I_{DQ})
5. Apply RF

Bias Off Sequence

1. Turn RF off
2. Apply pinch-off to the gate (V_G = -5 V)
3. Turn off drain voltage (V_D)
4. Turn off gate voltage (V_G)

Mechanical Information





NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M - 1994.

2. CONTROLLING DIMENSION: INCH.

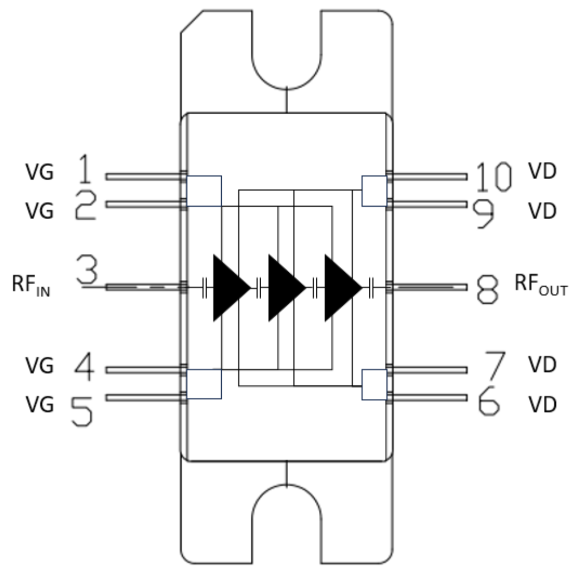
3. ADHESIVE FROM LID MAY EXTEND A MAXIMUM OF 0.020" BEYOND EDGE OF LID.

4. LID MAY BE MISALIGNED TO THE BODY OF PACKAGE BY A MAXIMUM OF 0.008" IN ANY DIRECTION.

	INCHES		MILLIMETERS		NOTES
DIM	MIN	MAX	MIN	MAX	
A	0.155	0.175	3.94	4.45	
A1	0.055	0.065	1.40	1.65	
A2	0.035	0.045	0.89	1.14	
b	0.01 TYP		0.254 TYP		10x
c	0.007	0.009	0.18	0.23	
D	0.995	1.005	25.27	25.53	
D1	0.835	0.845	21.21	21.46	
D2	0.623	0.637	15.82	16.18	
E	0.653 TYP		16.59 TYP		
E1	0.380	0.390	9.65	9.91	
E2	0.355	0.365	9.02	9.27	
E3	0.120	0.130	3.05	3.30	
E4	0.035	0.045	0.89	1.14	45° CHAMFER
e	0.200 TYP		5.08 TYP		4x
e1	0.150 TYP		3.81 TYP		4x
L	0.115	0.155	2.92	3.94	10x
r	0.025 TYP		.635 TYP		3x

Pin Description

Pin #	Name	Description
1, 2	VG	Pins 1 and 2 are same VG node and must be electrically connected to the gate bias voltage.
3	RF_{IN}	RF Input. 50-ohm matched. Internally DC blocked.
4, 5	VG	Pins 4 and 5 are same VG node and must be electrically connected to the gate bias voltage.
6, 7	VD	Pins 6 and 7 are same VD node and must be electrically connected to the drain bias voltage.
8	RF_{OUT}	RF Output. 50-ohm matched. Internally DC blocked.
9, 10	VD	Pins 9 and 10 are same VD node and must be electrically connected to the drain bias voltage.
Base	GND	RF and DC ground.



Revision History

Rev	Date	Change Description
V1	12/11/2024	Production release.