CMPA5585030F

30 W, 5.5 - 8.5 GHz, GaN MMIC, Power Amplifier

Package Type: 440213
PN: CMPA5585030F

Description

The CMPA5585030F is a gallium nitride (GaN) High Electron Mobility Transistor (HEMT) based monolithic microwave integrated circuit (MMIC). GaN has superior properties compared to silicon or gallium arsenide, including higher breakdown voltage, higher saturated electron drift velocity and higher thermal conductivity. GaN HEMTs also offer greater power density and wider bandwidths compared to Si and GaAs transistors. This MMIC is available in a 10 lead metal/ceramic flanged package for optimal electrical and thermal performance.

Typical Performance Over 5.8 - 8.4 GHz (T_C = 25°C)

Parameter	5.8 GHz	6.4 GHz	7.2 GHz	7.9 GHz	8.4 GHz	Units
S21[1,2]	25.9	23.8	26.5	24.5	26.7	dB
Power Gain[2,5]	22.3	19.0	20.9	21.6	21.2	dB
PAE[1,2,4,5]	24.7	20.7	20.3	22.6	22.9	%
ACLR[1,2,3,5]	-37	-42	-33	-34	-40	dBc

Notes (unless otherwise specified):
[1] At 25°C
[2] Measurements are performed using the test fixture AD-938516
[3] Under OQPSK modulated signal, 1.6 Msps, PN23, Alpha Filter = 0.2
[4] Power Added Efficiency = (P_{OUT} - P_{IN}) / PDC
[5] Measured at P_{OUT} = 41 dBm

Features

- 25 dB Small Signal Gain
- 30 W Typical P_{SAT}
- Operation up to 28 V
- High Breakdown Voltage
- High Temperature Operation
- Size 1.00 x 0.385 inches

Applications

- Point to Point Radio
- Communications Radar
- Satellite Communication Uplink

RoHS compliant

Absolute Maximum Ratings (not simultaneous)

Parameter	Symbol	Rating	Units	Conditions
Drain-source Voltage	V_{DSS}	150	V_{DC}	25˚C
Gate-source Voltage	V_{GS}	-10, +2		
Storage Temperature	T_{STG}	-65, +150	°C	
Operating Junction Temperature	T_J	225		
Maximum Forward Gate Current	I_{GMAX}	10	mA	25°C
Soldering Temperature[1]	T_S	245	°C	
Screw Torque	τ	40	in-oz	
CGHV40180F Thermal Resistance, Junction to Case	$R_{θJC}$	2.16	°C/W	CW, 85°C, P_{DISS} = 66 W
Case Operating Temperature	T_C	-40, +150	°C	

Note:
[1] Refer to the Application Note on soldering

Electrical Characteristics (Frequency = 5.5 GHz to 8.5 GHz unless otherwise stated; T_C = 25°C)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Conditions
DC Characteristics[1]						
Gate Threshold Voltage	$V_{GS(th)}$	-3.8	-2.8	-2.3	V	V_{DS} = 10 V, I_{DS} = 12.7 mA
Saturated Drain Current[2]	I_{DS}	9.2	12.7	–	A	V_{DS} = 6.0 V, V_{GS} = 2.0 V
Drain-Source Breakdown Voltage	V_{BD}	84	–	–	V	V_{GS} = -8 V, I_{DS} = 12.7 mA
RF Characteristics[3]						
Small Signal Gain	S21	22.85	26	–	dB	V_{DD} = 28 V, I_{DQ} = 285 mA, P_{IN} = -20 dBm
Input Return Loss	S11	–	-7	–		
Output Return Loss	S22	–		–		
Output Mismatch Stress	VSWR	–	–	5:1	Ψ	No damage at all phase angles, V_{DD} = 28 V, I_{DQ} = 285 mA, P_{OUT} = 43 dBm

Notes:
[1] Measured on-wafer prior to packaging
[2] Scaled from PCM data
[3] Measured using network analyzer (Power = -20 dBm)

Electrical Characteristics Continued (T_C = 25°C)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Conditions
RF Characteristics[1,2,4,6]						
Power Added Efficiency at 5.8 GHz[5]	PAE_1	19.0	25.8	–	%	V_{DD} = 28 V, I_{DQ} = 285 mA, P_{IN} = 41 dBm
Power Added Efficiency at 6.4 GHz[5]	PAE_2	16.0	22.4	–		
Power Added Efficiency at 7.2 GHz[5]	PAE_3	16.2	22.0	–		
Power Added Efficiency at 7.9 GHz[5]	PAE_4	18.0	23.9	–		
Power Added Efficiency at 8.4 GHz[5]	PAE_5	19.2	25.0	–		
Power Gain at 5.8 GHz	G_{P1}	18.25	22.4	–	dB	
Power Gain at 6.4 GHz	G_{P2}	16.35	20.2	–		
Power Gain at 7.2 GHz	G_{P3}	16.85	21.0	–		
Power Gain at 7.9 GHz	G_{P4}	17.15	22.2	–		
Power Gain at 8.4 GHz	G_{P5}	17.65	21.8	–		
OQPSK Linearity at 5.8 GHz	$ACLR_1$	–	-42	-32	dBc	
OQPSK Linearity at 6.4 GHz	$ACLR_2$	–	-44	-33		
OQPSK Linearity at 7.2 GHz	$ACLR_3$	–	-34	-27.5		
OQPSK Linearity at 7.9 GHz	$ACLR_4$	–	-37	-28		
OQPSK Linearity at 8.4 GHz	$ACLR_5$	–	-40	-32		

Notes:
1 At 25°C
2 Measurements are to be performed using the CMPA5585030F-AMP
3 Measured using network analyzer (Power = -20 dBm)
4 Under OQPSK modulated signal, 1.6 Msps, PN23, Alpha Filer = 0.2
5 Power Added Efficiency = (P_{OUT} - P_{IN})/PDC
6 Fixture loss de-embedded using the following offset. The offset is subtracted from the input offset value and added to the output offset value.
a. 5.8 GHz - 0.182 dB
b. 6.4 GHz - 0.200 dB
c. 7.2 GHz - 0.217 dB
d. 7.9 GHz - 0.234 dB
e. 8.4 GHz - 0.246 dB

Electrostatic Discharge (ESD) Classifications

Parameter	Symbol	Class	Classification Level	Test Methodology
Human Body Model	HBM	2	ANSI/ESDA/JEDEC JS-001 Table 3	JEDEC JESD22 A114-D
Charge Device Model	CDM	C3	ANSI/ESDA/JEDEC JS-002 Table 3	JEDEC JESD22 C101-C

Typical Performance of the CMPA5585030F

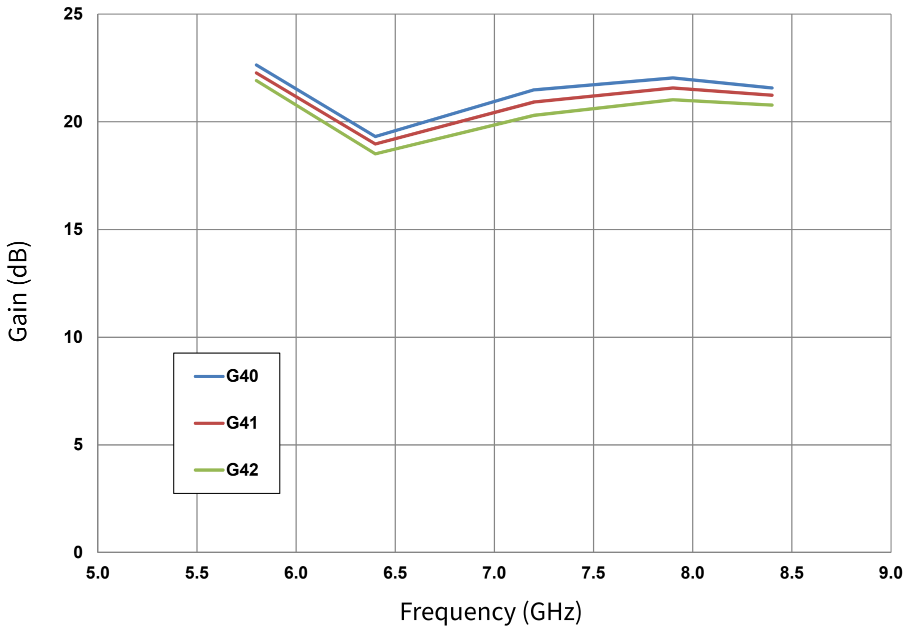


Figure 1. Gain vs. Frequency & Output Power OQPSK 1.6 Msps
V_{DD} = 28 V, I_{DQ} = 285 mA

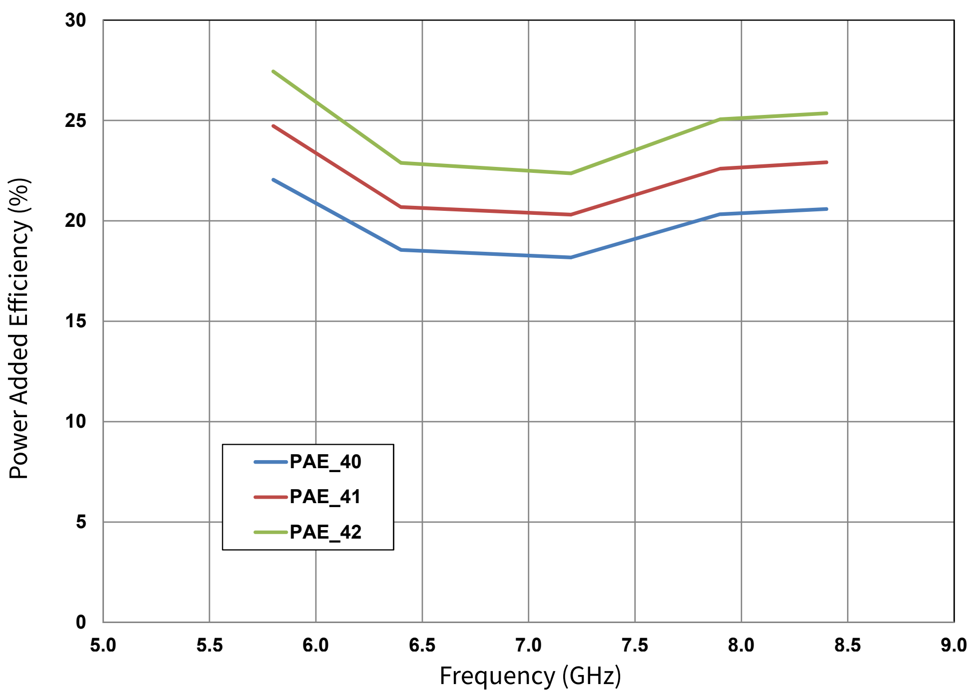


Figure 2. Power Added Efficiency vs. Frequency & Output Power OQPSK
1.6 Msps V_{DD} = 28 V, I_{DQ} = 285 mA

Typical Performance of the CMPA5585030F

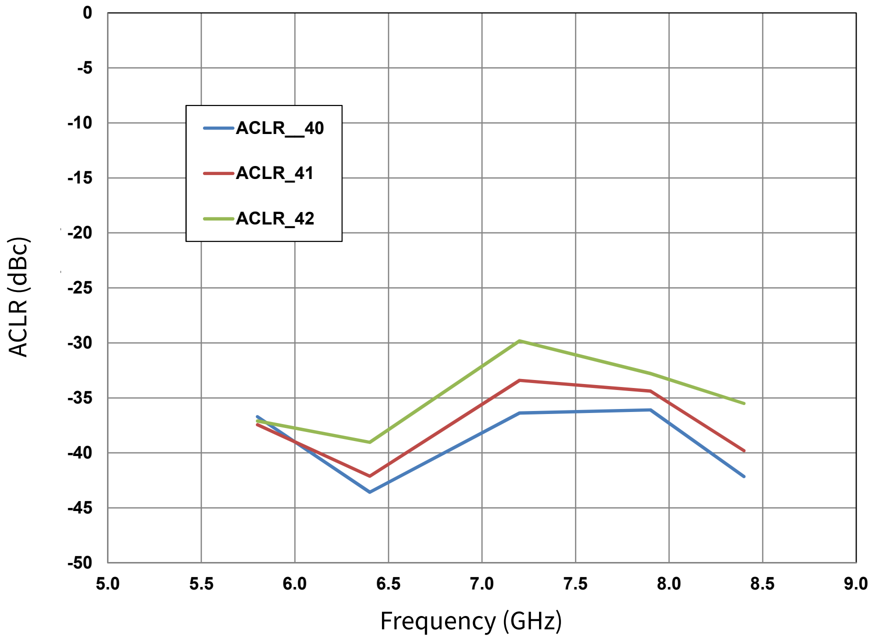


Figure 3. ACLR vs. Frequency & Output Power OQPSK 1.6 Msps
V_{DD} = 28 V, I_{DQ} = 285 mA

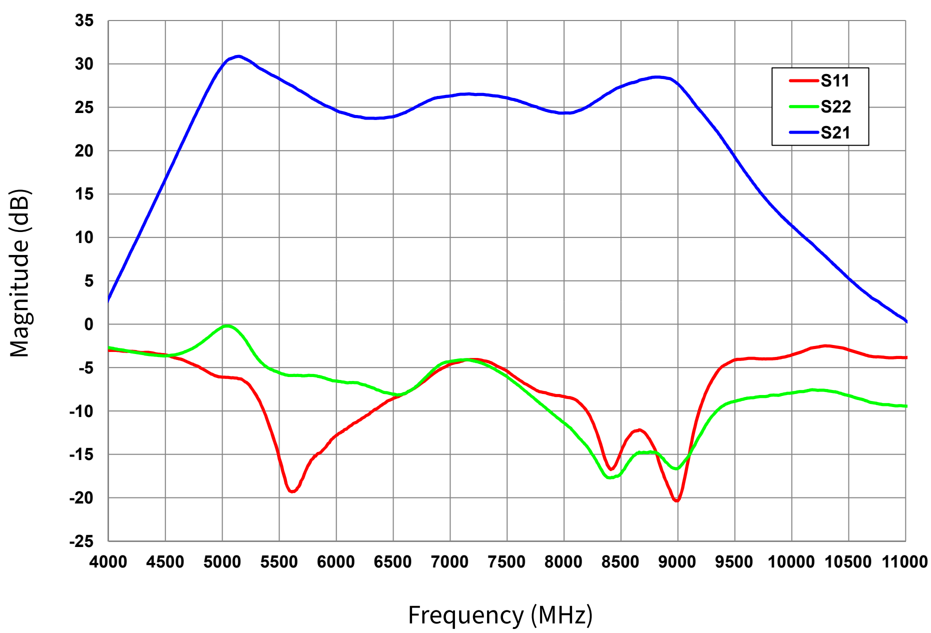


Figure 4. Typical S-Parameters
V_{DD} = 28 V, I_{DQ} = 285 mA

Typical Performance of the CMPA5585030F

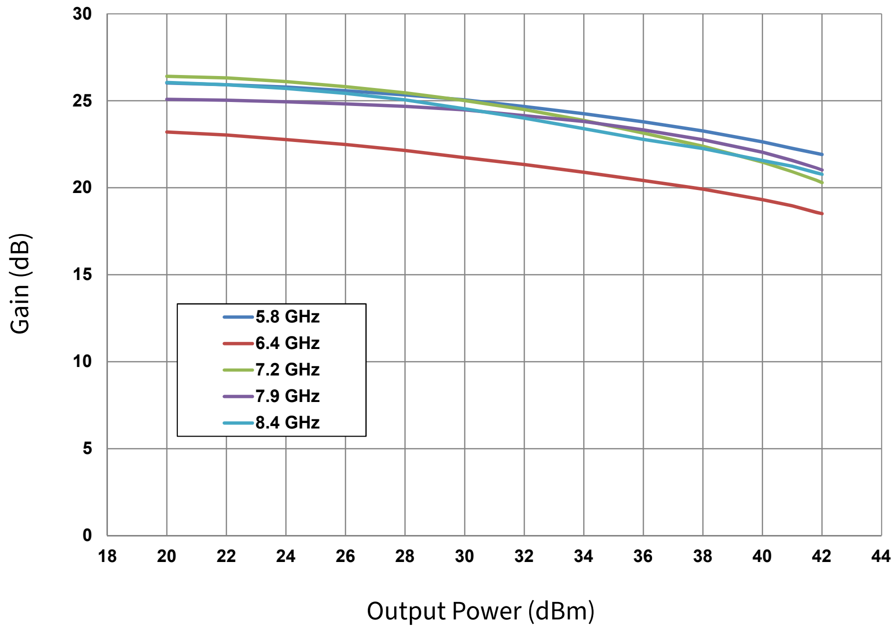


Figure 5. Gain vs. Output Power and Frequency OQPSK 1.6 Msps
V_{DD} = 28 V, I_{DQ} = 285 mA

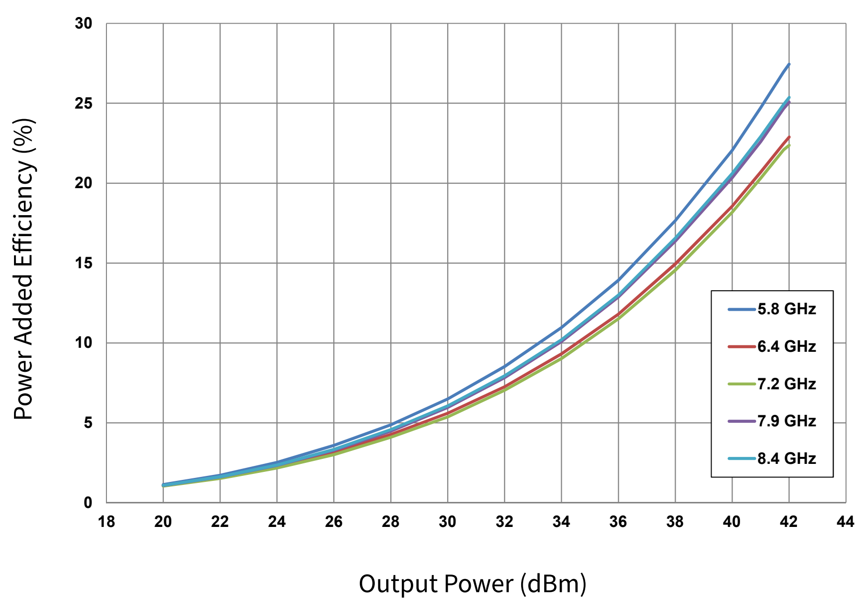


Figure 6. Power Added Efficiency vs. Output Power and Frequency OQPSK
1.6 Msps V_{DD} = 28 V, I_{DQ} = 285 mA

Typical Performance of the CMPA5585030F

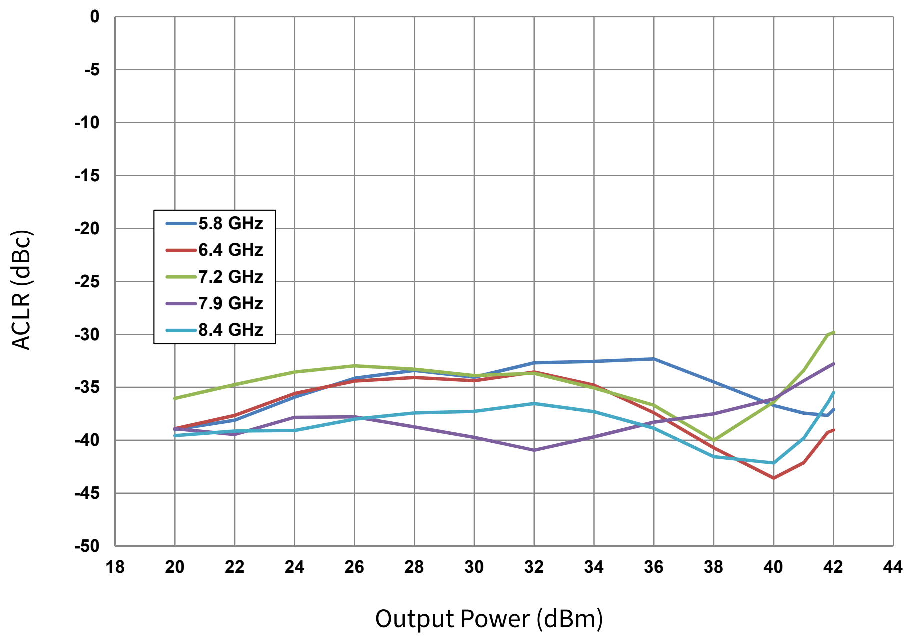


Figure 7. ACLR vs. Output Power and Frequency OQPSK 1.6 Msps
V_{DD} = 28 V, I_{DQ} = 285 mA

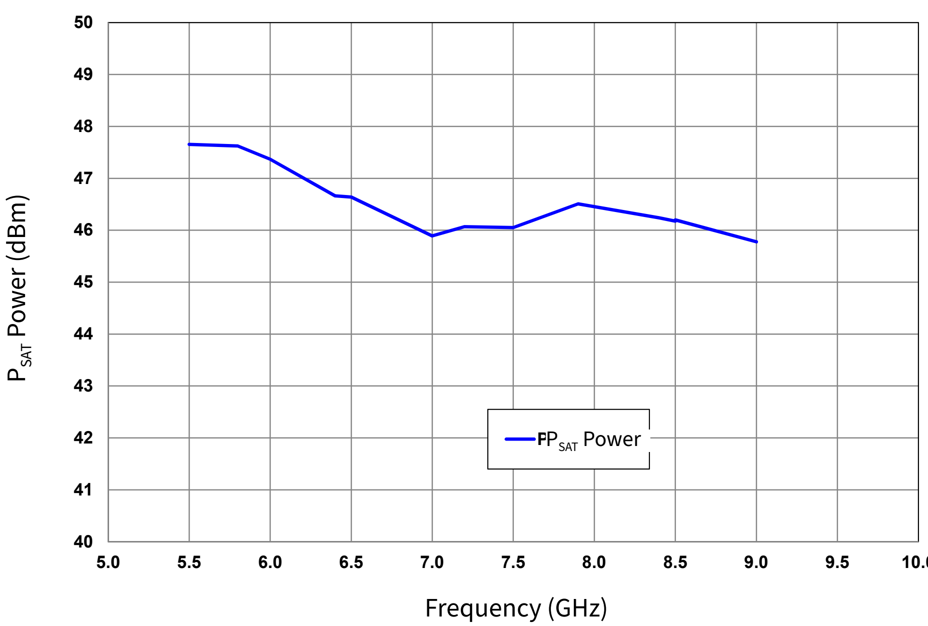


Figure 8. P_{SAT} Power vs. Frequency
V_{DD} = 28 V, I_{DQ} = 800 mA, Pulsed Width = 100µs, Duty Cycle = 10%

Typical Performance of the CMPA5585030F

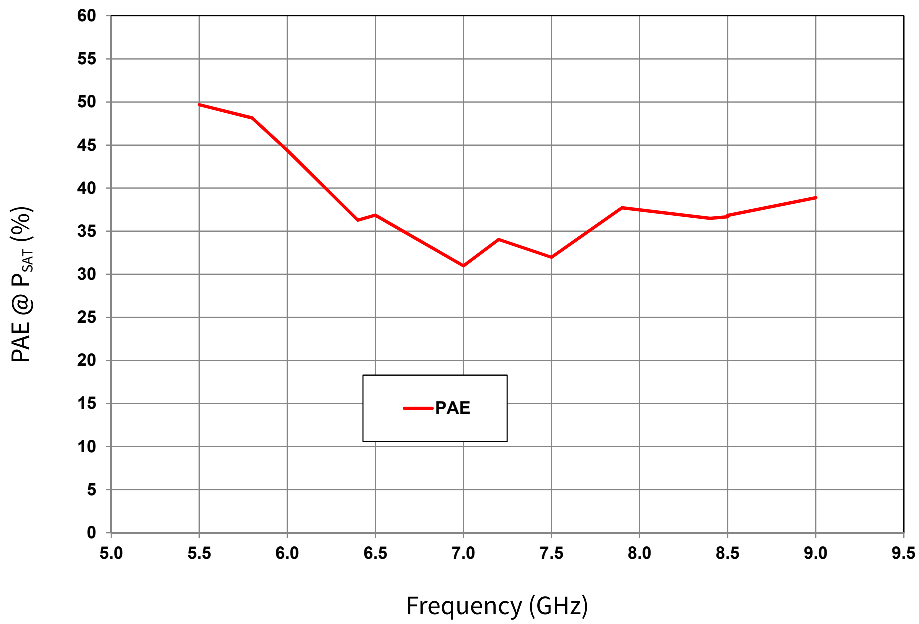


Figure 9. Power Added Efficiency @ Saturated Power vs. Frequency
V_{DD} = 28 V, I_{DQ} = 800 mA, Pulsed Width = 100µs, Duty Cycle = 10%

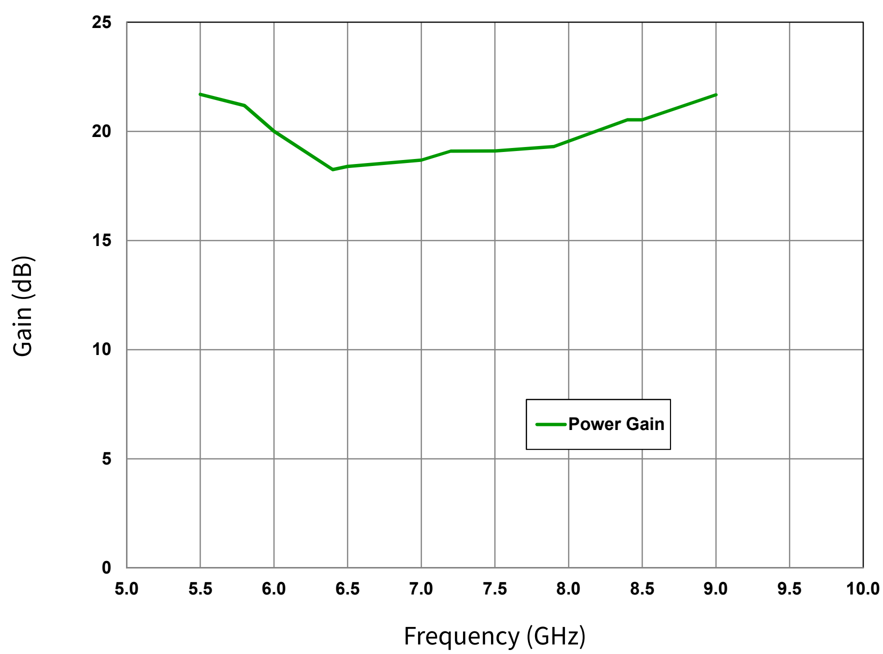


Figure 10. Gain @ Saturated Power vs. Frequency
V_{DD} = 28 V, I_{DQ} = 800 mA, Pulsed Width = 100µs, Duty Cycle = 10%

Typical Performance of the CMPA5585030F

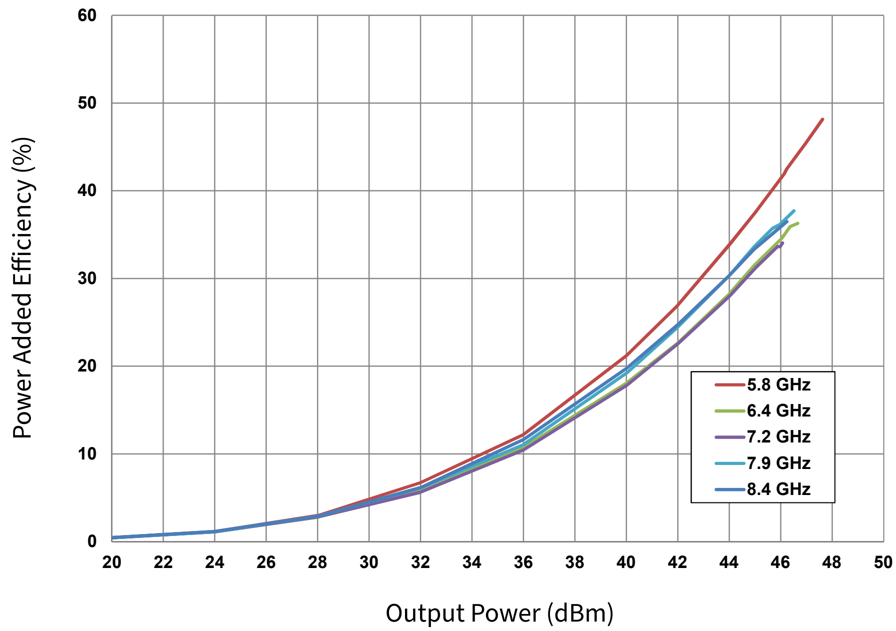


Figure 11. PAE vs. Output Power and Frequency
V_{DD} = 28 V, I_{DQ} = 800 mA, Pulsed Width = 100µs, Duty Cycle = 10%

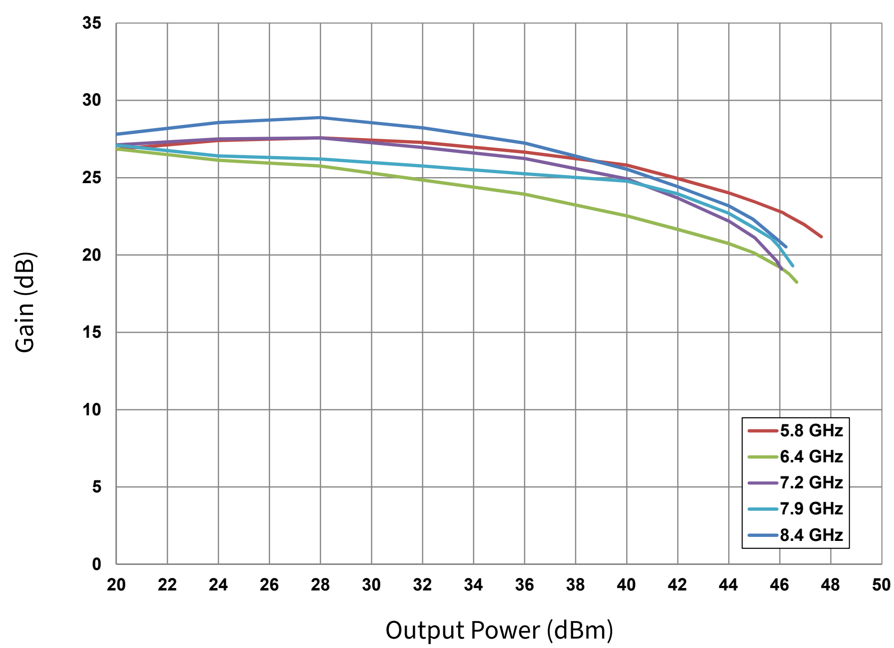
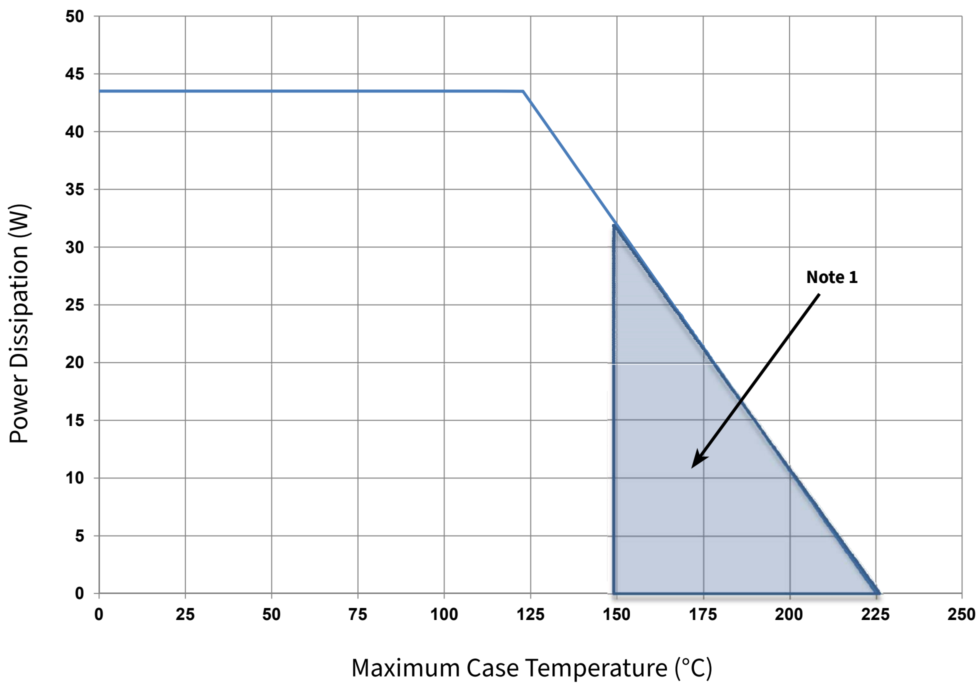


Figure 12. Gain vs. Output Power and Frequency
V_{DD} = 28 V, I_{DQ} = 800 mA, Pulsed Width = 100µs, Duty Cycle = 10%

CMPA5585030F Power Dissipation De-rating Curve

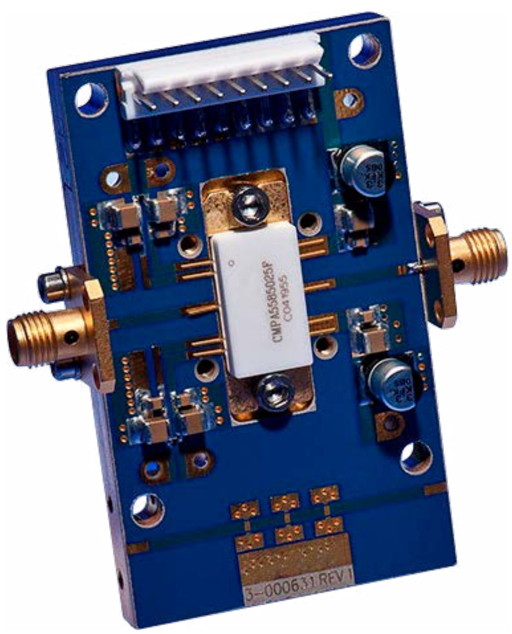


Note:
[1] Area exceeds Maximum Case Operating Temperature (See Page 2)

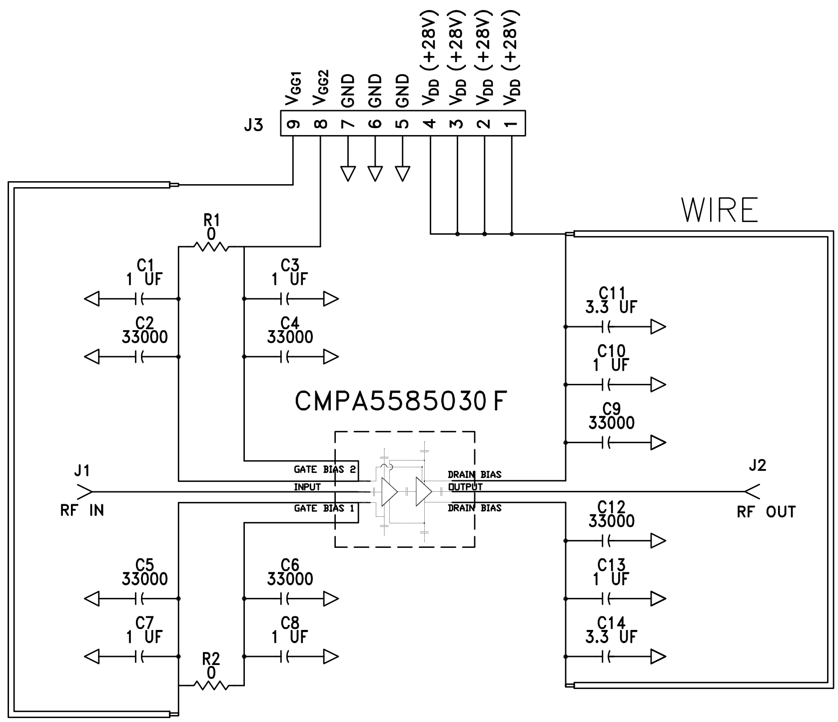
CMPA5585030F-AMP Application Circuit Bill of Materials

Designator	Description	Qty
C1, C3, C7, C8, C10, C13	CAP, 1.0µF, +/-10%, 1210, 100V, X7R	6
C2, C4, C5, C6, C9, C12	CAP, 33000pF, 0805, 100V, X7R	6
C11, C14	CAP ELECT 3.3µF 80V FK SMD	2
R1, R2	RES 0.0 OHM 1/16W 0402 SMD	2
J1,J2	CONN, SMA, PANEL MOUNT JACK, FLANGE, 4-HOLE, BLUNT POST, 20MIL	2
J3	CONNECTOR, HEADER, RT>PLZ .1CEN LK 9POS	1
	PCB, TACONIC, RF-35P-0200-CL1/CL1	1
Q1	CMPA5585030F	1

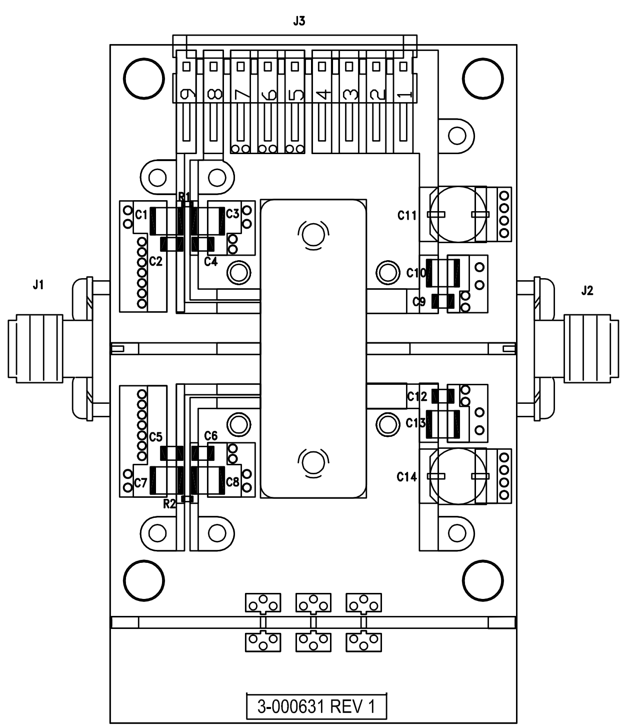
CMPA5585030F-AMP Demonstration Amplifier Circuit



CMPA5585030F-AMP Demonstration Amplifier Circuit

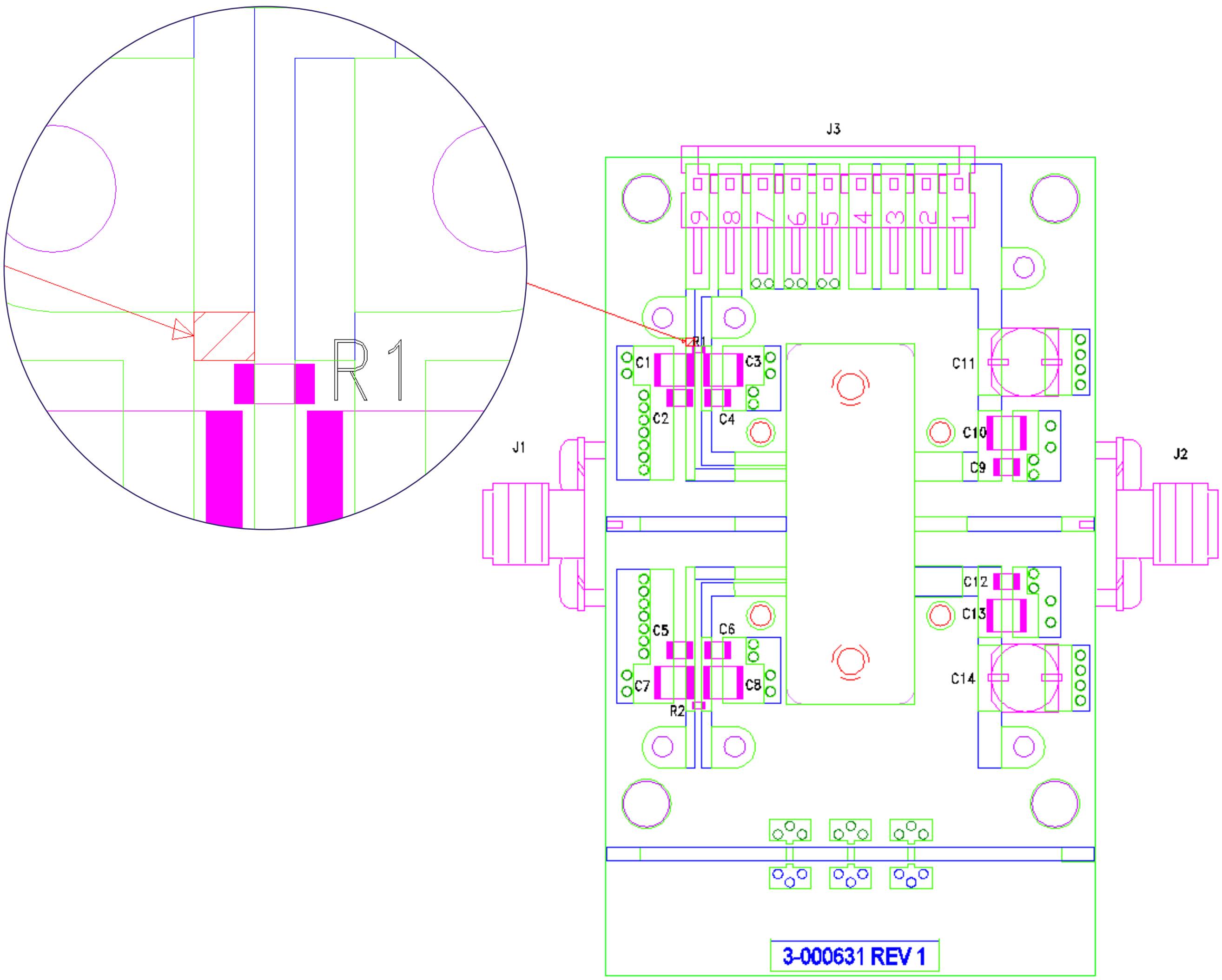


CMPA5585030F-AMP Demonstration Amplifier Circuit Outline

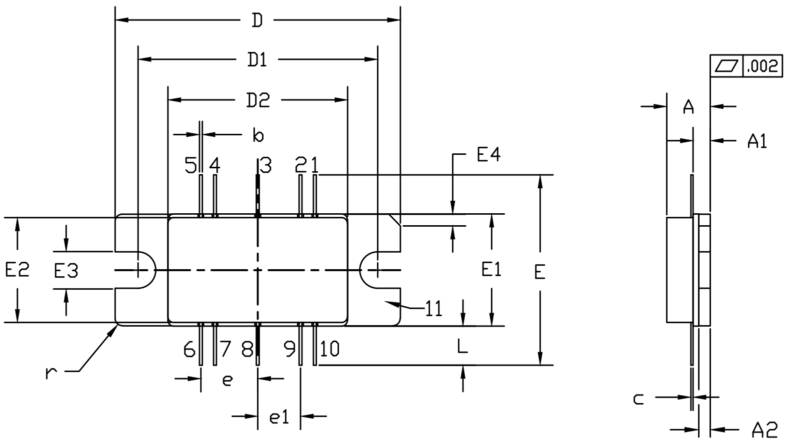


CMPA5585030F-AMP Demonstration Amplifier Circuit

To configure the CMPA5585030F test fixture to enable independent VG1 / VG2 control of the device, a cut must be made to the microstrip line just above the R1 resistor as shown. Pin 9 will then supply VG1 and Pin 8 will supply VG2.



Product Dimensions CMPA5585030F (Package Type — 440213)



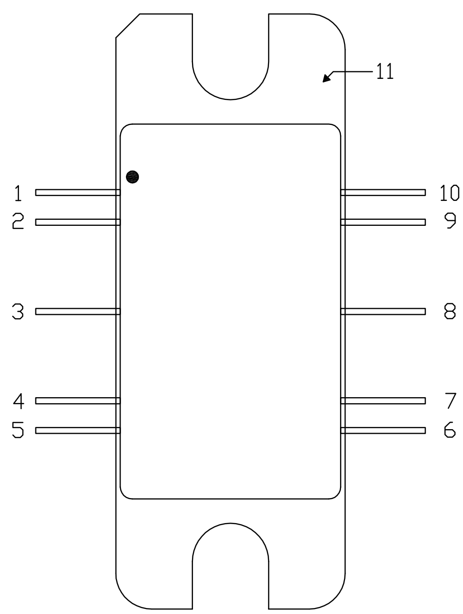
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M – 1994.
2. CONTROLLING DIMENSION: INCH.
3. ADHESIVE FROM LID MAY EXTEND A MAXIMUM OF 0.020" BEYOND EDGE OF LID.
4. LID MAY BE MISALIGNED TO THE BODY OF PACKAGE BY A MAXIMUM OF 0.008" IN ANY DIRECTION.

DIM	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.148	0.168	3.76	4.27	
A1	0.055	0.065	1.40	1.65	
A2	0.035	0.045	0.89	1.14	
b	0.01 TYP		0.254 TYP		10x
c	0.007	0.009	0.18	0.23	
D	0.995	1.005	25.27	25.53	
D1	0.835	0.845	21.21	21.46	
D2	0.623	0.637	15.82	16.18	
E	0.653 TYP		16.59 TYP		
E1	0.380	0.390	9.65	9.91	
E2	0.355	0.365	9.02	9.27	
E3	0.120	0.130	3.05	3.30	
E4	0.035	0.045	0.89	1.14	45° CHAMFER
e	0.200 TYP		5.08 TYP		4x
e1	0.150 TYP		3.81 TYP		4x
L	0.115	0.155	2.92	3.94	10x
r	0.025 TYP		.635 TYP		3x

PIN 1: GATE BIAS
2: GATE BIAS
3: RF IN
4: GATE BIAS
5: GATE BIAS
6: DRAIN BIAS
7: DRAIN BIAS
8: RF OUT
9: DRAIN BIAS
10: DRAIN BIAS
11: SOURCE

PIN	Qty
1	Gate Bias for Stage 2
2	Gate Bias for Stage 2
3	RF In
4	Gate Bias for Stage 1
5	Gate Bias for Stage 1
6	Drain Bias
7	Drain Bias
8	RF Out
9	Drain Bias
10	Drain Bias
11	Source



Part Number System

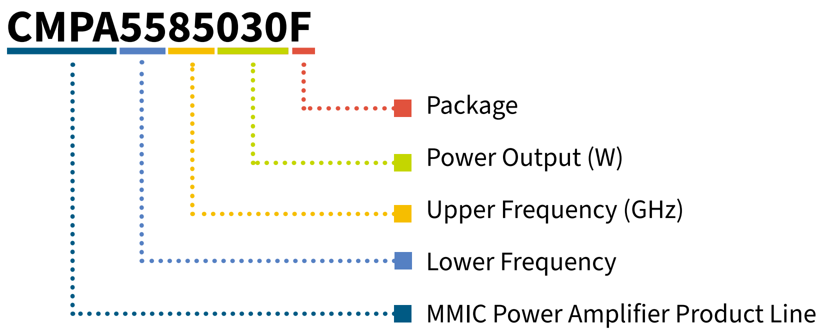


Table 1.

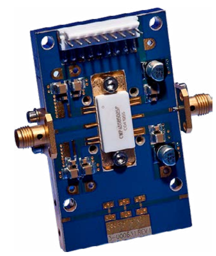
Parameter	Value	Units
Lower Frequency	5.5	GHz
Upper Frequency[1]	8.5	
Power Output	30	W
Package	Flange	–

Note:
[1] Alpha characters used in frequency code indicate a value greater than 9.9 GHz. See Table 2 for value.

Table 2.

Character Code	Code Value
A	0
B	1
C	2
D	3
E	4
F	5
G	6
H	7
J	8
K	9
Examples	1A = 10.0 GHz 2H = 27.0 GHz

Product Ordering Information

Order Number	Description	Unit of Measure	Image
CMPA5585030F	GaN MMIC	Each	
CMPA5585030F-AMP	Test board with GaN MMIC installed	Each	

Notes & Disclaimer