# CMPA1842040D

## 1.8 – 4.2 GHz, 45 W GaN HPA

## Description

The CMPA1842040D is a 45W MMIC HPA utilizing the high performance, 0.15um GaN on SiC production process. The CMPA1842040D operates from 1.8-4.2 GHz and supports electronic warfare applications. The CMPA1842040D achieves 45 W of saturated output power with 25 dB of large signal gain and typically 45% power-added efficiency under CW operation.

The CMPA1842040D provides improved RF performance over a more targeted narrow bandwidth allowing customers to improve SWaP-C benchmarks in their next-generation systems.

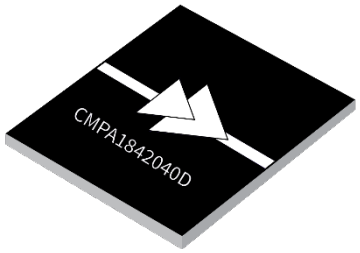



**Figure 1. CMPA1842040D**

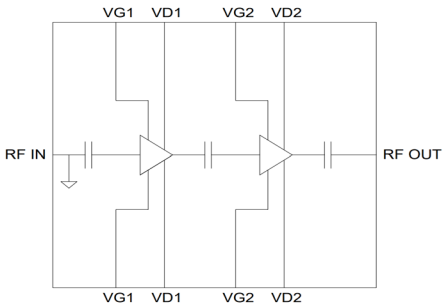



**Figure 2. Functional Block Diagram**

### Features

- Psat: 45 W
- PAE: 45 %
- LSG: 25 dB
- S21: 29 dB
- S11: -11 dB
- S22: -9 dB
- CW operation

Note: Features are typical performance across frequency under 25C operation. Please reference performance charts for additional information.

### Applications

- Electronic Warfare

RoHS compliant

## Absolute Maximum Ratings

| Parameter | Symbol | Units | Value | Conditions |
|---|---|---|---|---|
| Drain to Source Voltage | $V_{DSS}$ | V | 84 | |
| Drain Voltage | $V_D$ | V | 28 | |
| Gate Voltage | $V_G$ | V | -10, +2 | |
| Drain Current | $I_D$ | A | 4.8 | |
| Gate Current | $I_G$ | mA | 12.5 | |
| Input Power | $P_{in}$ | dBm | 23 | |
| Dissipated Power | $P_{diss}$ | W | 84 | 85°C |
| Storage Temperature | $T_{stg}$ | °C | -55, +150 | |
| Mounting Temperature | $T_J$ | °C | 320 | 30 seconds |
| Junction Temperature | $T_J$ | °C | 225 | MTTF>=1e6 Hours |
| Output Mismatch Stress | VSWR | Ψ | 5:1 | |

## Recommended Operating Conditions

| Parameter | Symbol | Units | Typical Value | Conditions |
|---|---|---|---|---|
| Drain Voltage | Vd | V | 28 | |
| Gate Voltage | Vg | V | -2.2 | |
| Drain Current | Idq | mA | 550 | |
| Input Power | Pin | dBm | 21 | CW |
| Case Temperature | Tcase | °C | -40 to 85 | |

## RF Specifications

Test conditions unless otherwise noted: Vd=28 V, Idq=550 mA, CW, Pin = 21 dBm, $T_{base}$=25 °C, Frequency: 3GHz

| Parameter | Units | Frequency | Min | Typical | Max | Conditions |
|---|---|---|---|---|---|---|
| Frequency | GHz | | 1.8 | | 4.2 | |
| Output Power | dBm | 1.8 | | 46 | | |
| | | 3.0 | | 46.5 | | |
| | | 4.2 | | 46.5 | | |
| Power-added Efficiency | % | 1.8 | | 58 | | |
| | | 3.0 | | 49 | | |
| | | 4.2 | | 42 | | |
| LSG | dB | 1.8 | | 25 | | |
| | | 3.0 | | 25.5 | | |
| | | 4.2 | | 25.5 | | |
| Small-Signal Gain (S21) | dB | 1.8 | | 28 | | Pin = -20 dBm |
| | | 3.0 | | 29 | | |
| | | 4.2 | | 29 | | |
| Input Return Loss | dB | | | -11 | | Pin = -20 dBm |
| Output Return Loss | dB | | | -9 | | Pin = -20 dBm |

Test conditions unless otherwise noted: Vd=28 V, Idq=550 mA, CW, Pin = 21 dBm, $T_{base}$=25 °C, Frequency: 3GHz

**Figure 3: Pout v. Frequency v. Temperature**

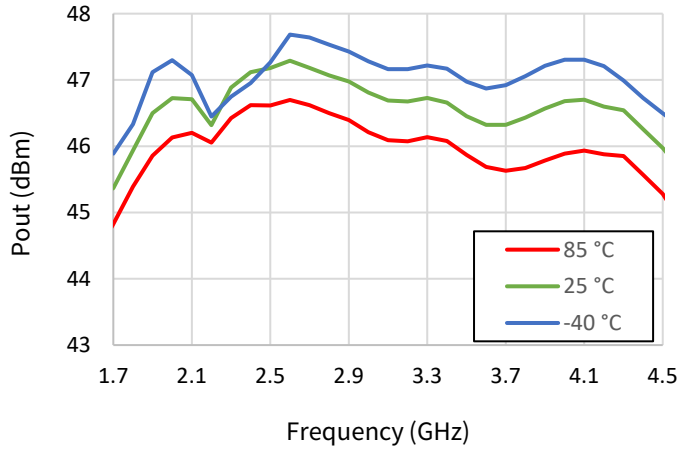



**Figure 4: PAE v. Frequency v. Temperature**

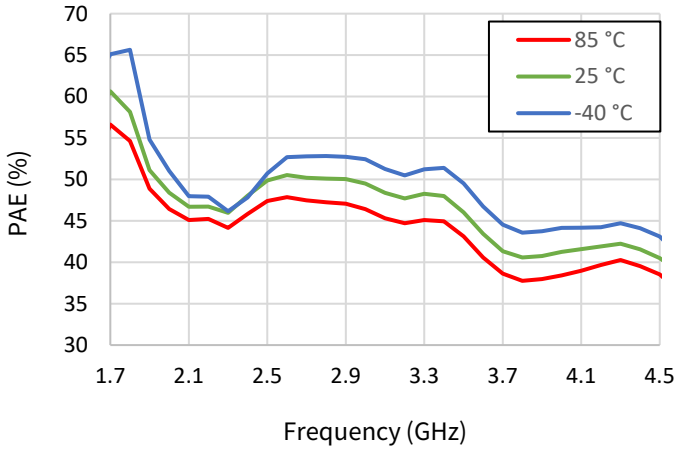



**Figure 5: Id v. Frequency v. Temperature**

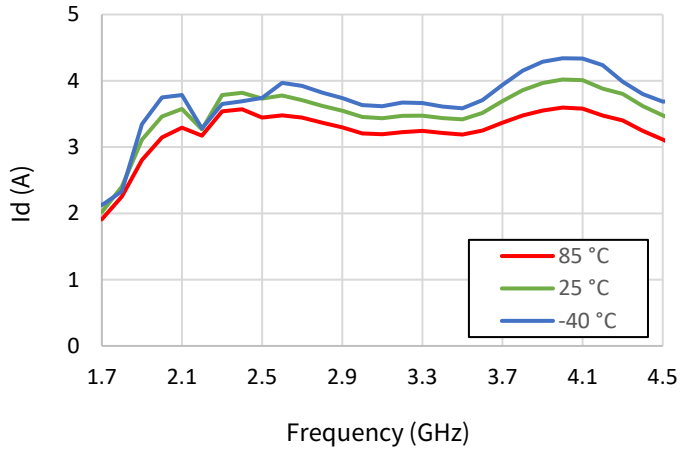



**Figure 6: Ig v. Frequency v. Temperature**

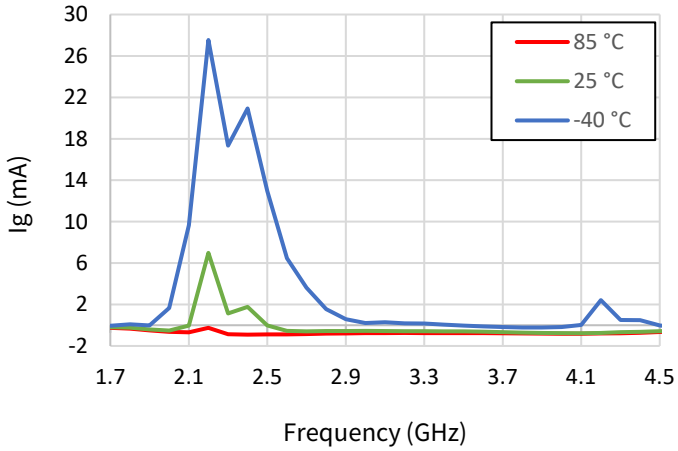
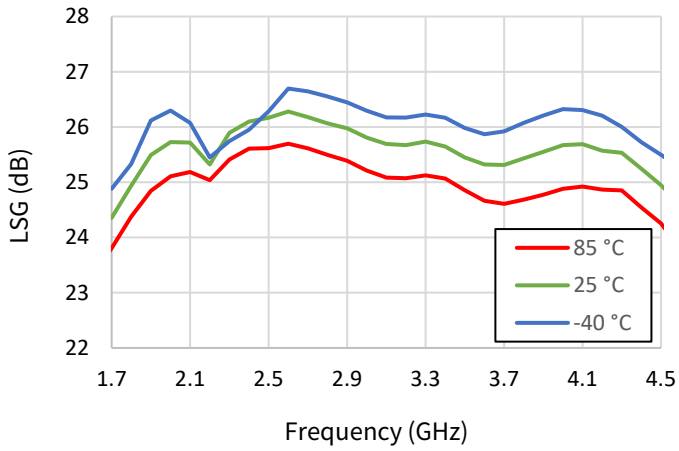



**Figure 7: LSG v. Frequency v. Temperature**



Test conditions unless otherwise noted: Vd=28 V, Idq=550 mA, CW, Pin = 21 dBm, $T_{base}$=25 °C, Frequency: 3GHz

**Figure 8: Pout v. Frequency v. Vd**

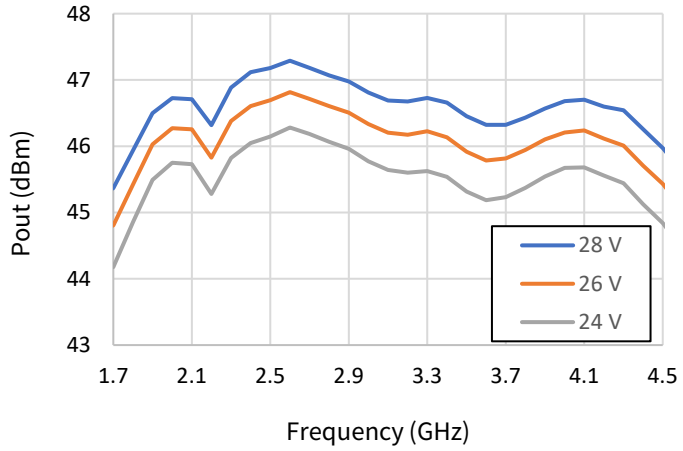



**Figure 9: PAE v. Frequency v. Vd**

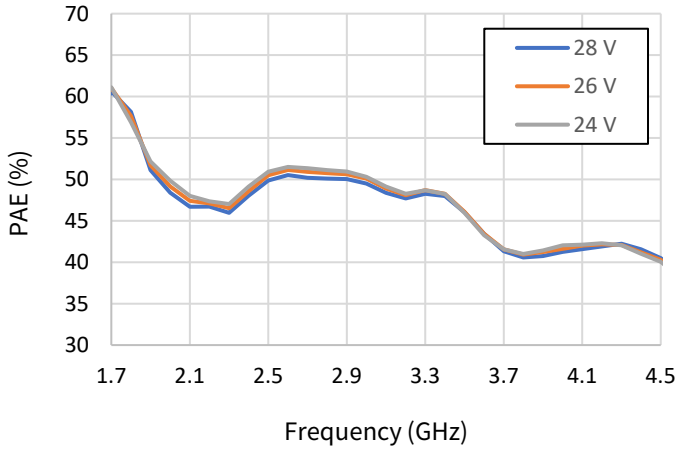



**Figure 10: Id v. Frequency v. Vd**

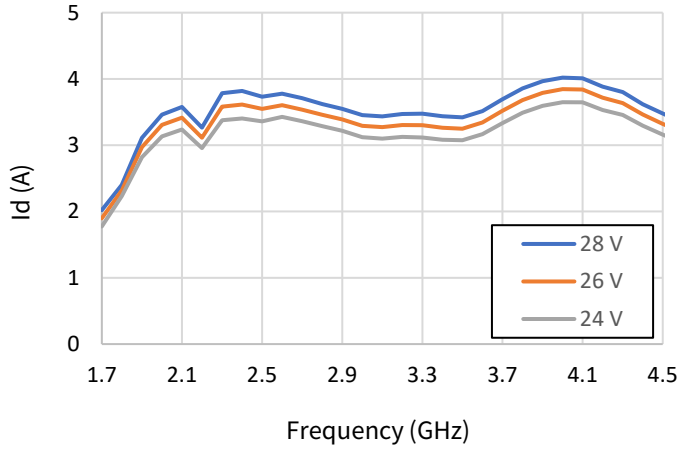



**Figure 11: Ig v. Frequency v. Vd**

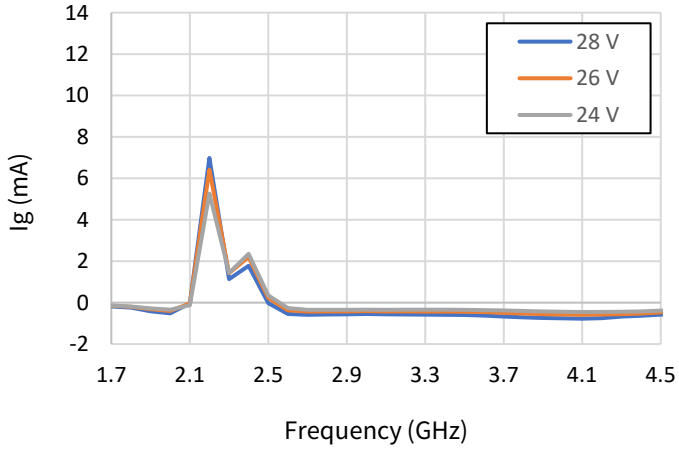
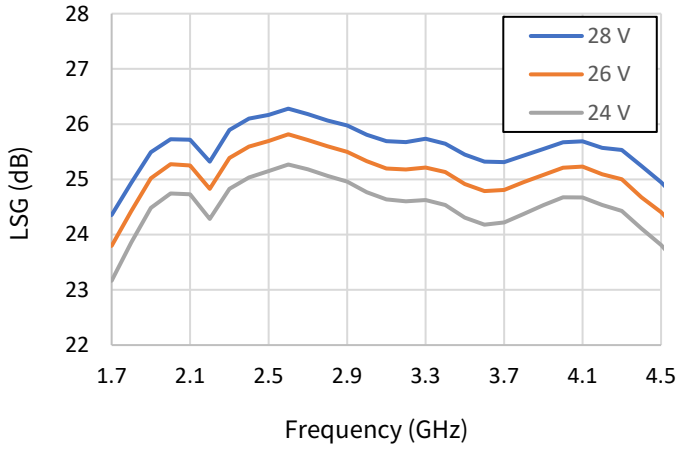



**Figure 12: LSG v. Frequency v. Vd**



Test conditions unless otherwise noted: Vd=28 V, Idq=550 mA, CW, Pin = 21 dBm, $T_{base}$=25 °C, Frequency: 3GHz

**Figure 13: Pout v. Frequency v. Idq**

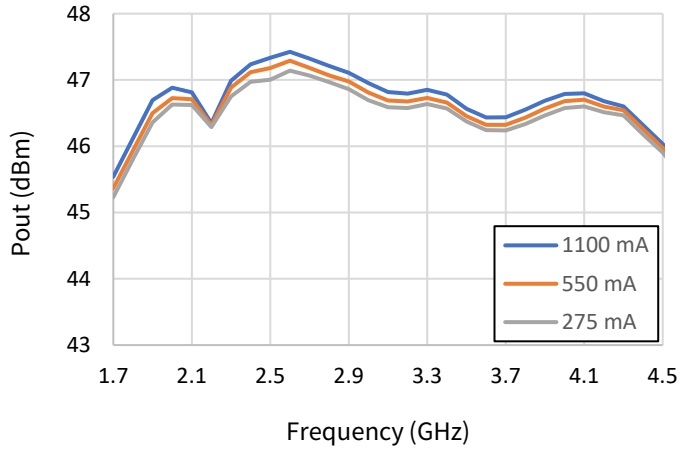



**Figure 14: PAE v. Frequency v. Idq**

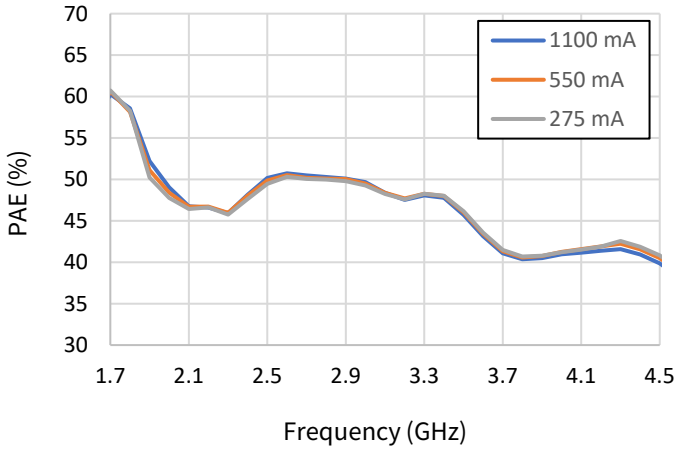



**Figure 15: Id v. Frequency v. Idq**

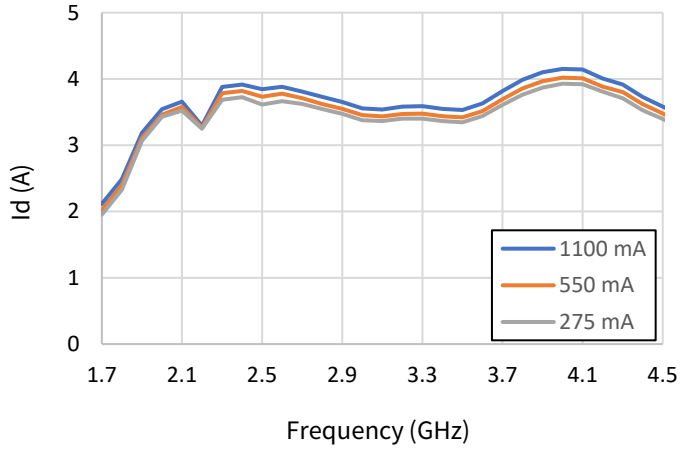



**Figure 16: Ig v. Frequency v. Idq**

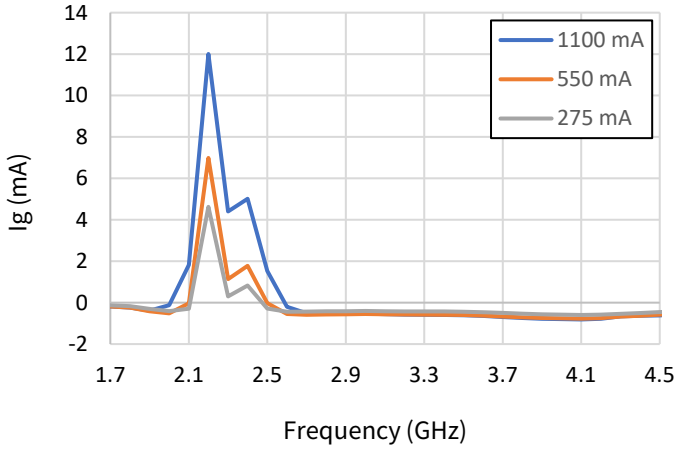
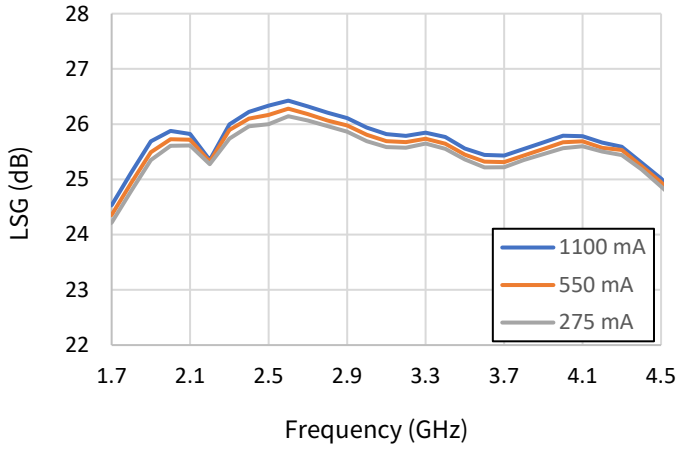



**Figure 17: LSG v. Frequency v. Idq**



Test conditions unless otherwise noted: Vd=28 V, Idq=550 mA, CW, Pin = 21 dBm, $T_{base}$=25 °C, Frequency: 3GHz

**Figure 18: Pout v. Pin v. Frequency**

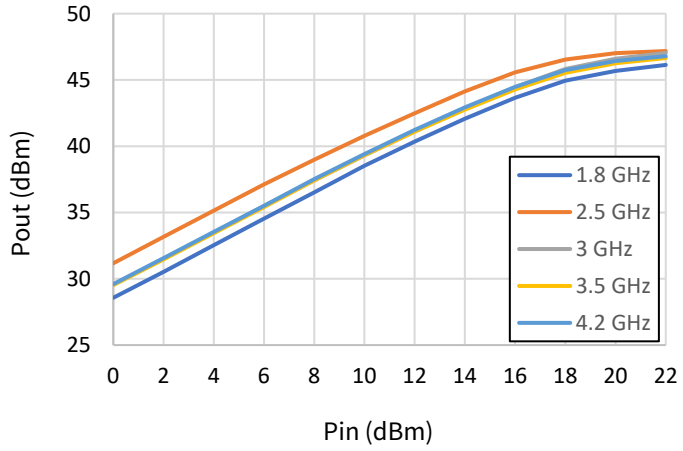



**Figure 19: PAE v. Pin v. Frequency**

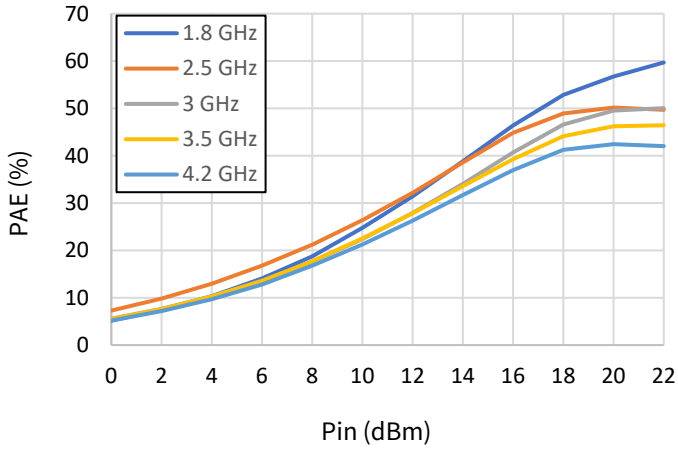



**Figure 20: Id v. Pin v. Frequency**

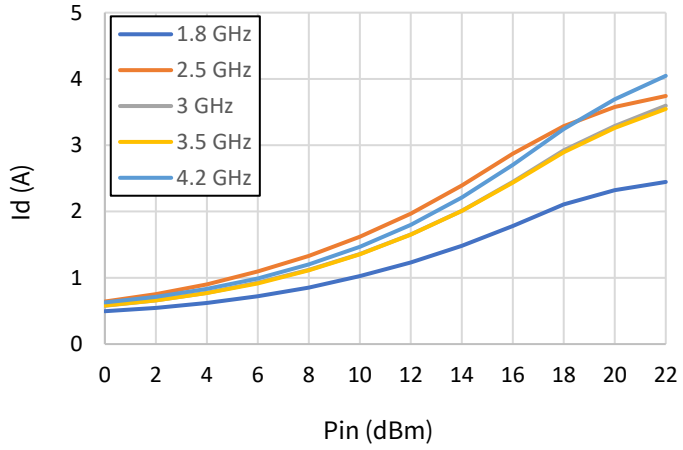



**Figure 21: Ig v. Pin v. Frequency**

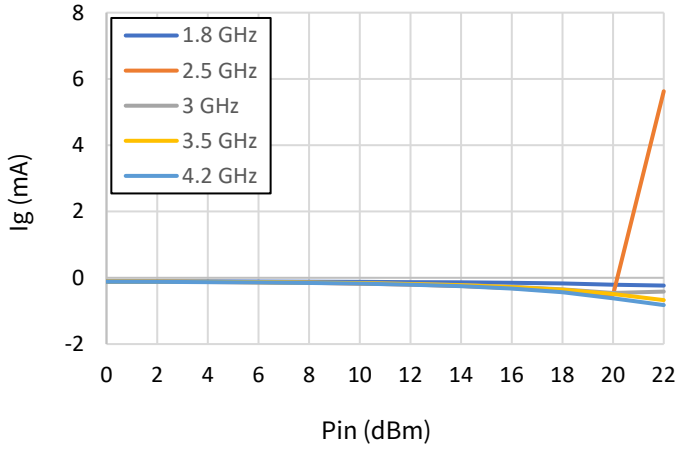
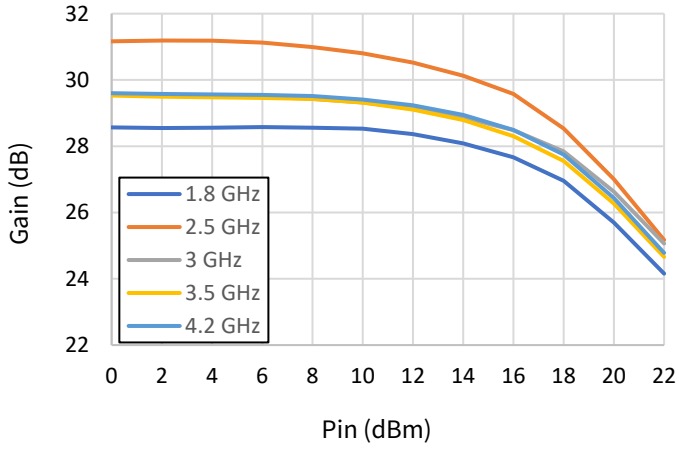



**Figure 22: Gain v. Pin v. Frequency**



Test conditions unless otherwise noted: Vd=28 V, Idq=550 mA, CW, Pin = 21 dBm, $T_{base}$=25 °C, Frequency: 3GHz

**Figure 23: Pout v. Pin v. Temperature**

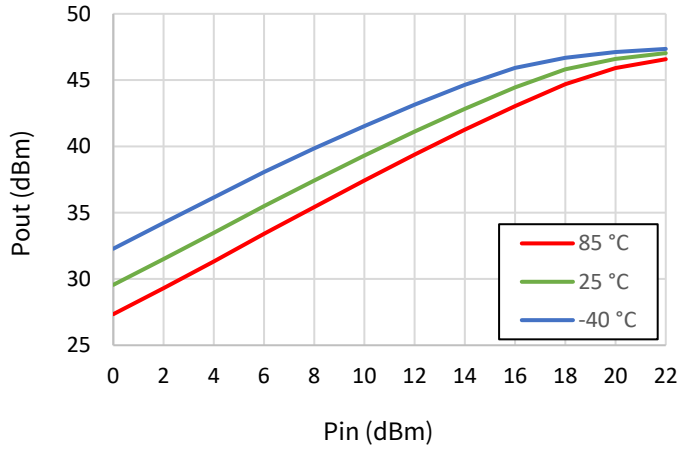



**Figure 24: PAE v. Pin v. Temperature**

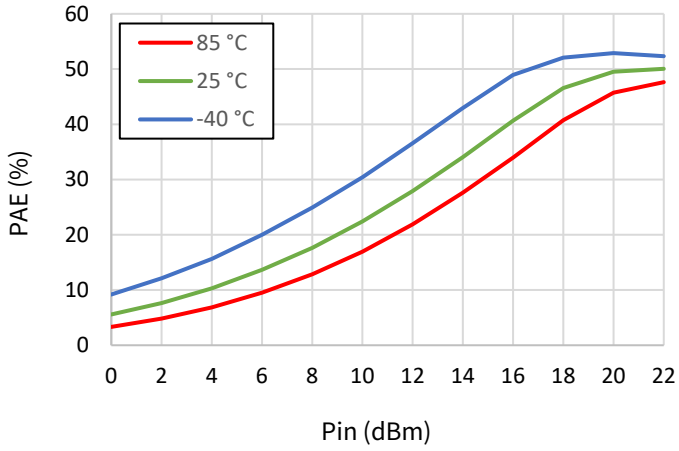



**Figure 25: Id v. Pin v. Temperature**

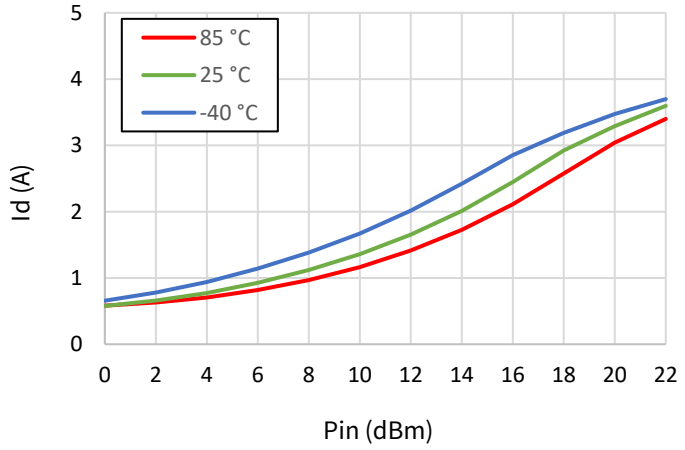



**Figure 26: Ig v. Pin v. Temperature**

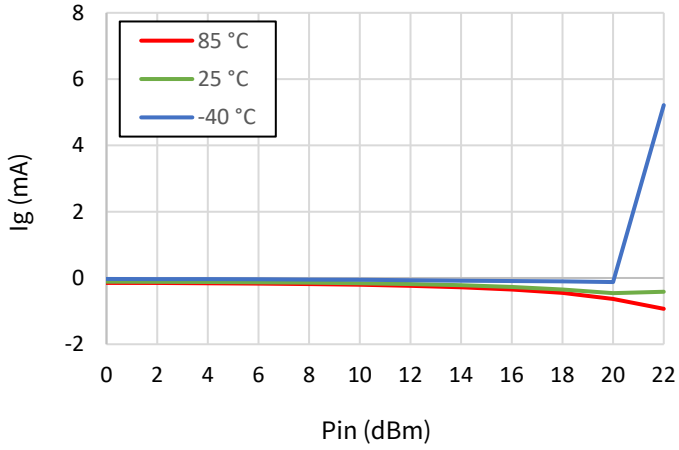
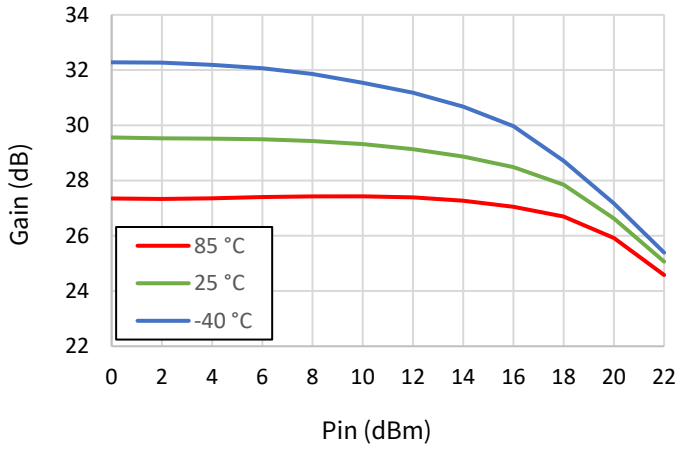



**Figure 27: Gain v. Pin v. Temperature**



Test conditions unless otherwise noted: Vd=28 V, Idq=550 mA, CW, Pin = 21 dBm, $T_{base}$=25 °C, Frequency: 3GHz

**Figure 28: Pout v. Pin v. Vd**

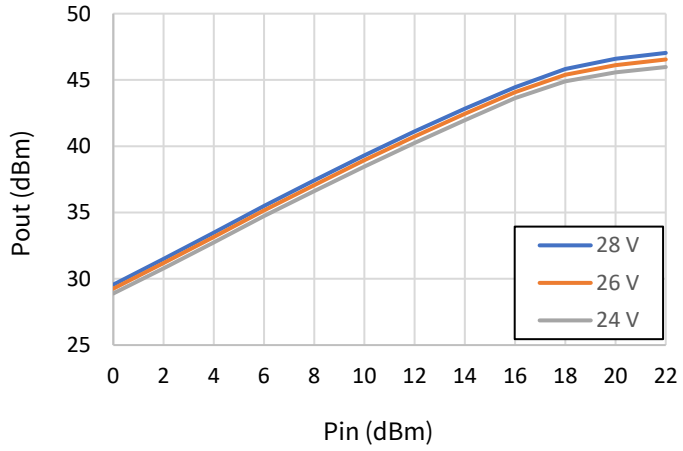



**Figure 29: PAE v. Pin v. Vd**

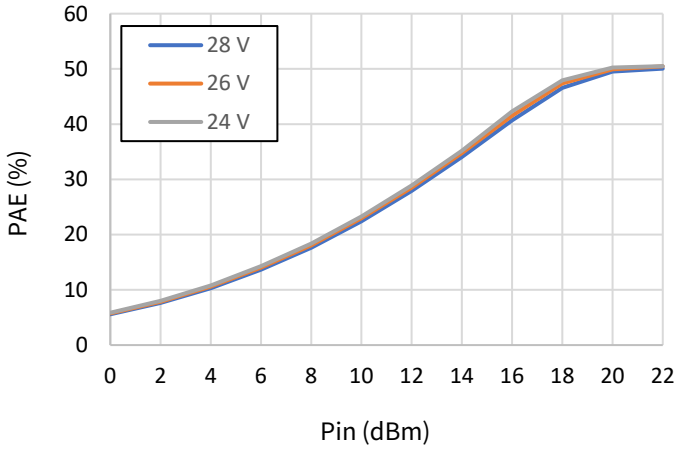



**Figure 30: Id v. Pin v. Vd**

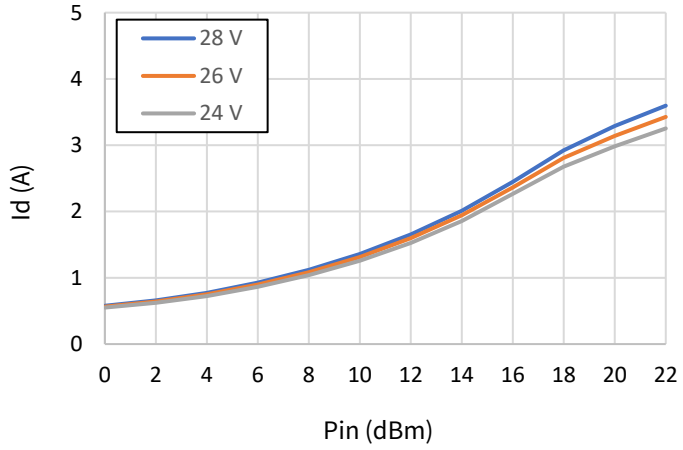



**Figure 31: Ig v. Pin v. Vd**

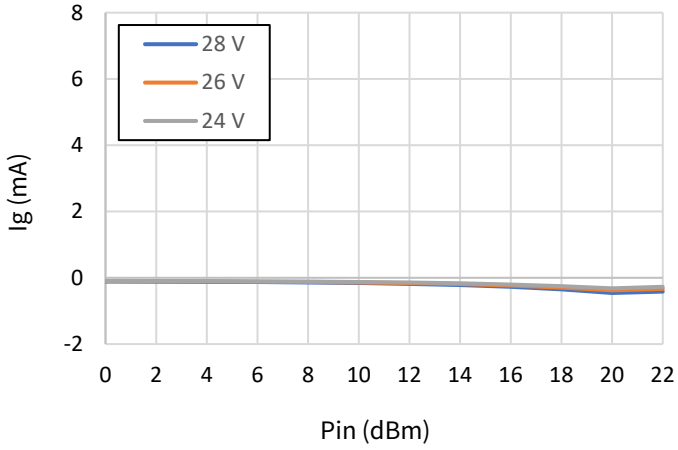
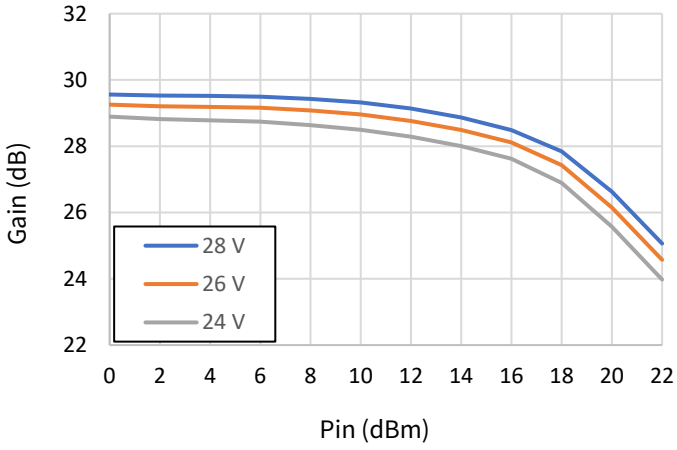



**Figure 32: Gain v. Pin v. Vd**



Test conditions unless otherwise noted: Vd=28 V, Idq=550 mA, CW, Pin = 21 dBm, $T_{base}$=25 °C, Frequency: 3GHz

**Figure 33: Pout v. Pin v. Idq**

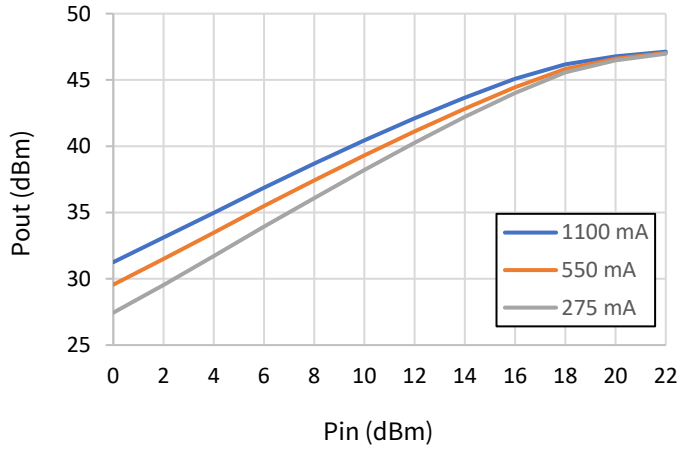



**Figure 34: PAE v. Pin v. Idq**

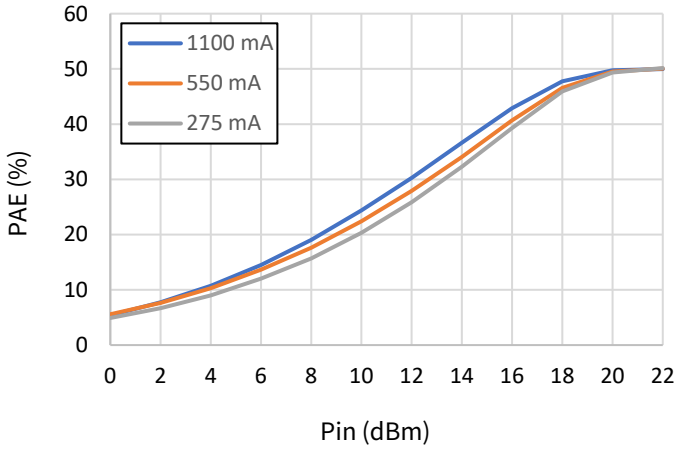



**Figure 35: Id v. Pin v. Idq**

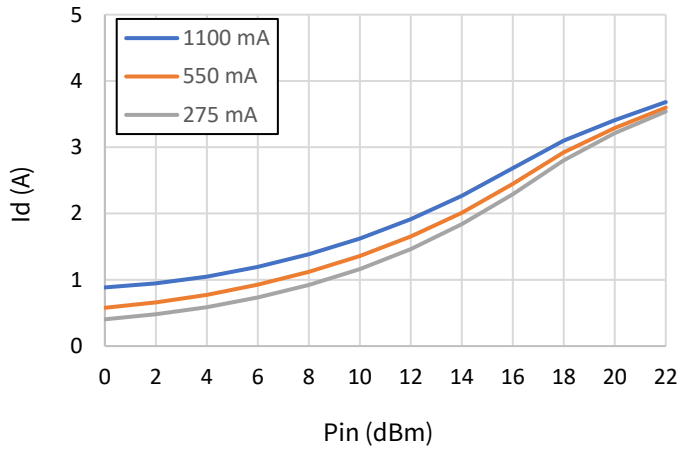



**Figure 36: Ig v. Pin v. Idq**

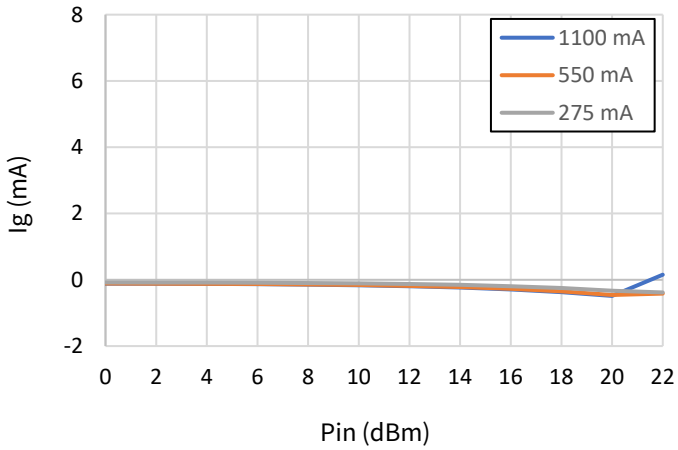
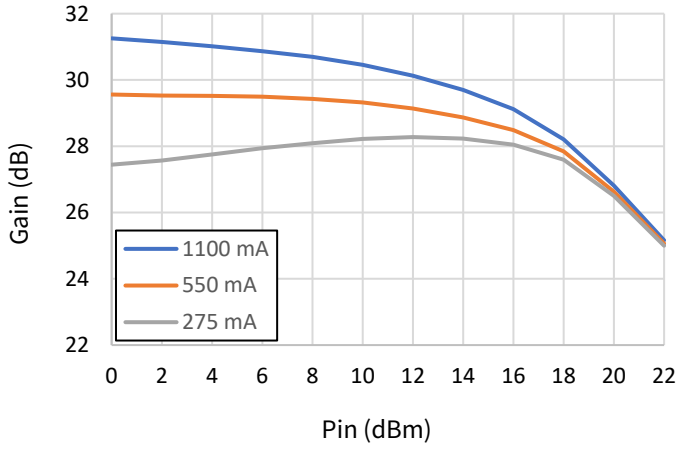



**Figure 37: Gain v. Pin v. Idq**



Test conditions unless otherwise noted: Vd=28 V, Idq=550 mA, CW, Pin = -20 dBm, $T_{base}$=25 °C

**Figure 38: S21 v. Frequency v. Temperature**

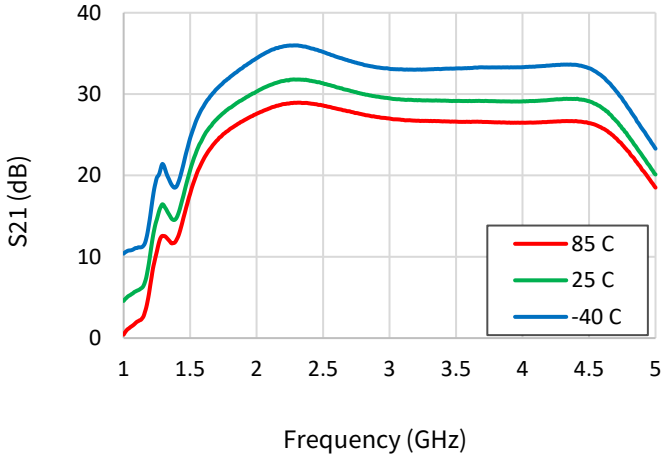



**Figure 39: S21 v. Frequency v. Vd**

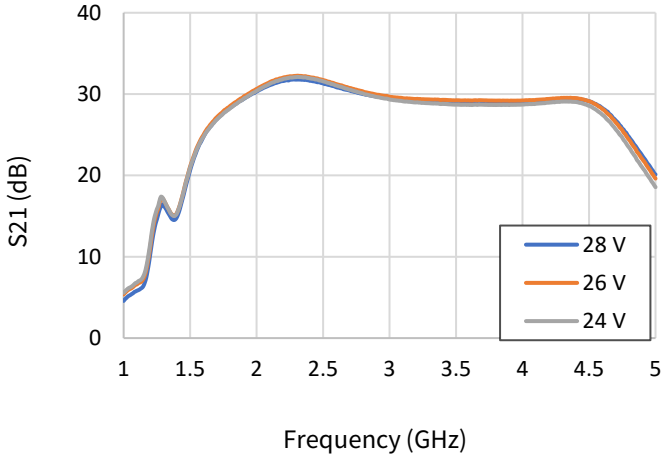



**Figure 40: S11 v. Frequency v. Temperature**

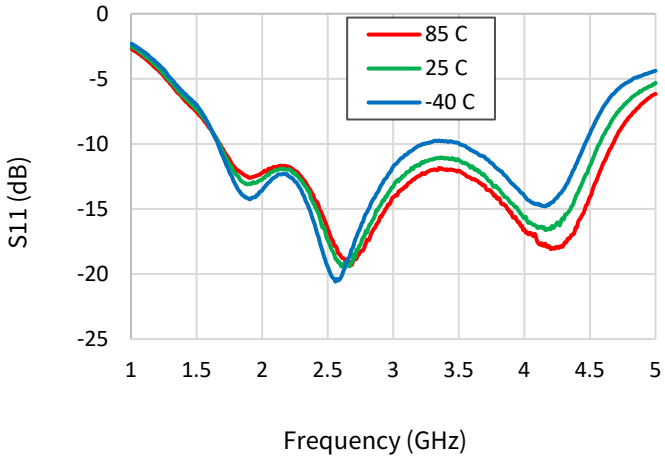



**Figure 41: S11 v. Frequency v. Vd**

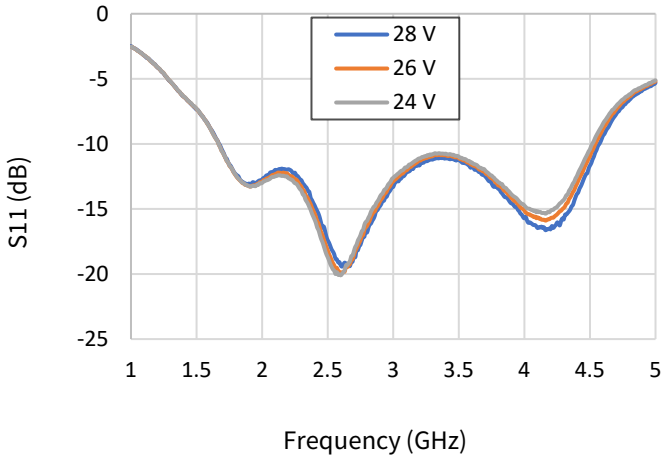



**Figure 42: S22 v. Frequency v. Temperature**

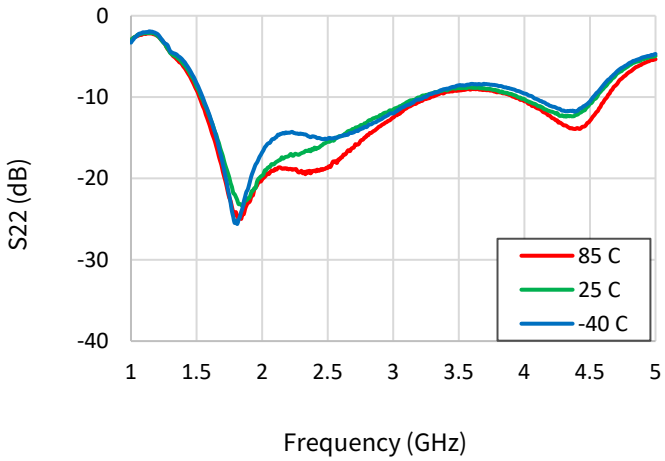
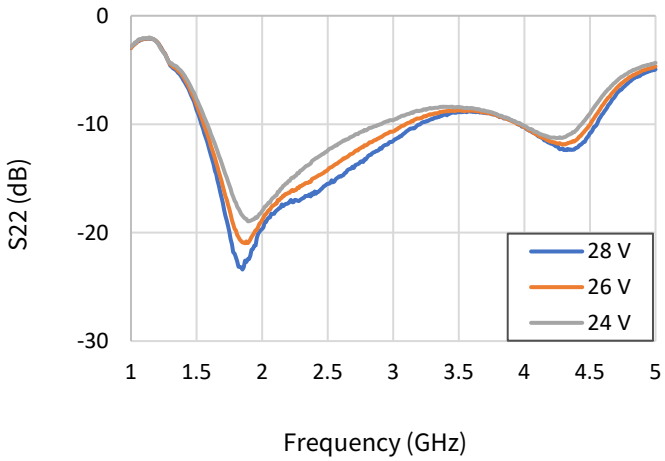



**Figure 43: S22 v. Frequency v. Vd**



Test conditions unless otherwise noted: Vd=28 V, Idq=550 mA, CW, Pin = -20 dBm, $T_{base}$=25 °C

**Figure 44: S21 v. Frequency v. Idq**

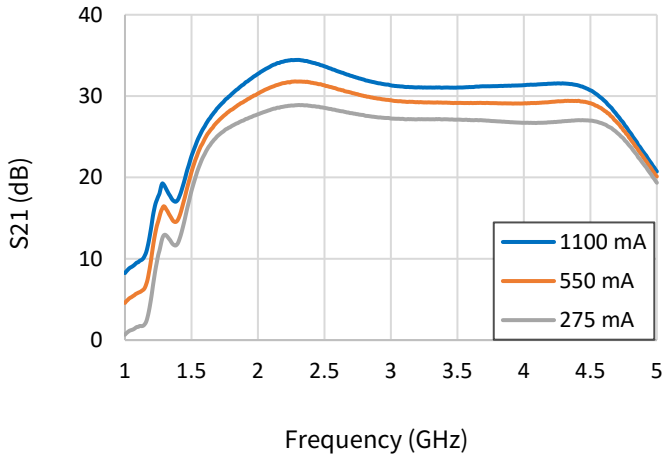



**Figure 45: S11 v. Frequency v. Idq**

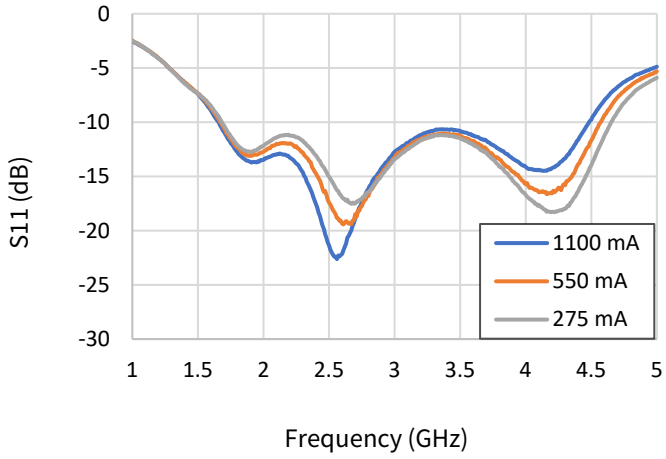
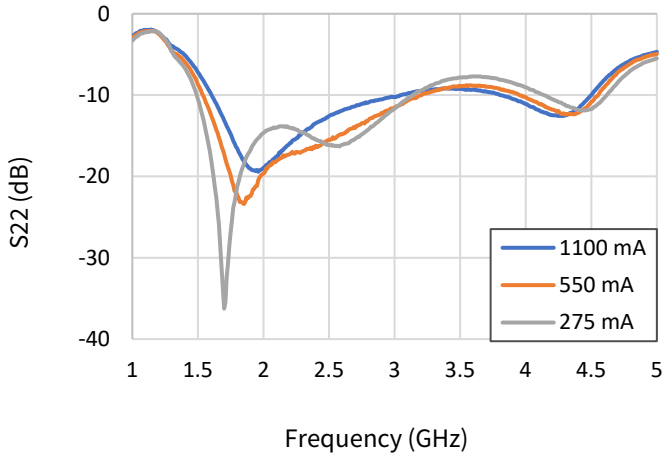



**Figure 46: S22 v. Frequency v. Idq**



Test conditions unless otherwise noted: Vd=28 V, Idq=550 mA, CW, Pin = 21 dBm, $T_{base}$=25 °C
Frequency 1= 1.8 GHz, Frequency 2 = 3 GHz, Frequency 3 = 4.2 GHz

**Figure 47: 2f v. Pout v. Temperature, F1**

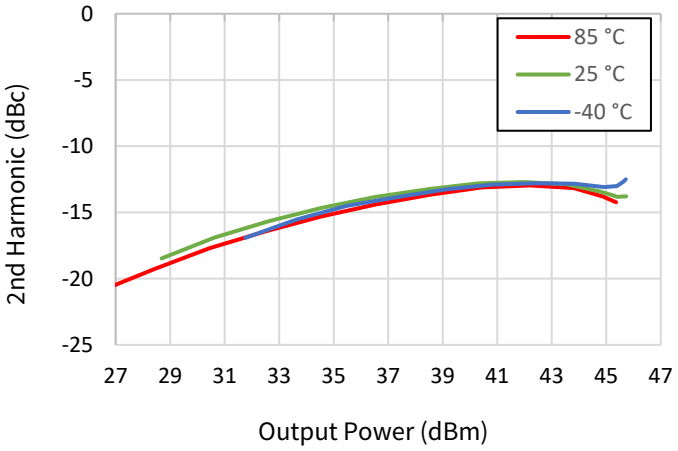



**Figure 48: 2f v. Pout v. Vd, F1**

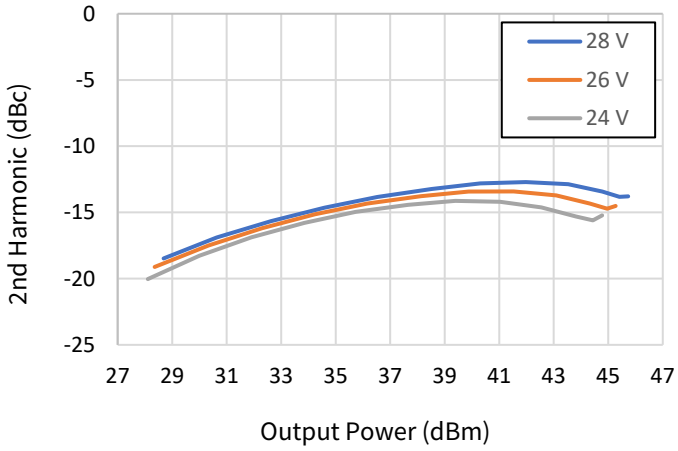



**Figure 49: 2f v. Pout v. Temperature, F2**

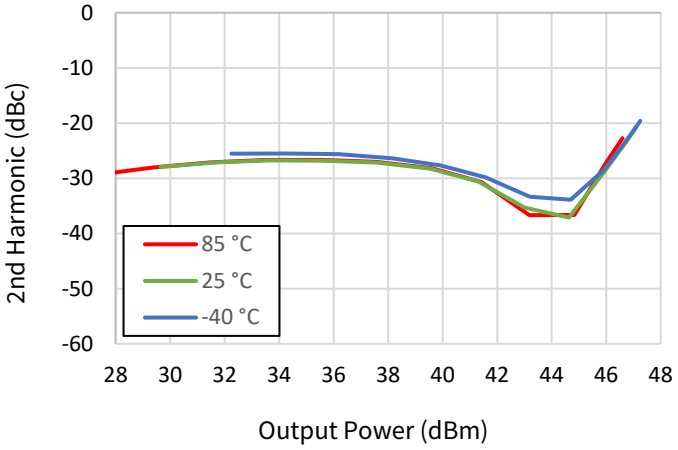



**Figure 50: 2f v. Pout v. Vd, F2**

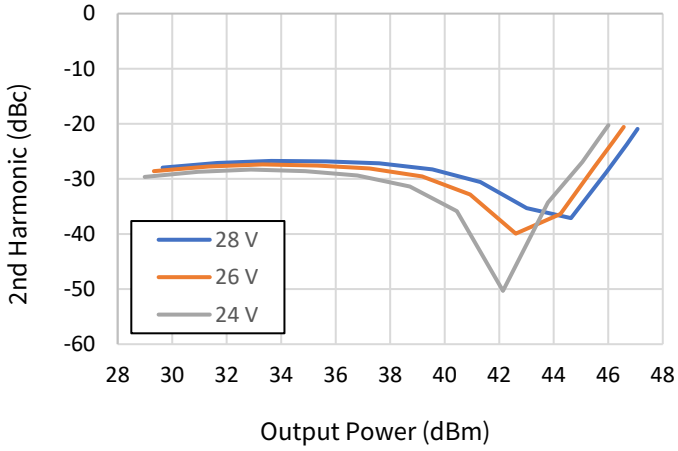



**Figure 51: 2f v. Pout v. Temperature, F3**

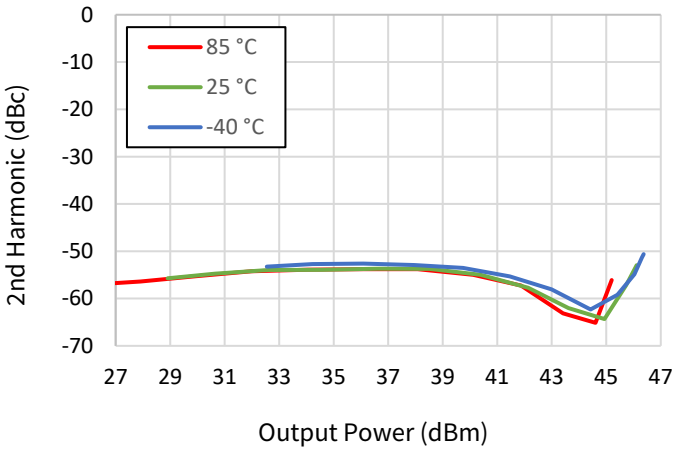
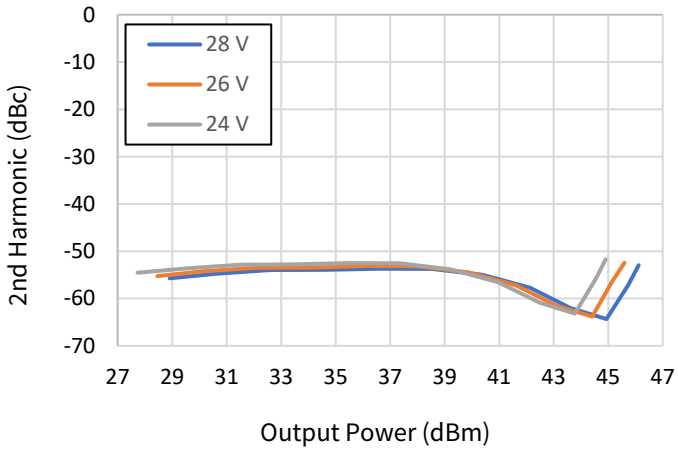


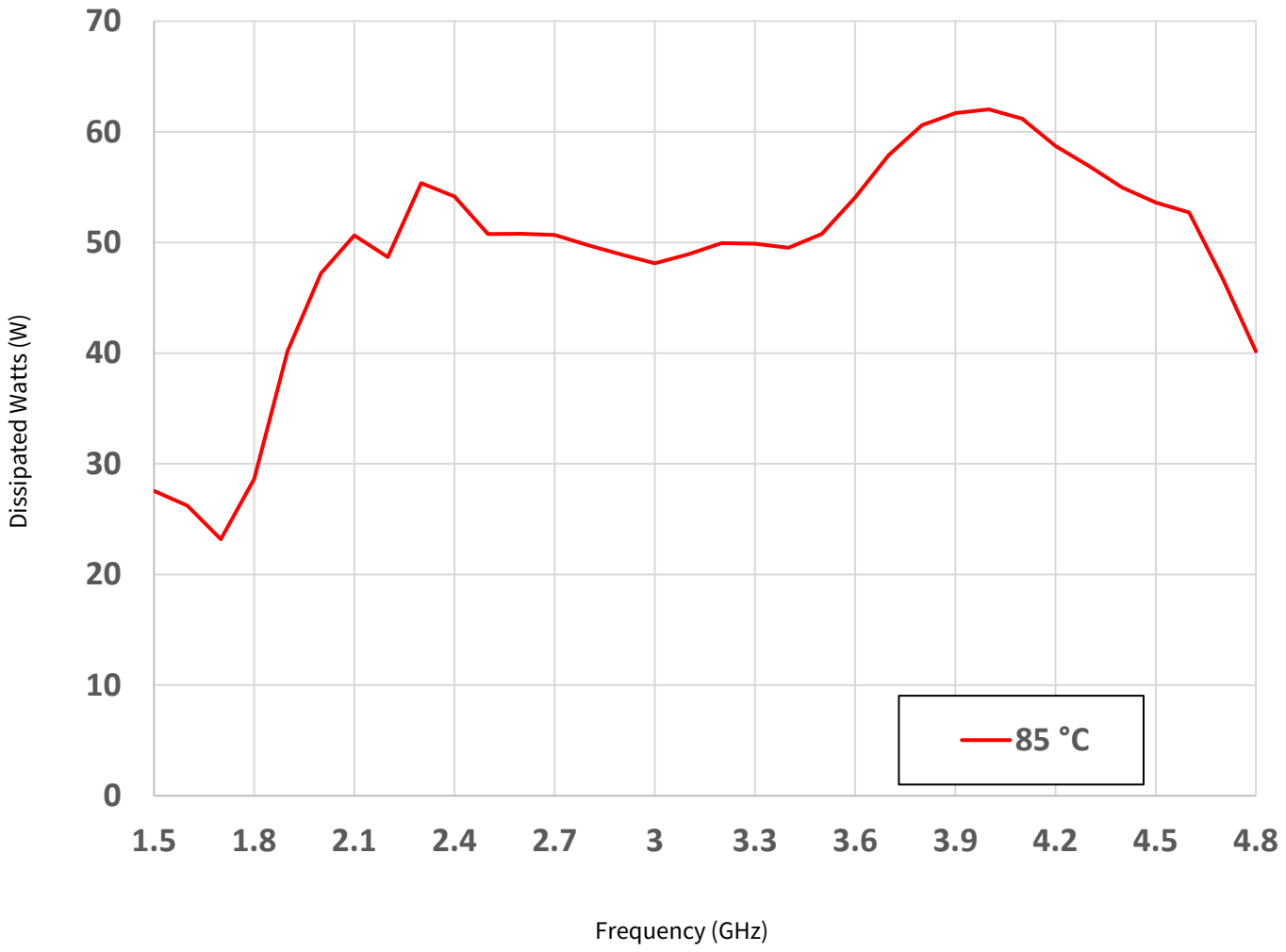

**Figure 52: 2f v. Pout v. Vd, F3**



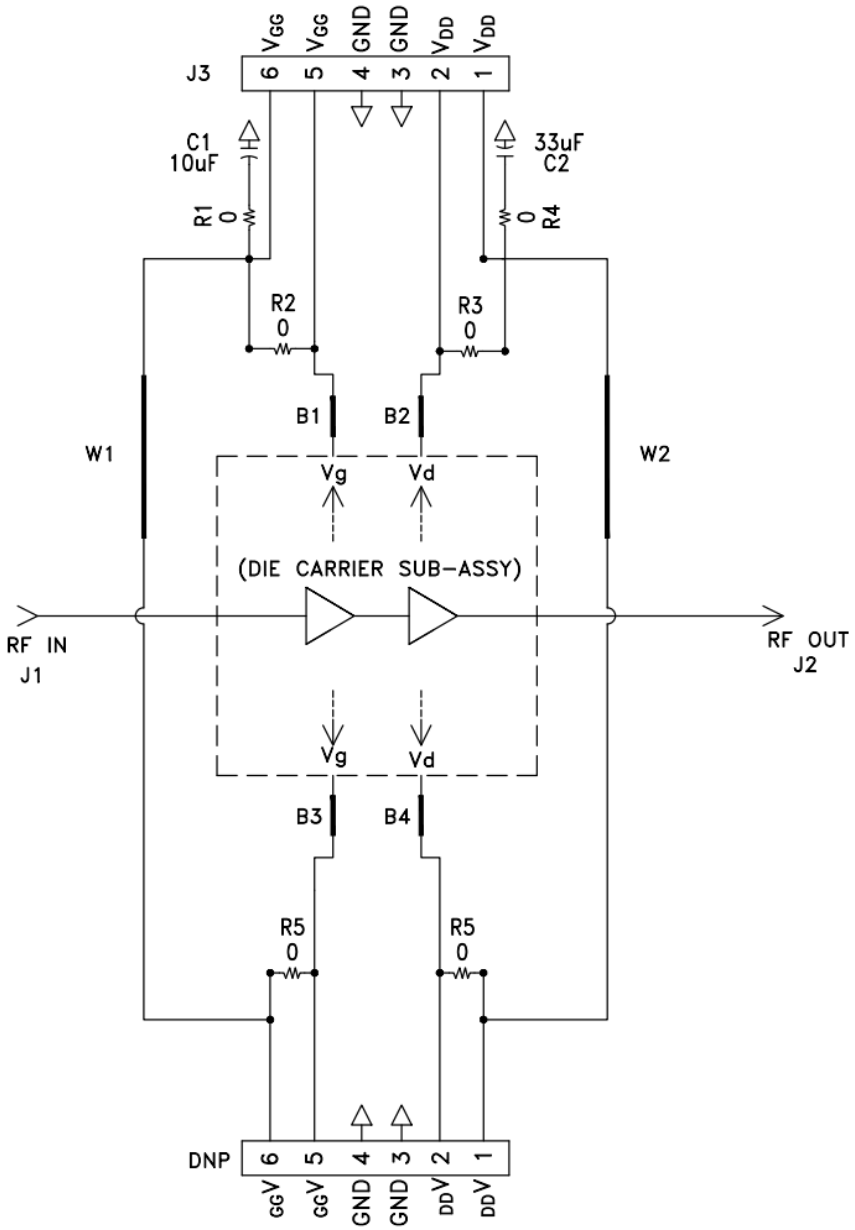
## Thermal Characteristics

| Parameter | Symbol | Value | Operating Conditions |
|---|---|---|---|
| Operating Junction Temperature | $T_J$ | 152.8°C | Freq = 3 GHz, $V_d$ = 28 V, $I_{dq}$ = 550 mA, $I_{drive}$ = 3.25 A, $P_{in}$ = 21 dBm, $P_{out}$ = 46.1 dBm, $P_{diss}$ = 40.7 W, $T_{case}$ = 85°C, CW |
| Thermal Resistance, Junction to Case | $R_{\theta JC}$ | 1.67 °C/W | |

### Power Dissipation v. Frequency (Tcase = 85°C)



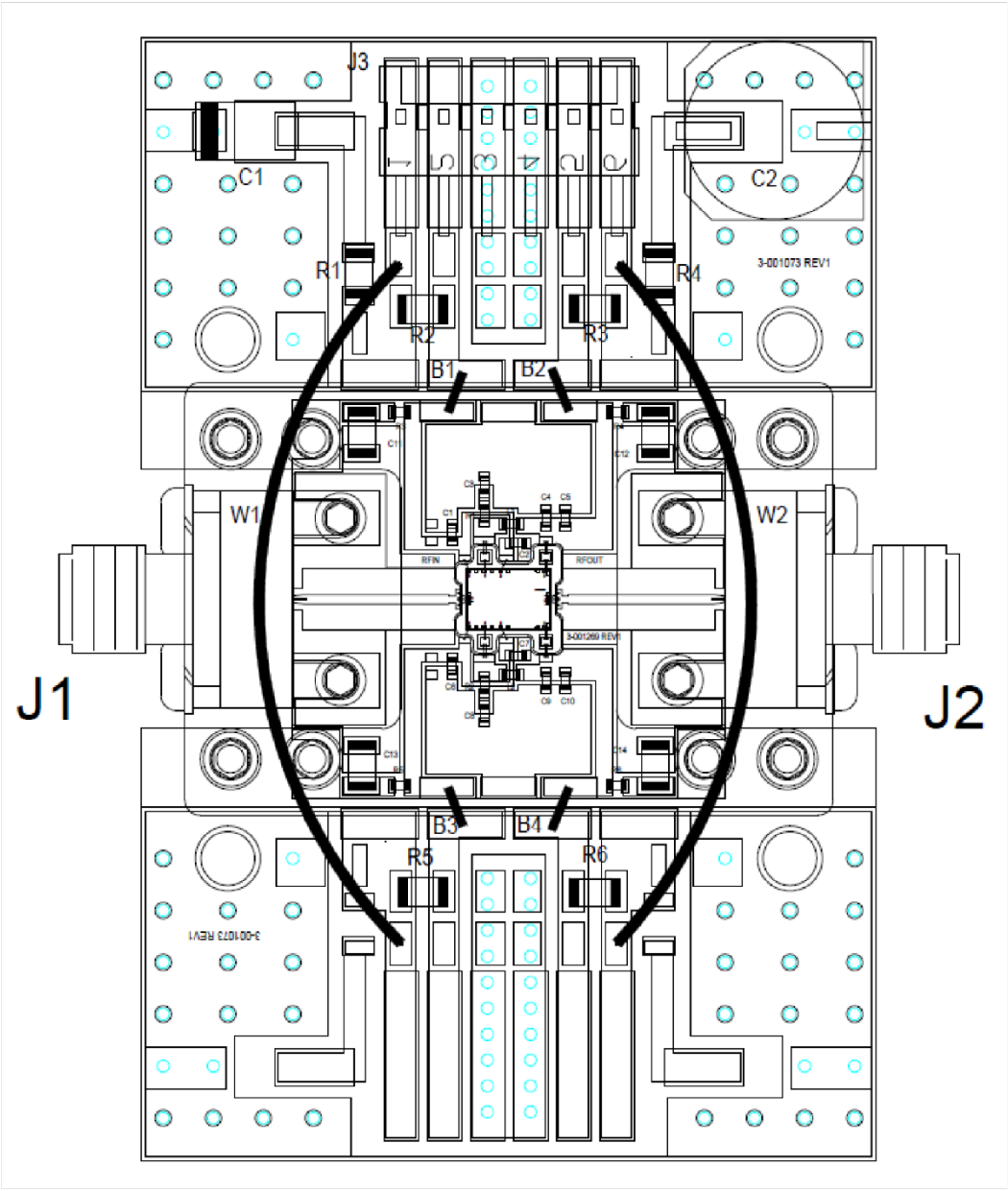
## CMPA1842040D-AMP Evaluation Board Schematic Drawing




## CMPA1842040D-AMP Evaluation Board Bill of Materials

| Reference Designator | Description | Qty |
|---|---|---|
| J1, J2 | CONNECTOR SMA JACK (FEMALE) END LAUNCH | 2 |
| J3 | 6-PIN DC HEADER, RIGHT ANGLE | 1 |
| R1-R6 | RESISTOR, 0 OHMS, 1206 | 6 |
| C1 | CAPACITOR, 10UF, TANTALUM | 1 |
| C2 | CAPACITOR, 33UF, ELECTROLYTIC | 1 |
| B1-B4 | JUMPER WIRE | 4 |
| W1-W2 | WIRE, BLACK, 22AWG (~2”) | 2 |

## CMPA1842040D-AMP Evaluation Board Assembly Drawing



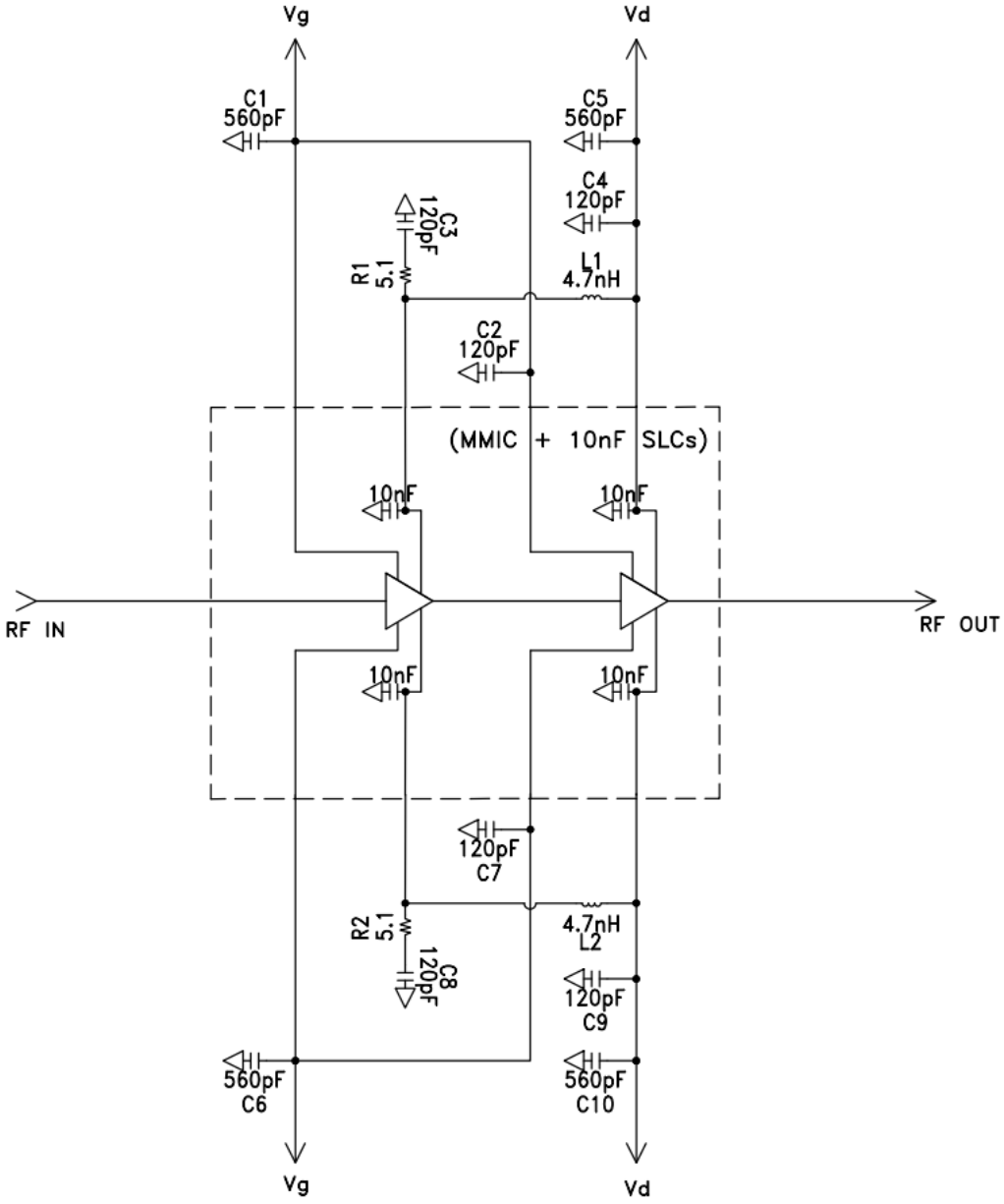

## Bias On Sequence

1. Ensure RF is turned-off
2. Apply pinch-off voltage of -5 V to the gate (Vg)
3. Apply nominal drain voltage (Vd)
4. Adjust Vg to obtain desired quiescent drain current (Idq)
5. Apply RF

## Bias Off Sequence

1. Turn RF off
2. Apply pinch-off to the gate (Vg=-5V)
3. Turn off drain voltage (Vd)
4. Turn off gate voltage (Vg)

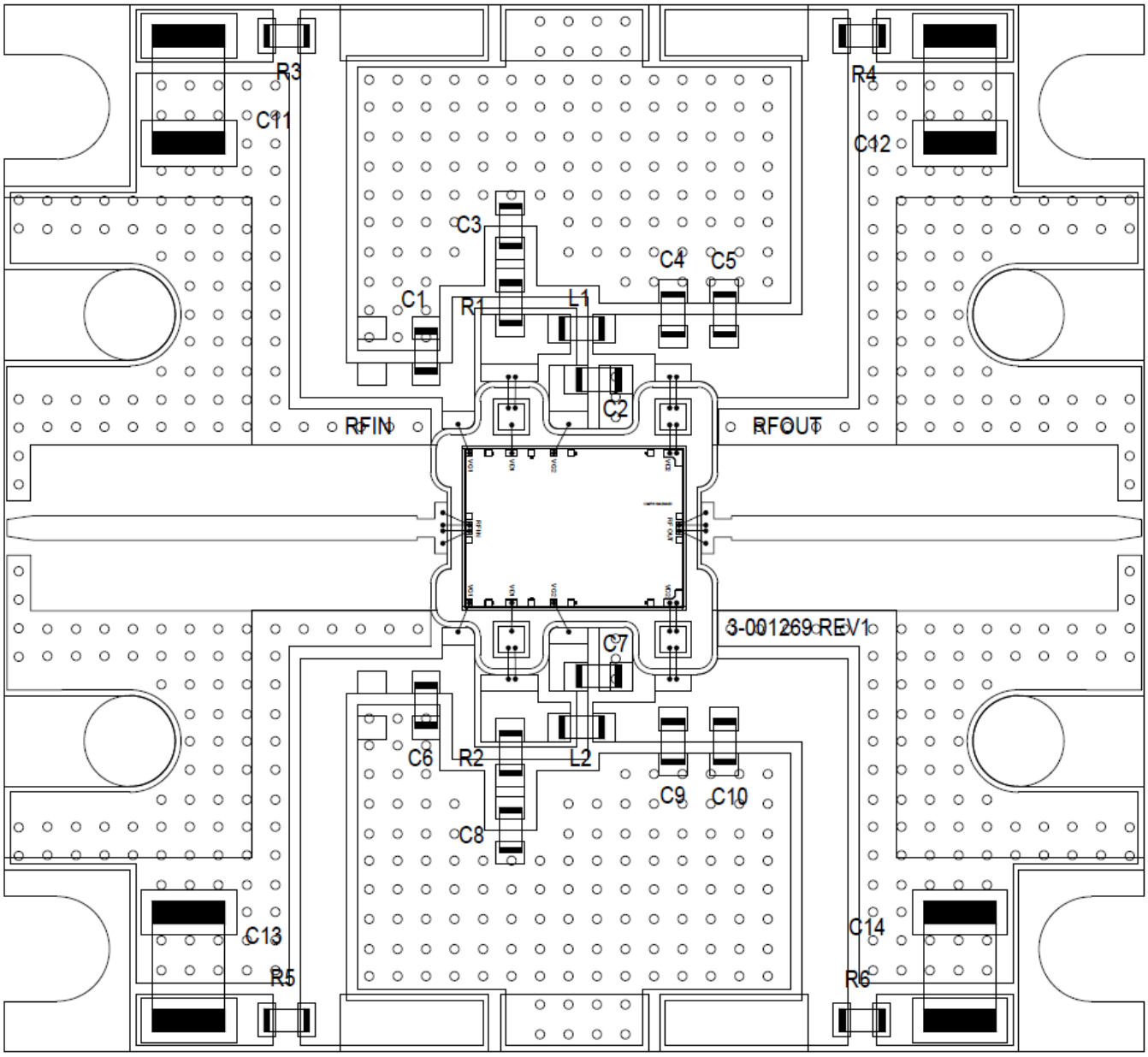
## CMPA1842040D-AMP Carrier Schematic Drawing



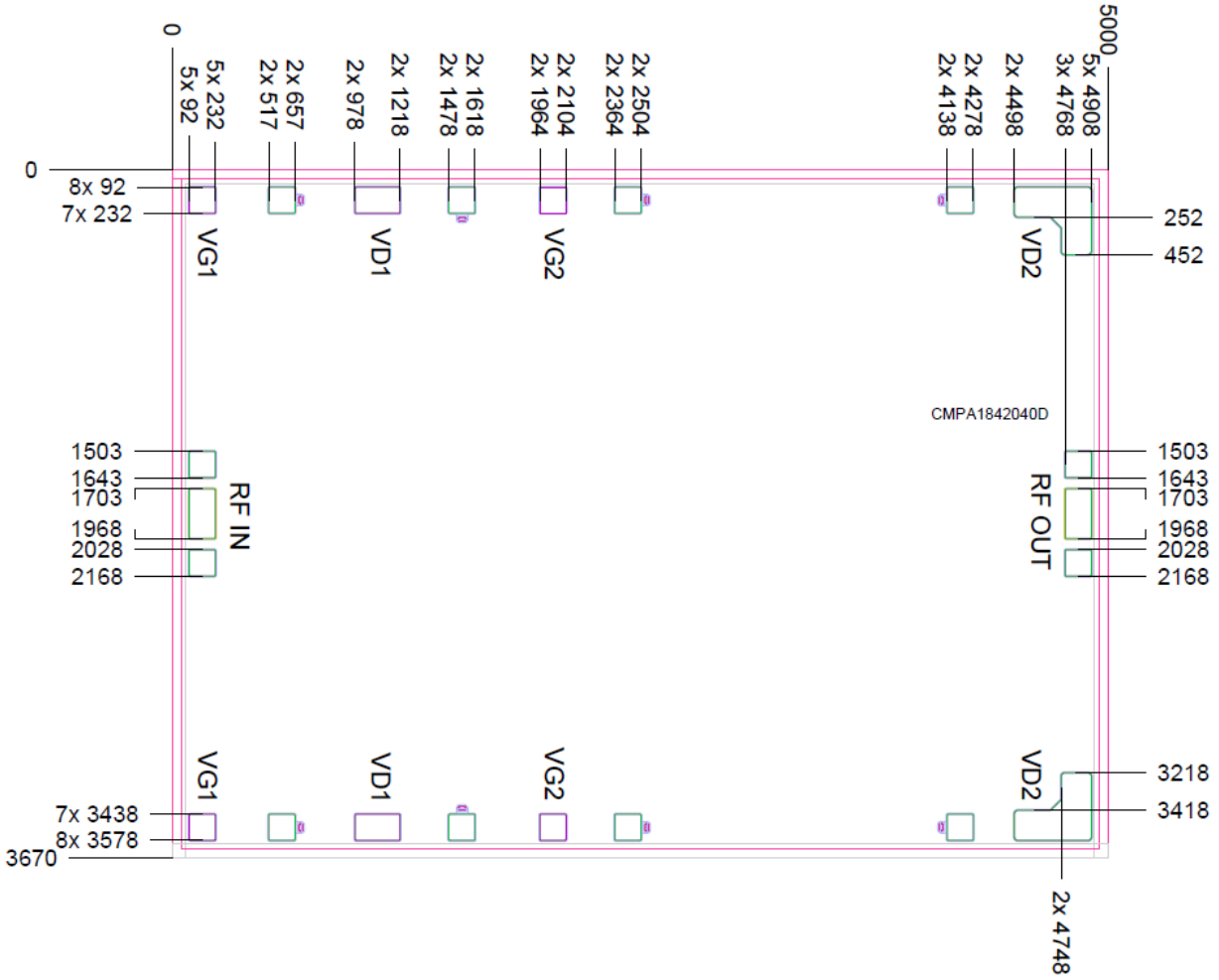

## CMPA1842040D-AMP Carrier Bill of Materials

| Reference Designator | Description | Qty |
|---|---|---|
| C1,C5,C6,C10 | CAPACITOR, 0402, 560pF | 4 |
| C2-C4,C7-C9 | CAPACITOR, 0402, 120pF | 6 |
| R1,R2 | RESISTOR, 0402, 5.1 Ohm | 2 |
| L1,L2 | INDUCTOR, 0402, 4.7nH | 2 |
| C11-C14 | CAPACITOR, 1206, 10uF, 50V | 4 |
| R3-R6 | RESISTOR, 0603, 0 Ohm | 4 |

## CMPA1842040D-AMP Carrier Assembly Drawing



## Product Dimensions




Overall die size is 3670 x 5000 (+/-50) microns. Die thickness 75 (+/-10) microns.
All Gate and Drain pads must be wire bonded for electrical connection.

| Function | Description | Pad Size (um) | Note |
|---|---|---|---|
| RF IN | RF Input pad. Matched to 50 ohms. DC grounded. | 150 x 275 | 2 |
| VG1 (top & bottom) | Gate control for stage 1 | 150 x 150 | 1 |
| VG2 (top & bottom) | Gate control for stage 2 | 150 x 150 | 1 |
| VD1 (top & bottom) | Drain supply for stage 1 | 250 x 150 | 1 |
| VD2 (top & bottom) | Drain supply for stage 2 | 420 x 170 | 1 |
| RF OUT | RF Output pad. Matched to 50 ohms. | 150 x 275 | 2 |

Notes

[1] Attach bypass capacitor to pads per application circuit.

[2] The RF Input and Output pad have a ground-signal-ground with a nominal pitch of 262.5 um.

## Electrostatic Discharge (ESD) Classification

| Parameter | Symbol | Class | Classification Level | Test Methodology |
|---|---|---|---|---|
| Human Body Model | HBM | TBD | ANSI/ESDA/JEDEC JS-001 Table 3 | JEDEC JESD22 A114-D |

## Product Ordering Information

| Part Number | Description | MOQ Increment | Image |
|---|---|---|---|
| CMPA1842040D | 1.8 – 4.2 GHz, 45W GaN MMIC | 1 Each |  |
| CMPA1842040D-AMP | Evaluation Board w/ PA | 1 Each | |

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