Features

- Saturated Power: 35 W
- Power Added Efficiency: 40%
- Large Signal Gain: 14 dB
- Small Signal Gain: 18 dB
- Input Return Loss: -12 dB
- Output Return Loss: -10 dB
- CW Operation

Applications

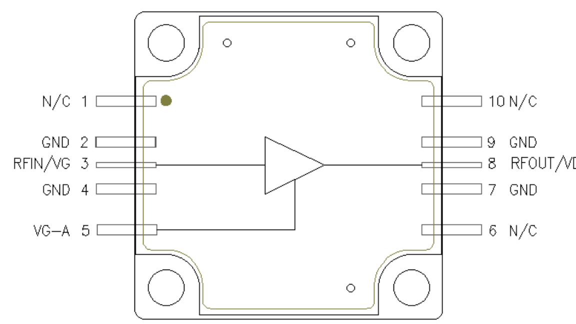
- Military and Commercial Radar
- EMC Amplifiers
- Electronic Warfare
- General Amplification

Description

MACOM's CMPA0335030F is a broadband, 35 W package MMIC HPA utilizing MACOM's high performance, 0.15 µm GaN on SiC production process. Using a cascode NDPA architecture, the CMPA0335030F operates from 0.3 – 3.5 GHz and supports a variety of both defense and commercial-related applications. The CMPA0335030F achieves 35 W of saturated output power with 14 dB of large signal gain and typically 40% power-added efficiency under CW operation.

Packaged in a 15x15 mm bolt-down, flange package, the CMPA0335030F provides superior RF performance and thermal management allowing customers to improve SWaP-C benchmarks in their next-generation systems.

Functional Schematic



Pin Configuration[1,2]

Pin #	Function
1, 6, 10	No Connection
2, 4, 7, 9	RF/DC Ground
3	RF Input/ VG
5	VG-A (alternate)
8	RF Output / VD

1. MACOM recommends connecting No Connection (N/C) pins to ground.
2. The package base (flange) must be connected to RF, DC and thermal ground.

Ordering Information

Part Number	Package (MOQ/ Mult)
CMPA0335030F	Tray (10/10)
CMPA0335030F-AMP	Sample Board (1/1)

RF Electrical Specifications: V_D = 50 V, I_{DQ} = 500 mA, CW, T_C = 25°C, Z_0 = 50 Ω

Parameter	Test Conditions	Frequency (GHz)	Units	Min.	Typ.	Max.
Output Power	P_{IN} = 32 dBm	0.3 1.4 2.6 3.5	dBm	— 45.5 45.5 45.5	45.5 46.4 46.0 46.3	—
Power Added Efficiency	P_{IN} = 32 dBm	0.3 1.4 2.6 3.5	%	— 40 35 35	55 43 40 39	—
Large Signal Gain	P_{IN} = 32 dBm	0.3 1.4 2.6 3.5	dB	— 13.5 13.5 13.5	13.5 14 14 14	—
Small Signal Gain	P_{IN} = -20 dBm	0.3 1.4 2.6 3.5	dB	—	20 18 18 18	—
Input Return Loss	P_{IN} = -20 dBm	0.3—3.5	dB	—	-12	—
Output Return Loss	P_{IN} = -20 dBm	0.3—3.5	dB	—	-10	—

DC Electrical Specifications:

Parameter	Units	Min.	Typ.	Max.
Drain Voltage	V	—	50	—
Gate Voltage	V	—	-1.92	—
Quiescent Drain Current	mA	250	500	750
Saturated Drain Current	A	—	2.0	—

Recommended Operating Conditions

Parameter	Symbol	Unit	Min.	Typ.	Max.
Input Power	P_{IN}	dBm		32	
Drain Voltage	V_D	V		50	
Gate Voltage	V_G	V		-1.92	
Quiescent Drain Current	I_{DQ}	mA		500	
Operating Temperature	T_C	°C	-40		+85

Absolute Maximum Ratings[3,4]

Parameter	Symbol	Unit	Min.	Max.
Input Power	P_{IN}	dBm		34
Drain to Source Breakdown Voltage	V_{DS}	V		84
Operating Drain Voltage	V_D	V		53
Gate Voltage	V_G	V	-8	+2
Drain Current	I_D	A		2.3
Gate Current	I_G	mA		8.32
Dissipated Power @ +85°	P_{DISS}	W		64
VSWR				5:1
Junction Temperature (MTTF > 1E6 Hrs)	T_J	°C		+225
Storage Temperature	T_{STG}	°C	-65	+150
Mounting Temperature (30 seconds)	T_M	°C		+260
Screw Torque	τ	in-oz		40

3. Exceeding any one or combination of these limits may cause permanent damage to this device.
4. MACOM does not recommend sustained operation near these survivability limits.

Handling Procedures

Please observe the following precautions to avoid damage:

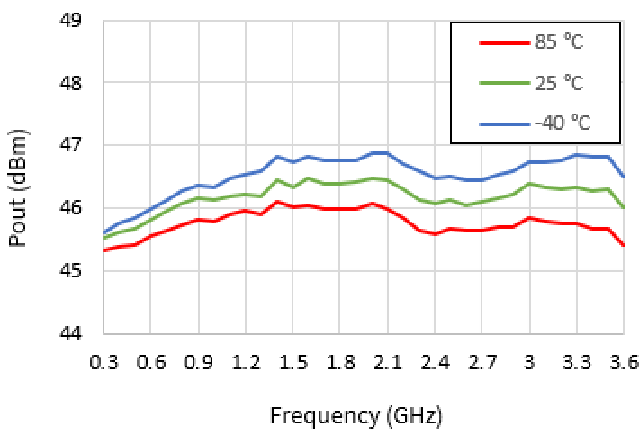
Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM class 1B and CDM class C2b devices.

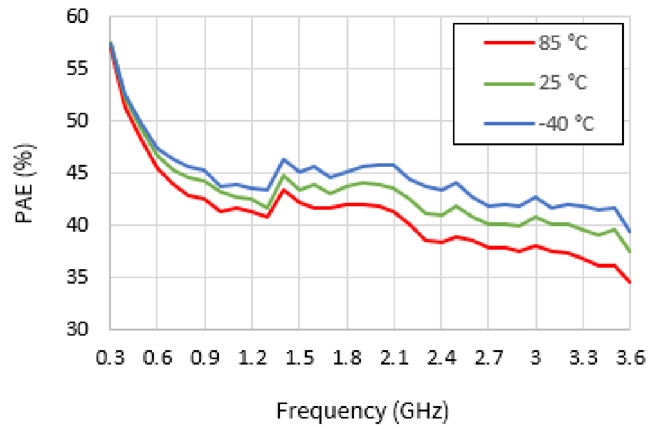
Typical Performance Curves - Large Signal over Temperature:

V_D = 50 V, I_{DQ} = 500 mA, CW, P_{IN} = 32 dBm

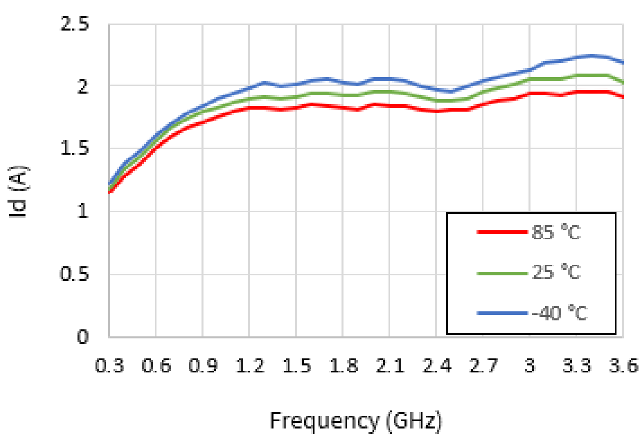
Pout vs. Frequency



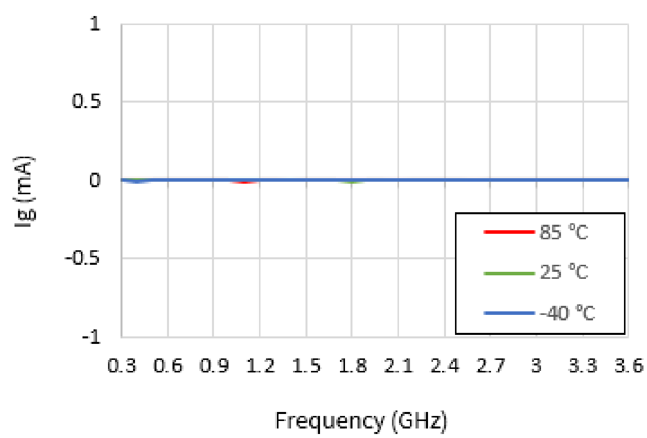
PAE vs. Frequency



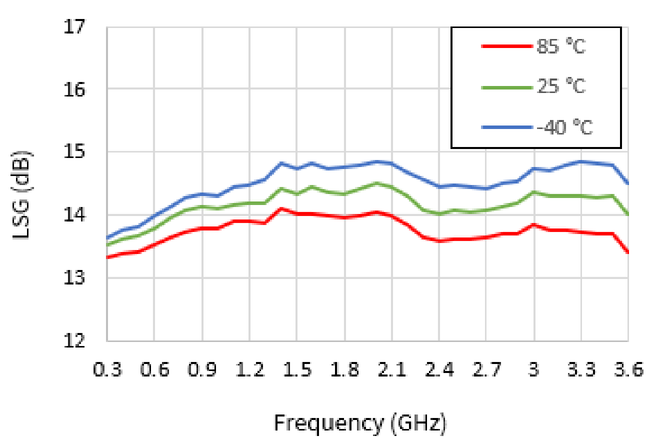
Drain Current vs. Frequency



Gate Current vs. Frequency



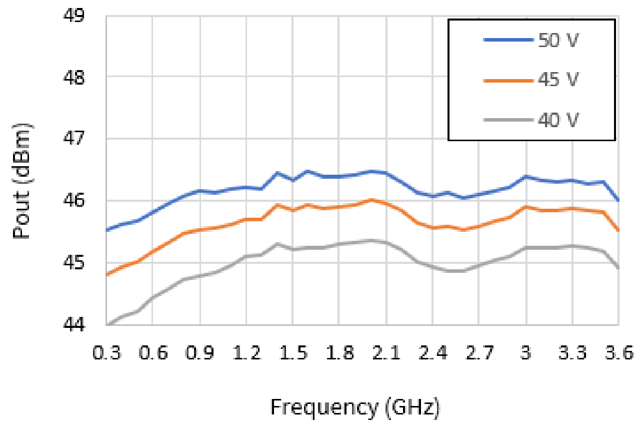
Large Signal Gain vs. Frequency



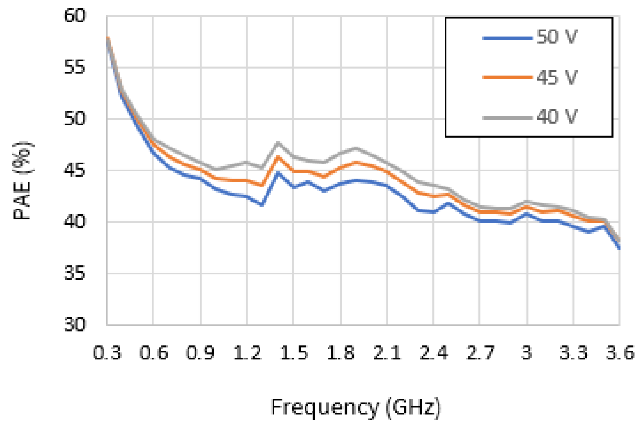
Typical Performance Curves - Large Signal over V_D:

I_{DQ} = 500 mA, CW, P_{IN} = 32 dBm, T_C = 25 °C

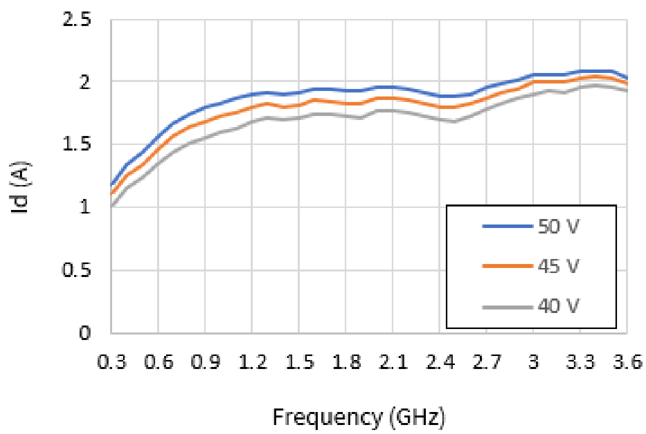
Pout vs. Frequency



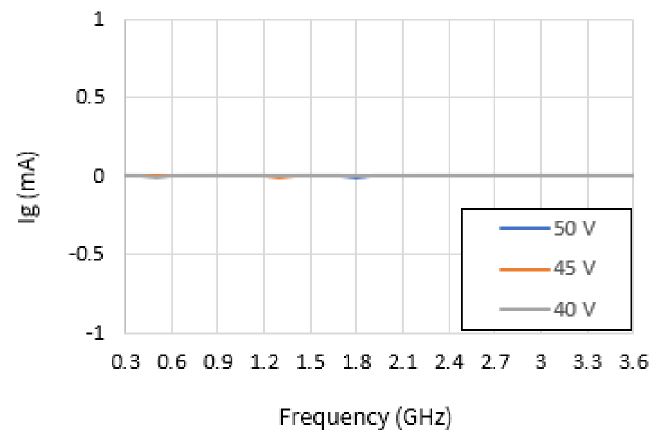
PAE vs. Frequency



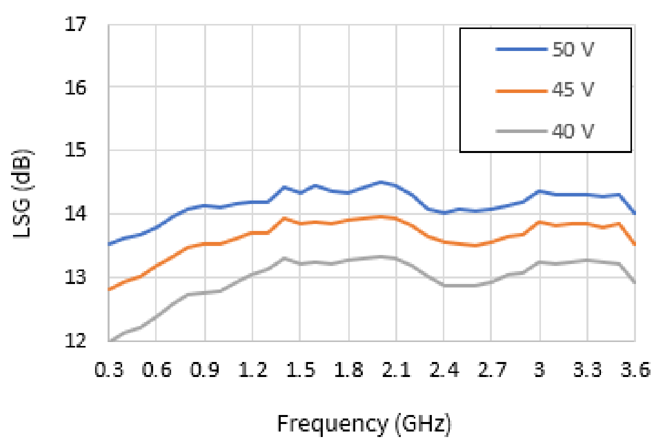
Drain Current vs. Frequency



Gate Current vs. Frequency



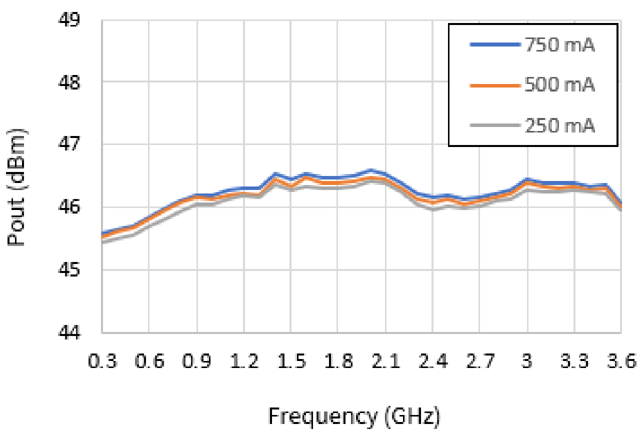
Large Signal Gain vs. Frequency



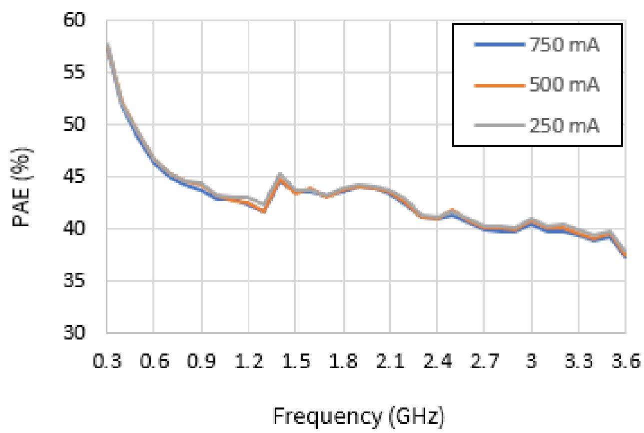
Typical Performance Curves - Large Signal over I_{DQ}:

V_D = 50 V, CW, P_{IN} = 32 dBm, T_C = 25 °C

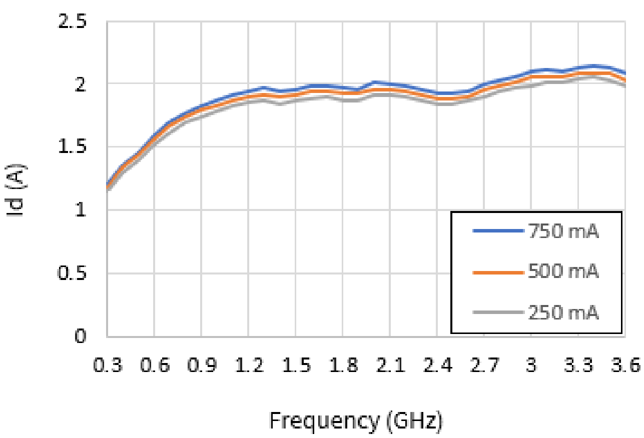
Pout vs. Frequency



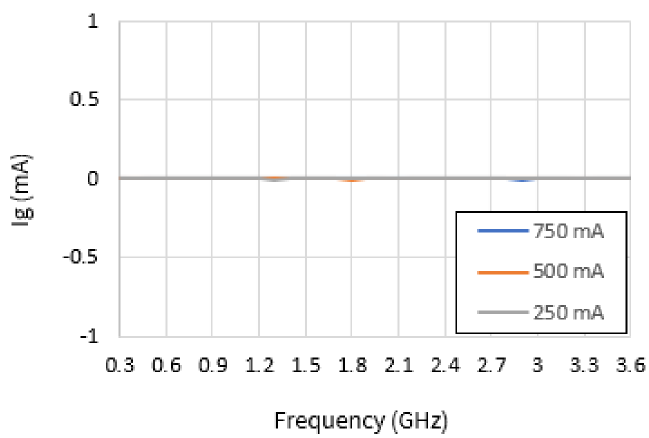
PAE vs. Frequency



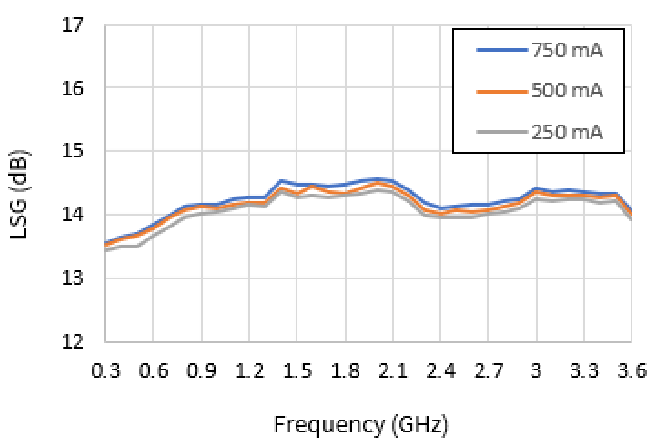
Drain Current vs. Frequency



Gate Current vs. Frequency



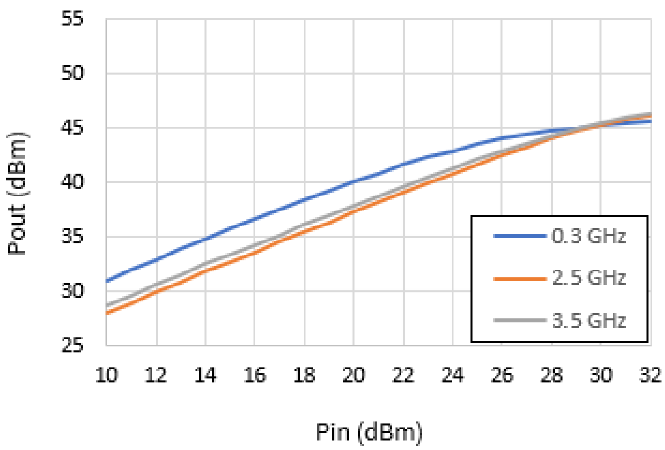
Large Signal Gain vs. Frequency



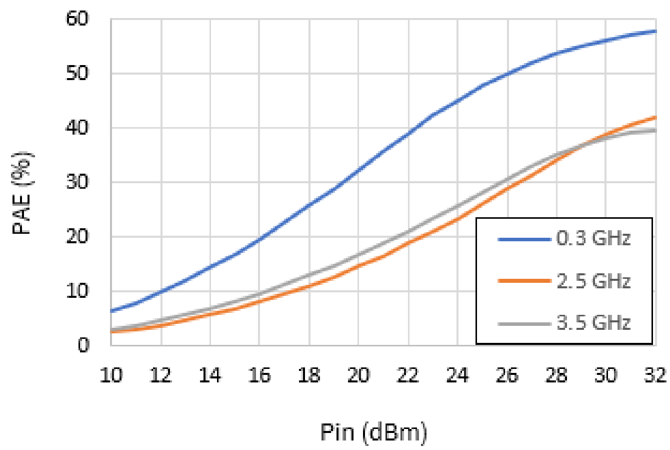
Typical Performance Curves - Drive-Up over Frequency:

V_D = 50 V, I_{DQ} = 500 mA, CW, T_C = 25 °C

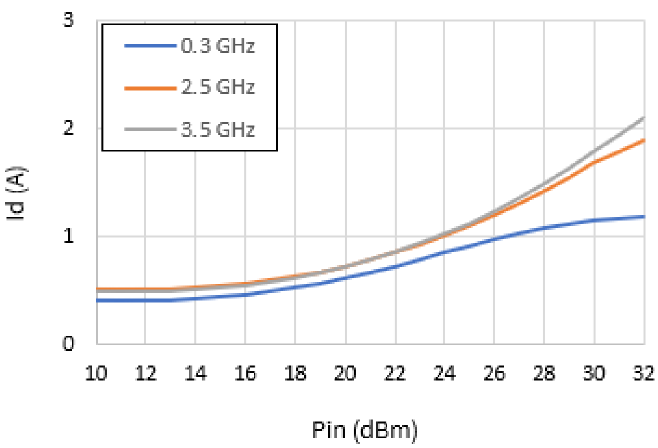
Pout vs. Input Power



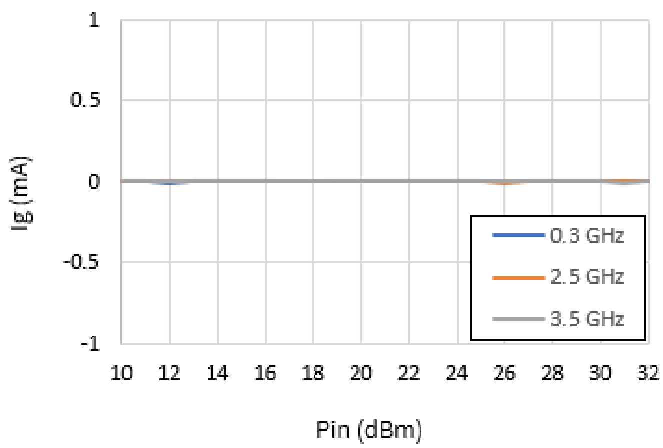
PAE vs. Input Power



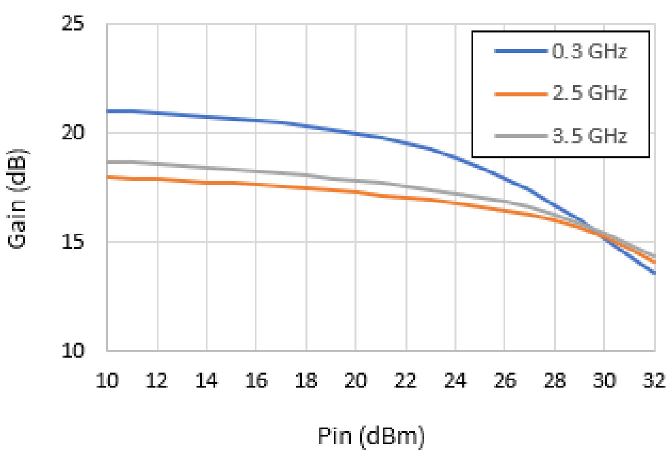
Drain Current vs. Input Power



Gate Current vs. Input Power



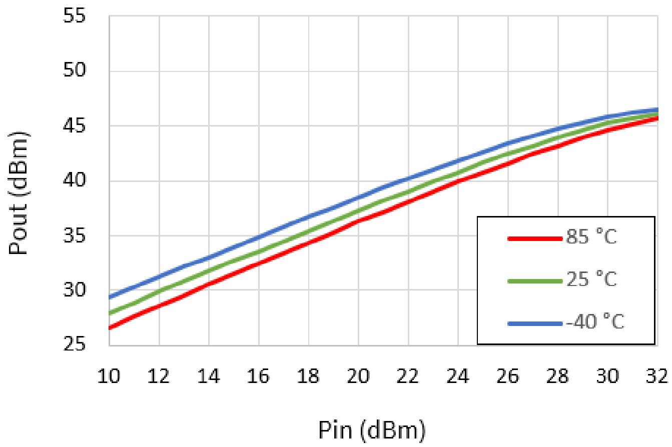
Gain vs. Input Power



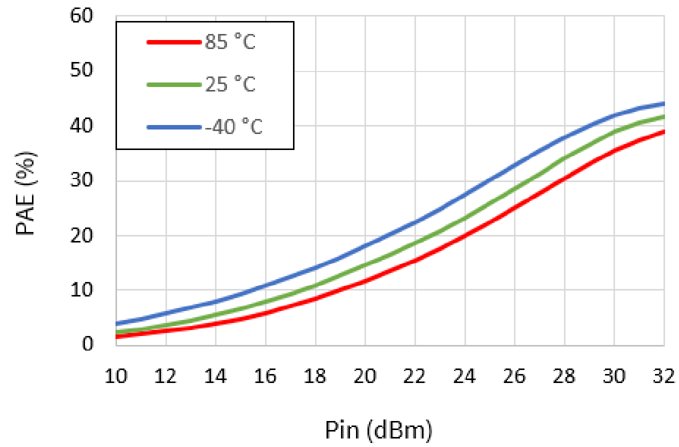
Typical Performance Curves - Drive-Up over Temperature:

V_D = 50 V, I_{DQ} = 500 mA, CW, Frequency = 2.5GHz

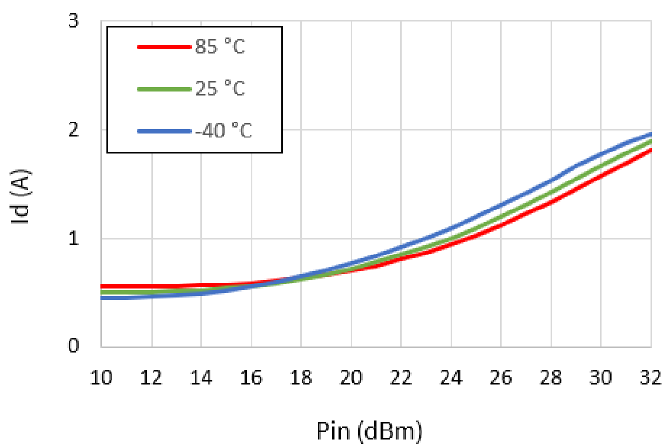
Pout vs. Input Power



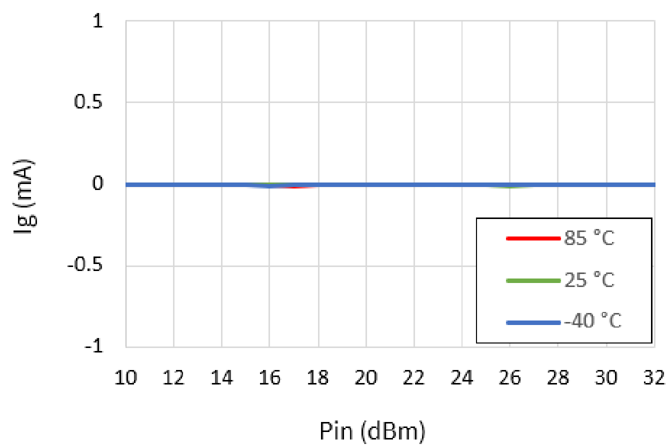
PAE vs. Input Power



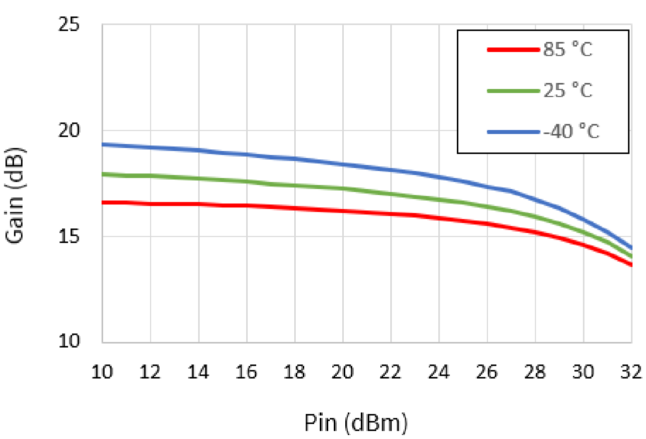
Drain Current vs. Input Power



Gate Current vs. Input Power



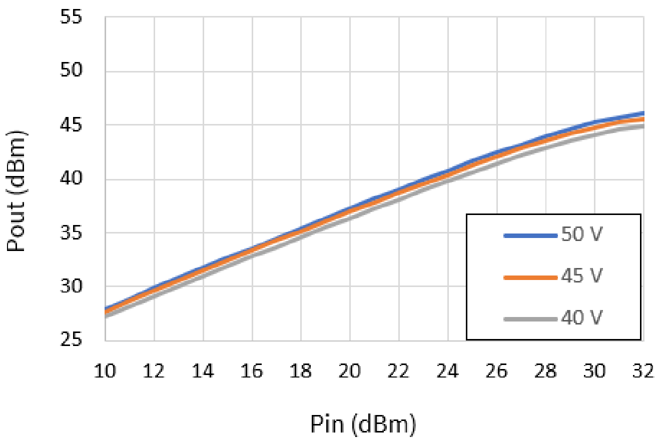
Gain vs. Input Power



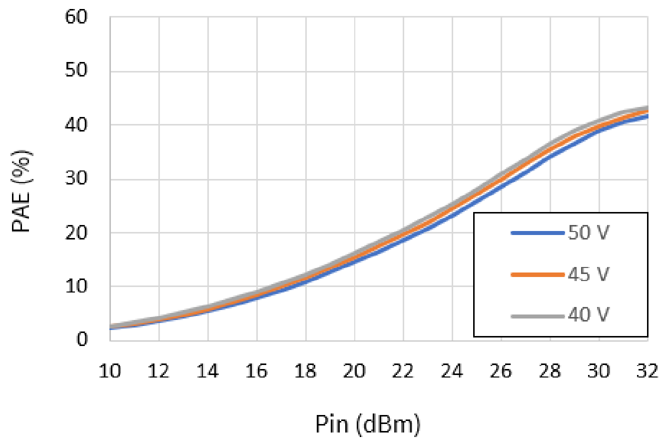
Typical Performance Curves - Drive-Up over V_D:

I_{DQ} = 500 mA, CW, T_C = 25 °C, Frequency = 2.5GHz

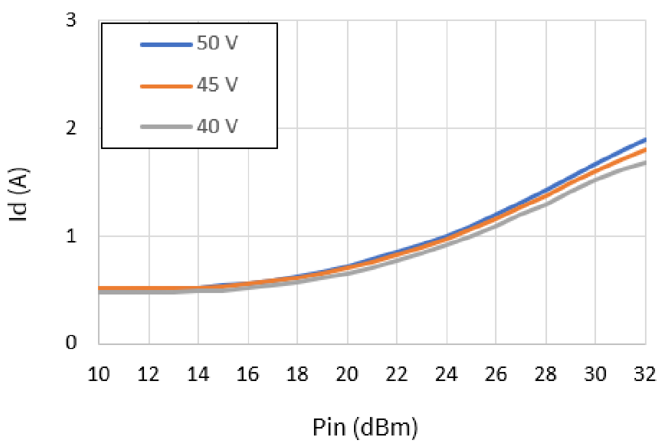
Pout vs. Input Power



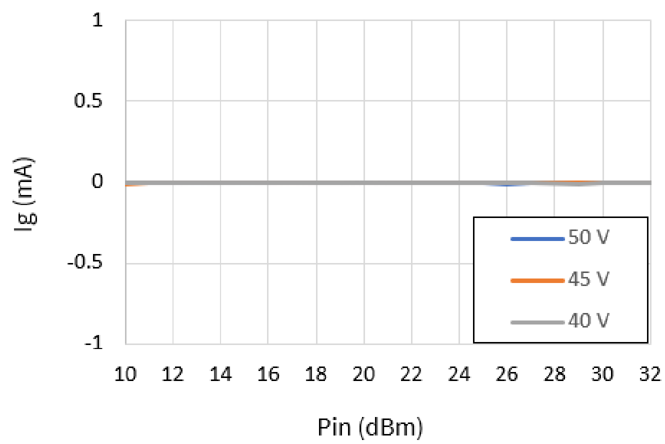
PAE vs. Input Power



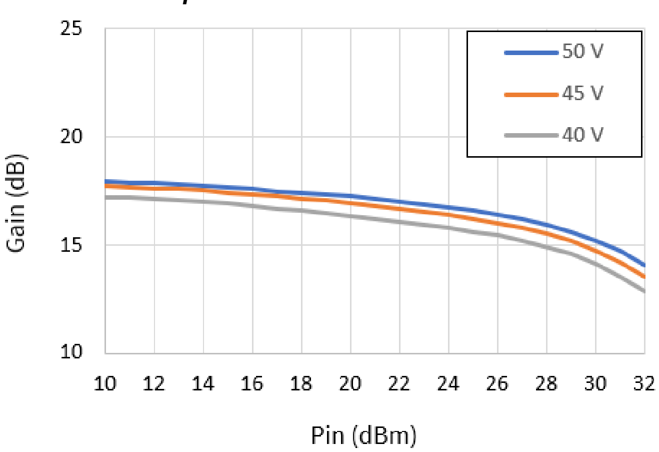
Drain Current vs. Input Power



Gate Current vs. Input Power



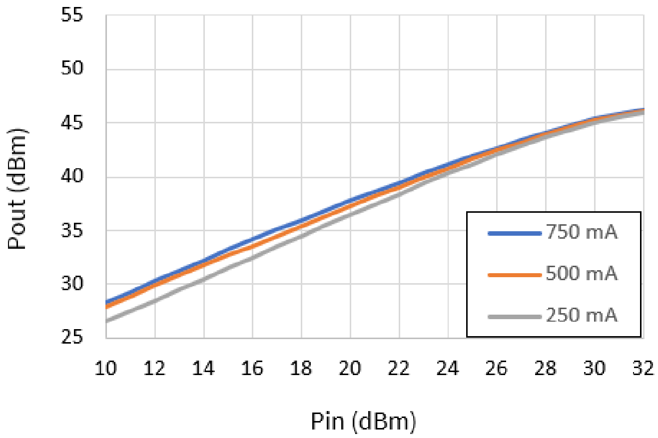
Gain vs. Input Power



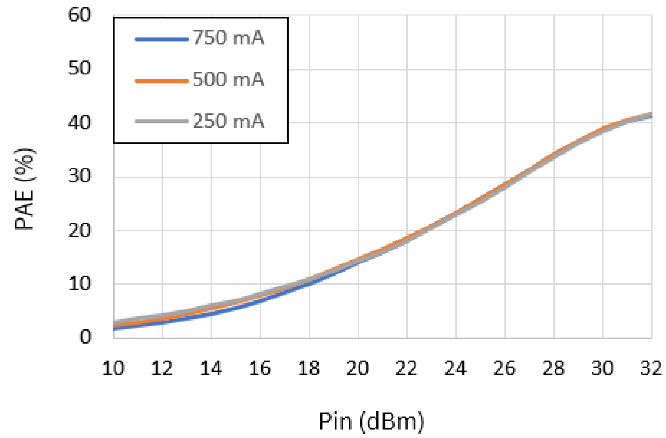
Typical Performance Curves - Drive-Up over I_{DQ}:

V_D = 50 V, CW, T_C = 25 °C, Frequency = 2.5GHz

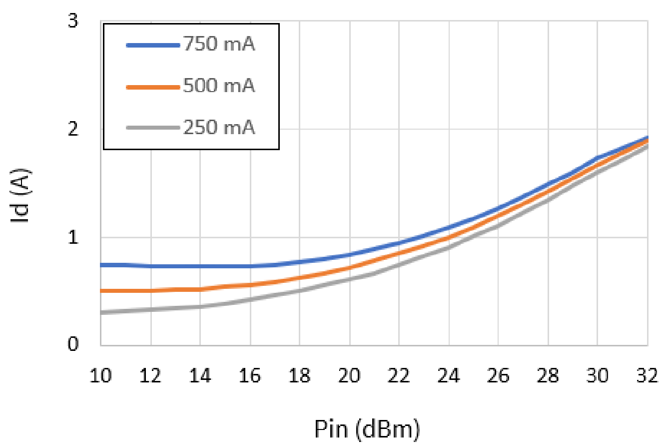
Pout vs. Input Power



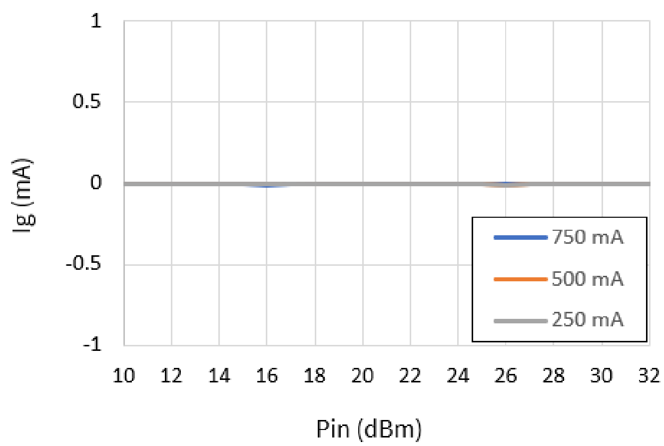
PAE vs. Input Power



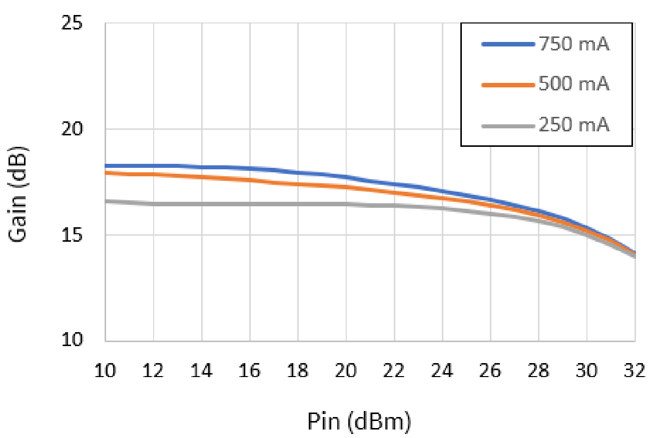
Drain Current vs. Input Power



Gate Current vs. Input Power



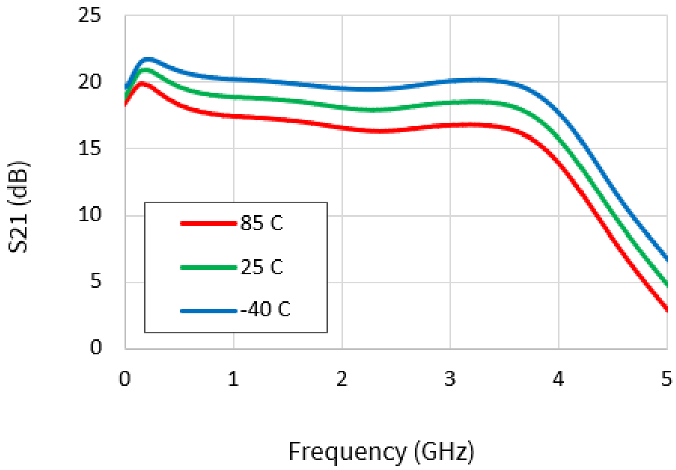
Large Signal Gain vs. Input Power



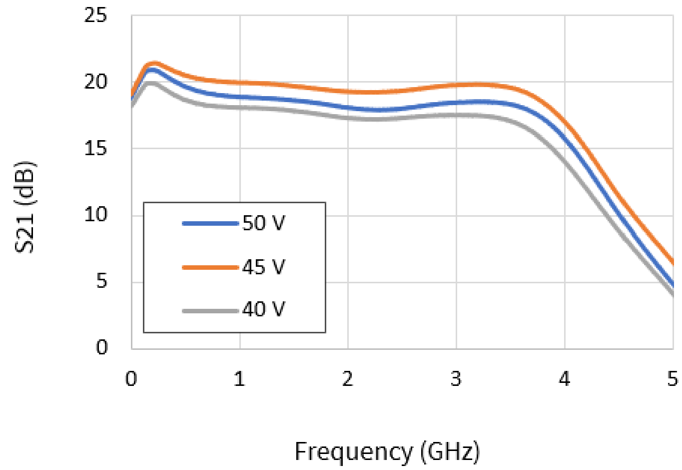
Typical Performance Curves - Small Signal vs. Temperature and V_D:

I_{DQ} = 500 mA, CW, P_{IN} = -20 dBm,

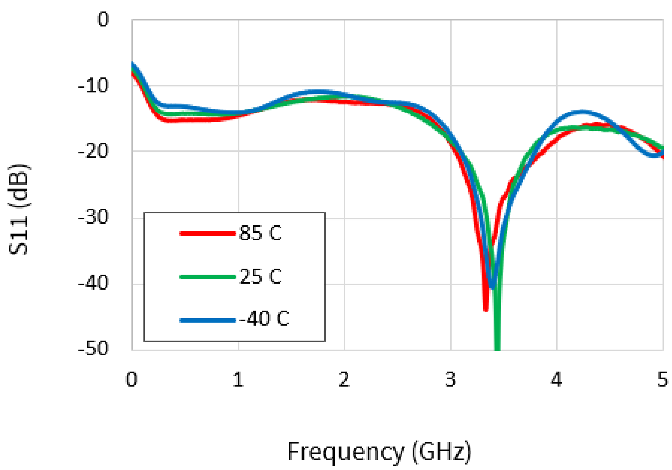
S21 vs. Frequency over Temperature @ V_D = 50 V



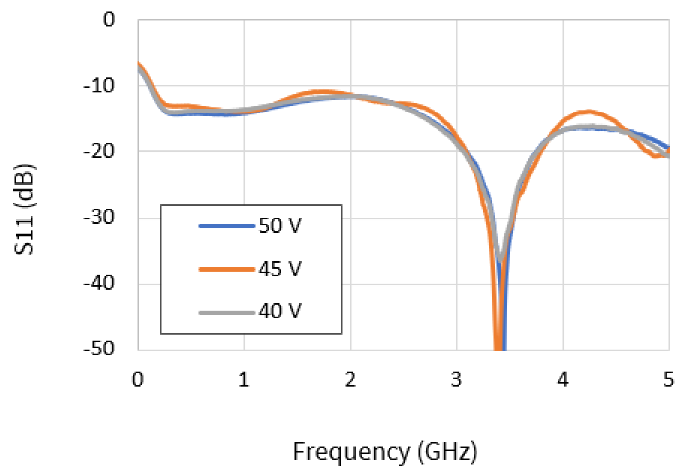
S21 vs. Frequency over V_D @ 25°C



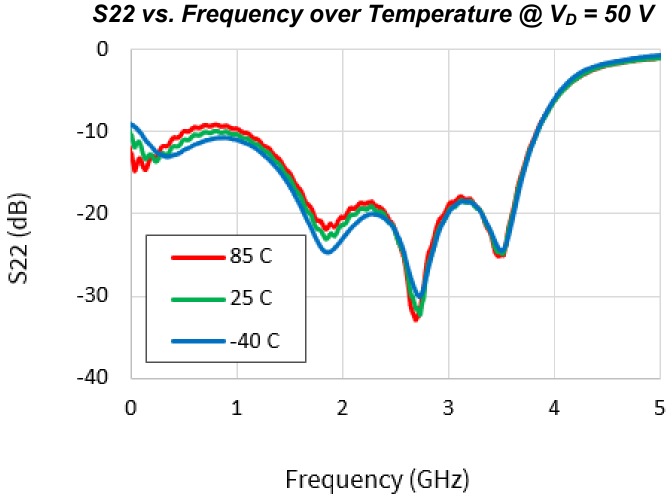
S11 vs. Frequency over Temperature @ V_D = 50 V



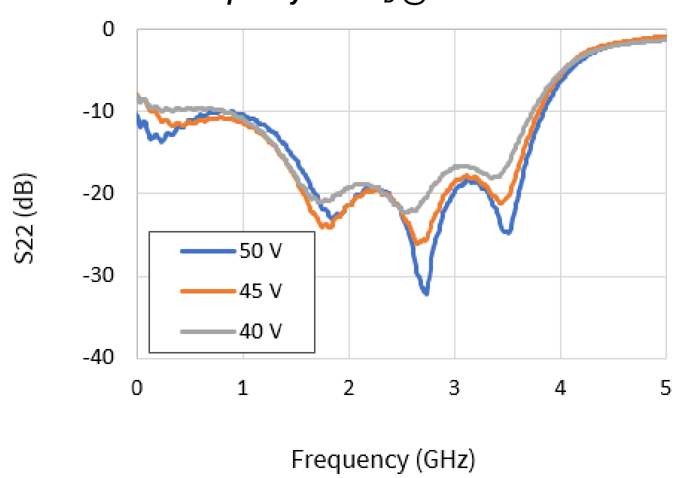
S11 vs. Frequency over V_D @ 25°C



S22 vs. Frequency over Temperature @ V_D = 50 V



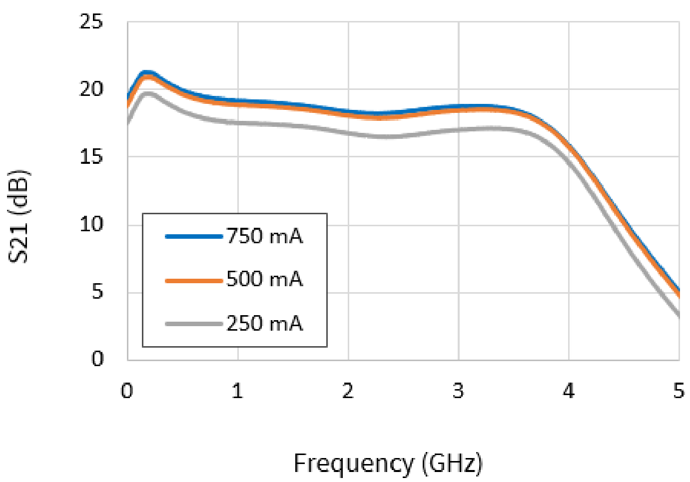
S22 vs. Frequency over V_D @ 25°C



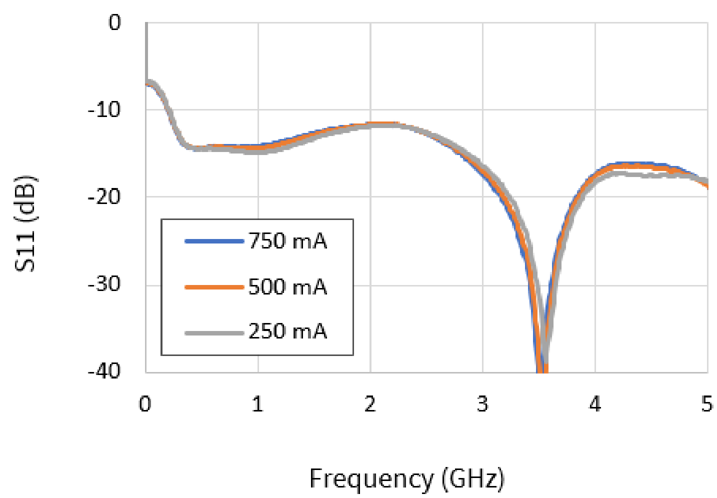
Typical Performance Curves - Small Signal vs. I_{DQ}:

V_D = 50 V, CW, P_{IN} = -20 dBm, T_C = 25 °C

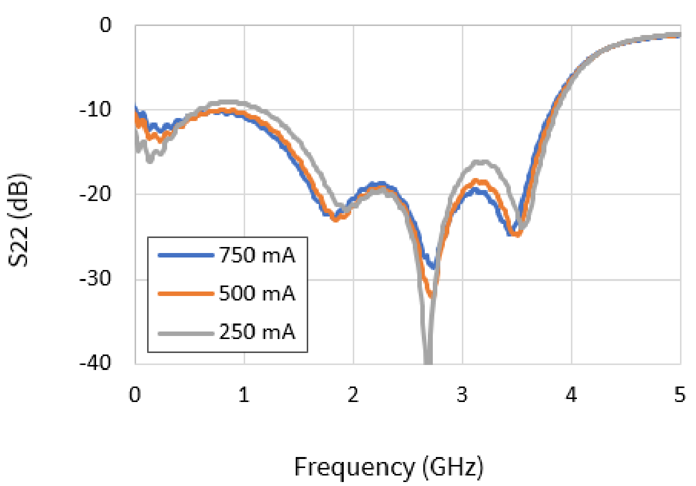
S21 vs. Frequency over I_{DQ}



S11 vs. Frequency over I_{DQ}



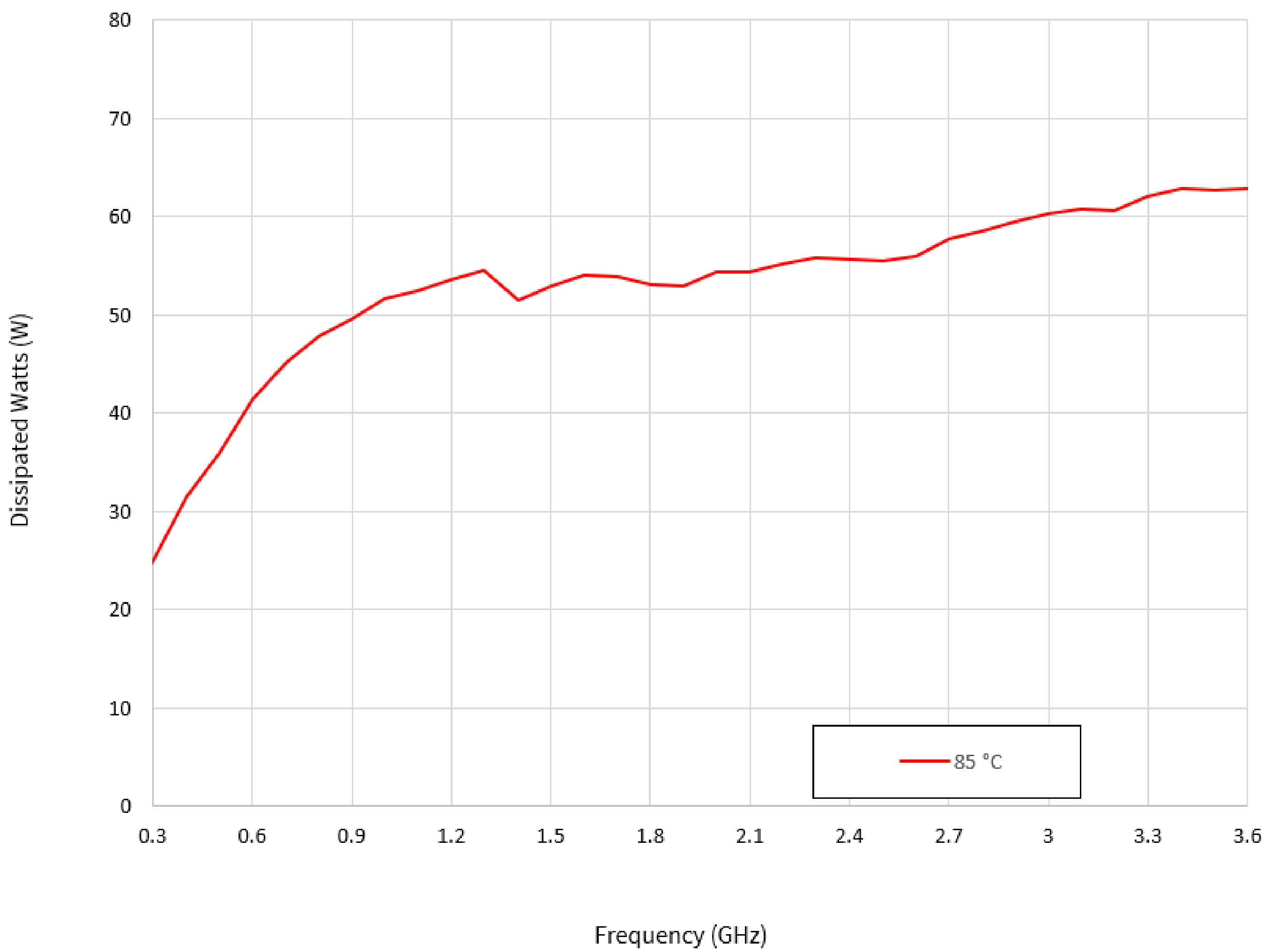
S22 vs. Frequency over I_{DQ}



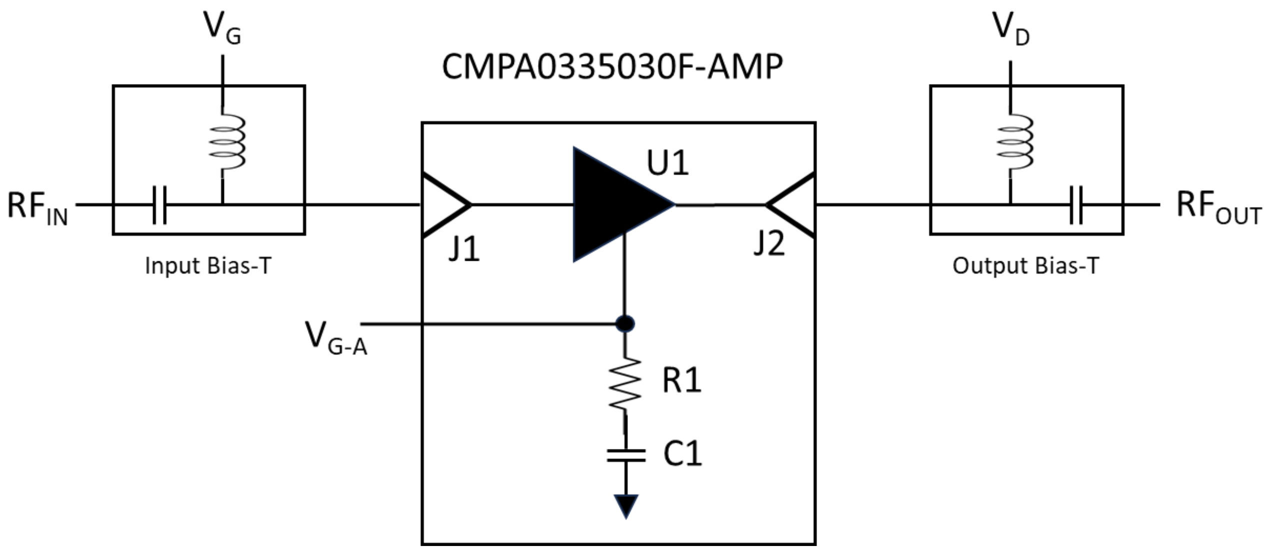
Thermal Characteristics

Parameter	Operating Conditions	Value
Operating Junction Temperature (T_J)	Freq = 2.5 GHz, V_D = 50 V, I_{DQ} = 500 mA, I_{DRIVE} = 1.8 A, P_{IN} = 32 dBm, P_{OUT} = 45.67 dBm, P_{DISS} = 55.5 W, T_{CASE} = 85°C, CW	206.4ºC
Thermal Resistance, Junction to Case ($R_{\theta JC}$)		2.187

Power Dissipation vs. Frequency (T_C = 85°C)



Evaluation Board Schematic (CMPA0335030F-AMP)

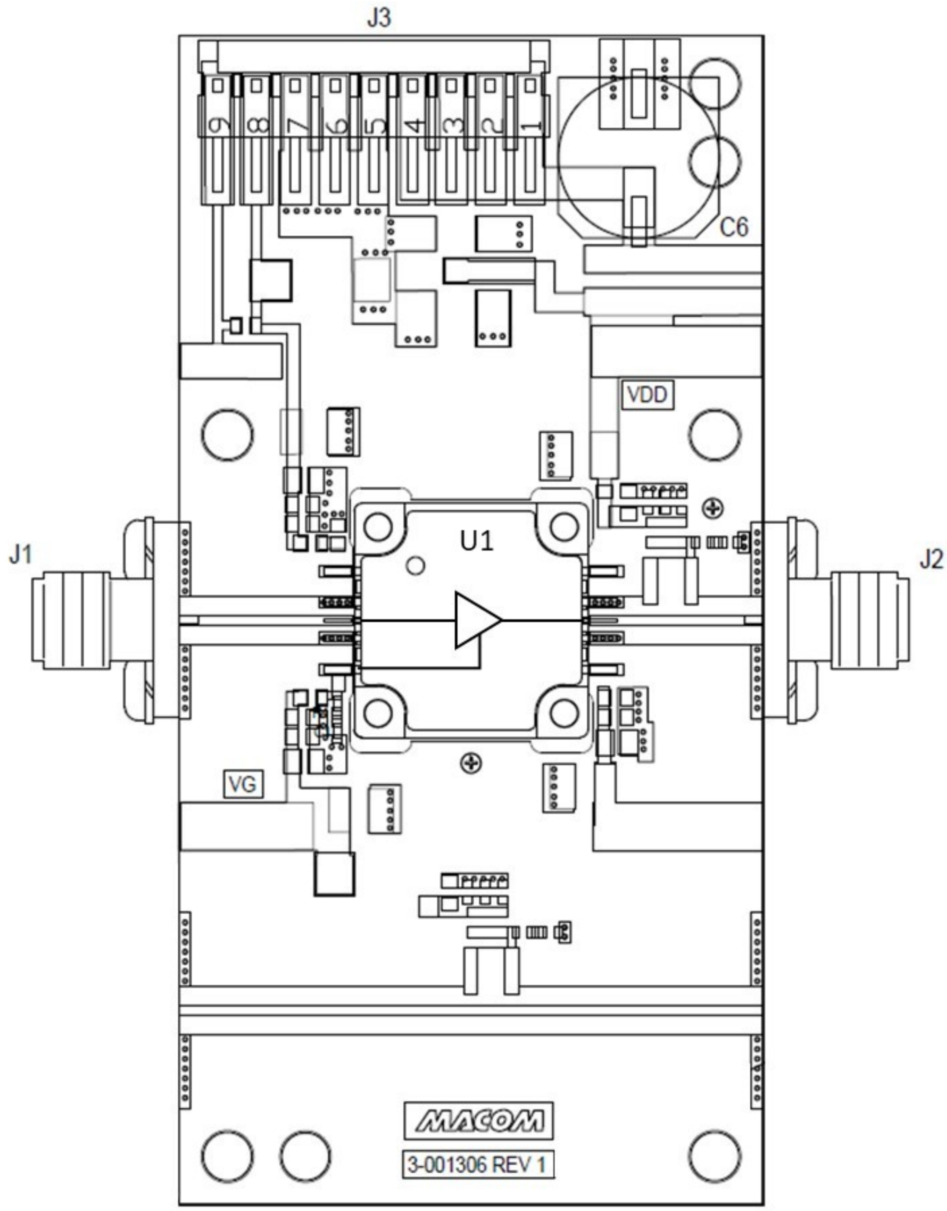


Notes:
1. Input and output bias-T's are used to provide DC and RF power to the amplifier. All data herein is taken using external bias-T's.
2. VG-A is an alternative pin that can be used to provide gate bias to the amplifier. If not used, this pin should be treated as a NC (No Connect).
3. Note, for VG-A to be used on the MACOM eval board, a 0-ohm resistor must bridge the open to the left of R1. External gate bias will need to connect to the trace labeled VG. A blocking cap will also need to be added on the RF input line if the VG-A bias approach is used.

Parts List

Part	Value	Qty.
	BASEPLATE, CU, 3.0 X 1.5 X 0.25 IN	1
	EPOXY, ABLESTICK, CF 3350-004, 3x1.5	1
	PCB 3.0" x 1.5" x 0.010" (RO3003, DK 3.0), TEST FIXTURE CMPA0335030F	1
R1	RES 100 Ohm,1/16W, 1%, 0402	1
C1	CAP, 100 pF, 100V, 0402, KEMET	1
J1, J2	CONN, SMA, PANEL MOUNT JACK, FLANGE, 4-HOLE, BLUNT POST, 20MIL	2
	2-56 SOC HD SCREW 3/16 SS	4
	#2 SPLIT LOCKWASHER SS	4
U1	CMPA0335030F	1

Evaluation Board Assembly Drawing (CMPA0335030F-AMP)



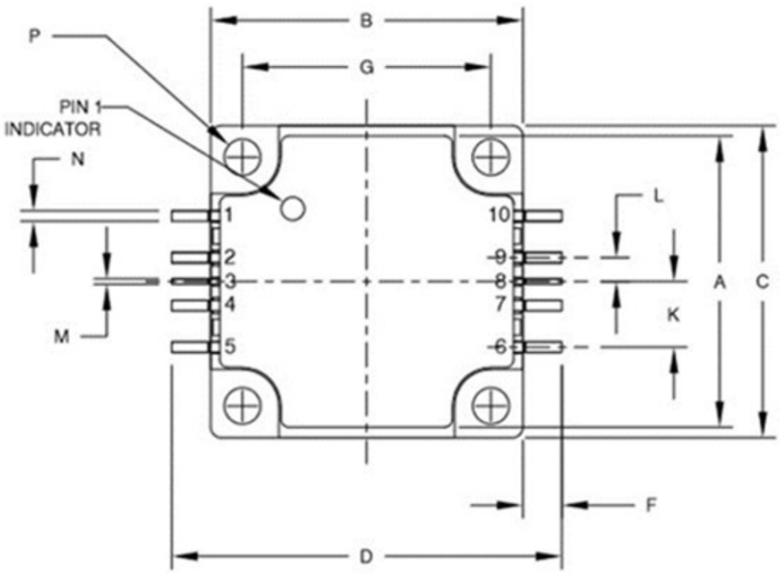
Bias On Sequence

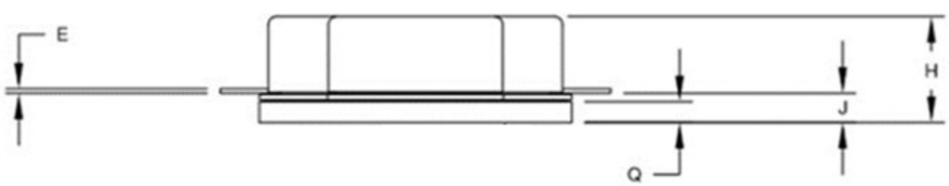
1. Ensure RF is turned-off
2. Apply pinch-off voltage of -5 V to the gate (V_G)
3. Apply nominal drain voltage (V_D)
4. Adjust Vg to obtain desired quiescent drain current (I_{DQ})
5. Apply RF

Bias Off Sequence

1. Turn RF off
2. Apply pinch-off to the gate (V_G = -5 V)
3. Turn off drain voltage (V_D)
4. Turn off gate voltage (V_G)

Mechanical Information

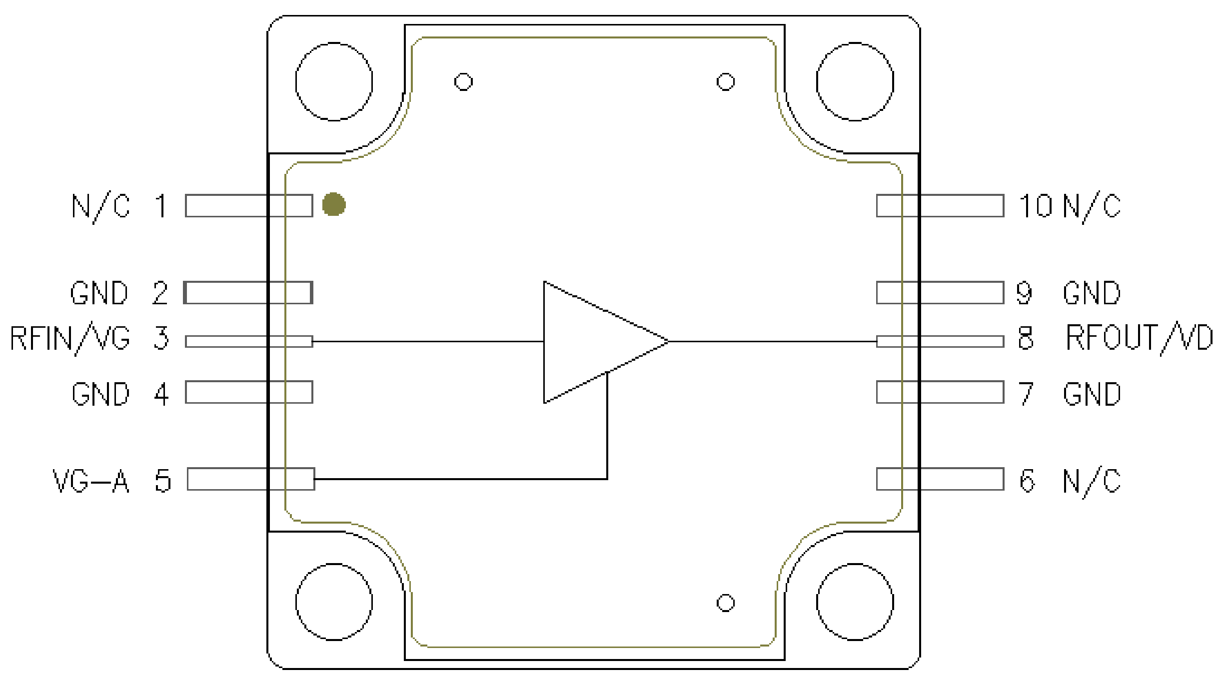




DIM	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	.555	.560	.565	14.10	14.22	14.35
B	.595	.600	.605	15.11	15.24	15.37
C	.595	.600	.605	15.11	15.24	15.37
D	-	(.750)	-	-	(19.05)	-
E	.006	.008	.010	0.15	0.20	0.25
F	.065	.075	.085	1.66	1.91	2.16
G	.473	.478	.483	12.01	12.14	12.27
H	.191	.203	.215	4.86	5.16	5.46
J	.049	.056	.063	1.24	1.42	1.60
K	.121	.126	.131	3.07	3.20	3.33
L	.041	.046	.051	1.04	1.17	1.30
M	.005	.010	.015	0.13	.25	0.38
N	.015	.020	.025	0.38	.51	0.63
P	.065	.070	.075	1.65	1.78	1.90
Q	.038	.040	.042	0.97	1.02	1.07

Pin Description

Pin #	Name	Description
1	NC	Should solder to PCB ground to prevent mechanical damage.
2	GND	RF and DC ground.
3	RF Input/VG	Not internally DC blocked (DC-coupled). VGS only if using an external bias-T. Otherwise use pin 5.
4	GND	RF and DC ground.
5	VG-A / NC	Can be used as an alternative to gate biasing through a bias-T. Reference application circuit and notes (p.14).
6	NC	Should solder to PCB ground to prevent mechanical damage.
7	GND	RF and DC ground.
8	RF Output/VD	Not internally DC blocked (DC-coupled). Requires external bias-T.
9	GND	RF and DC ground.
10	NC	Should solder to PCB ground to prevent mechanical damage.
Paddle	GND	RF and DC ground.



Revision History

Rev	Date	Change Description
V1P	09/13/2024	Initial preliminary release.
V1	03/11/2025	Production release with specification limits, ESD results.