# Low Noise Amplifier
# 44 - 69 GHz

**CGY2272UH**
**Rev. V1**

## Features

- Gain: 29 dB
- Noise Figure: <1.7 dB
- ROBUSTMax 1.5 dBm in CW Input Power
- Single Positive & Negative Supply
  - $V_{DD}$ = 1.5 V
  - $V_{SS}$ = 1.5 V
  - $I_{DD}$ = 46 mA
- 50 Ω Input & Output Matched
- Chip Size: 2.35 x 1.2 mm
- Tested, Inspected Known Good Die (KGD)
- Space and MIL-STD MMICs
- RoHS* Compliant

## Applications

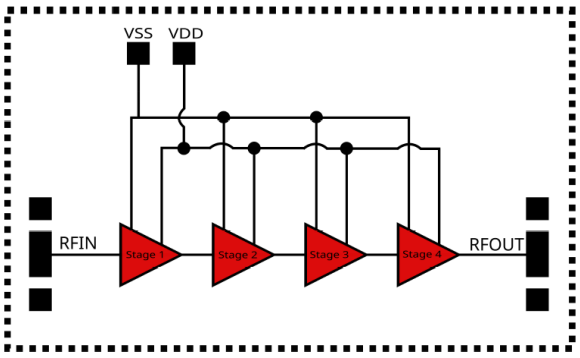
- Radar
- Telecommunication
- Instrumentation
- Space

## Description

The CGY2272UH is a high-performance GaAs low noise amplifier MMIC designed to operate in the V-Band.

The die is manufactured using an advanced 70 nm gate length high indium contains mHEMT technology (D007IH). The MMIC uses gold bonding pads and backside metallization and is fully protected with silicon nitride passivation to obtain the highest level of reliability.

## Block Diagram




## Ordering Information

| Part Number | Package |
|---|---|
| CGY2272UH | die |



* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

## Electrical Specifications: Measured On Wafer, Freq. = 44 - 69 GHz, $V_{DD}$ = 1.5 V, $I_{DD}$ = 46 mA, $T_A$ = +25°C

| Parameter | Test Conditions | Units | Min. | Typ. | Max. |
|---|---|---|---|---|---|
| Gain | — | dB | 26 | 29 | 31 |
| Reverse Isolation | — | dB | -50 | -32 | — |
| Noise Figure | — | dB | — | — | 1.7 |
| Input Return Loss | 50 Ω | dB | — | 8 | — |
| Output Return Loss | 50 Ω | dB | — | 8 | — |
| P1dB | — | dBm | — | 8 | — |

## Absolute Maximum Ratings[1,2]

| Parameter | Absolute Maximum |
|---|---|
| Input Power<br>CW during 1 min. | 15 dBm |
| Voltage:<br>Drain<br>Negative | <br>2 V<br>-2 - 0.6 V |
| Current:<br>Drain<br>Negative | <br>90 mA<br>5 mA |
| Junction Temperature | +150°C |
| Operating Temperature | -40°C to +85°C |
| Storage Temperature | -55°C to +150°C |
| Mounting Temperature | +300°C, 60 seconds |

1. Exceeding any one or combination of these limits may cause permanent damage to this device.
2. MACOM does not recommend sustained operation near these survivability limits.

## Thermal Characteristics

| Parameter | Absolute Maximum |
|---|---|
| Thermal Resistance | 454°C/W @ 20°C<br>548°C/W @ 85°C |

## Bias Up Procedure

1. Set $I_{DD}$ to 100 mA, $I_{SS}$ limit to 10 mA
2. Apply -1.5 V to $V_{SS}$
3. Apply +1.5 V to $V_{DD}$, ensure $I_{DD}$ is approximately 0 mA
4. Adjust $V_{SS}$ until $I_{DD}$ = 46 mA
5. Turn on RF supply

## Bias Down Procedure

1. Turn off RF supply
2. Reduce $V_{SS}$ to -1.5 V
3. Set $V_{DD}$ to 0 V
4. Turn off $V_{DD}$ supply
5. Turn off $V_{SS}$ supply

## Handling Procedures

Please observe the following precautions to avoid damage:

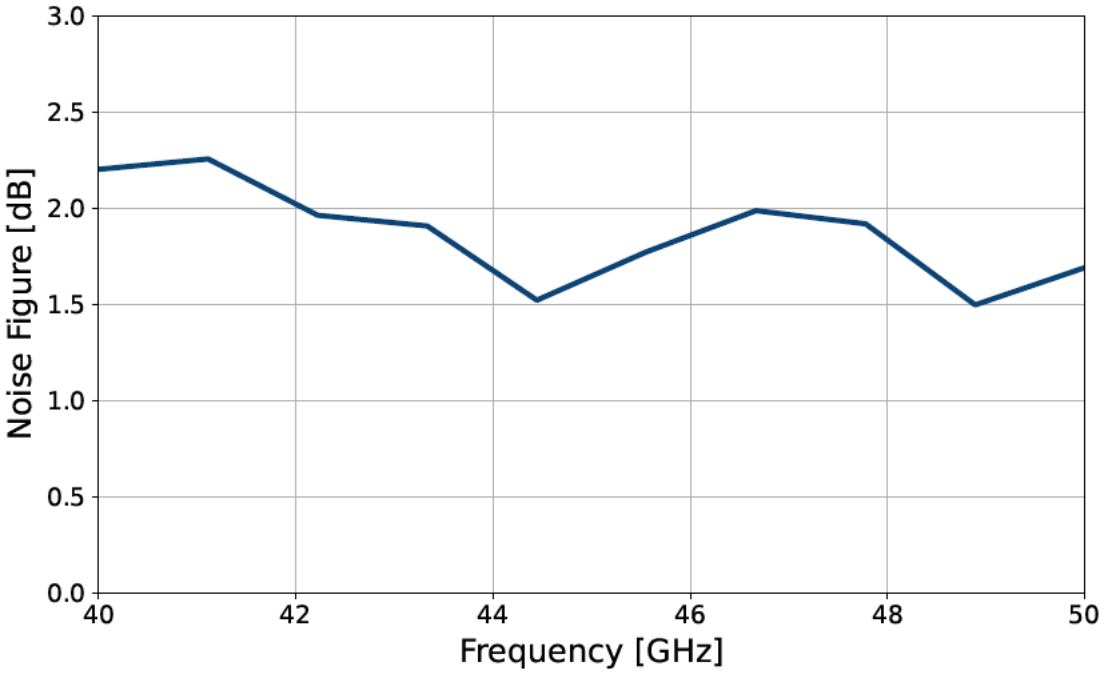
## Static Sensitivity

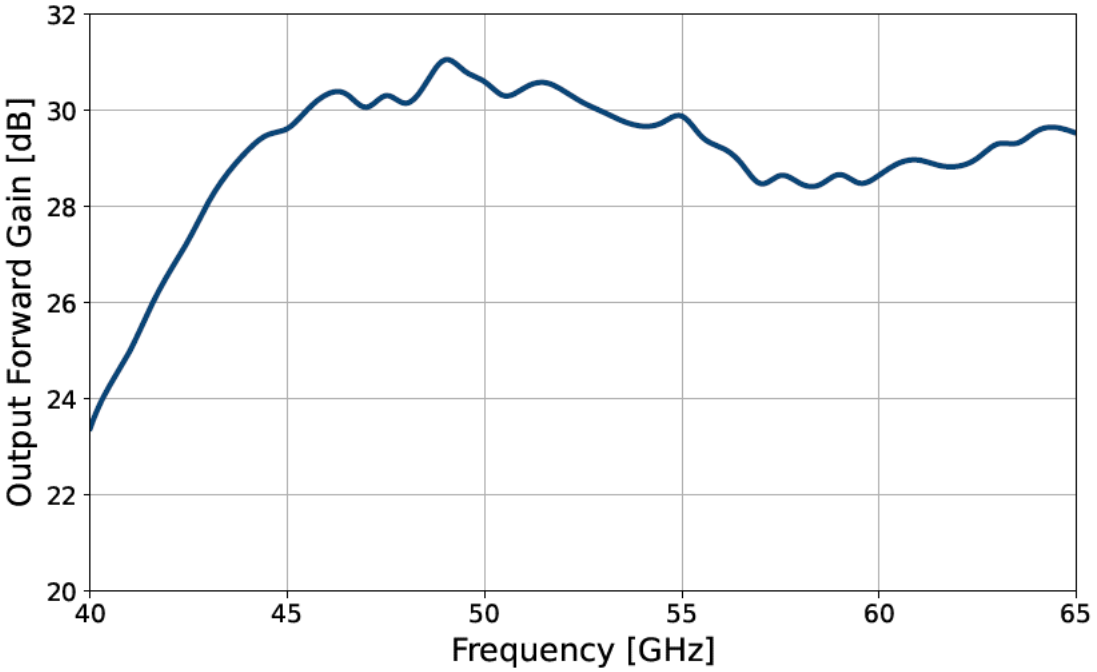
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

On wafer measurements with a CW test bench to assure a full polarization conditions and cold channel temperature.

This method also removes the risk of reliability damages due to high temperature overstress inherent to on wafer measurements at full polarization and reflects the performances of the devices in good cooling conditions.
$V_{DD}$ = 1.5 V / $I_{DD}$ = 46 mA, $T_A$ = +25°C

## Typical Performance Curves: On Wafer Measurements



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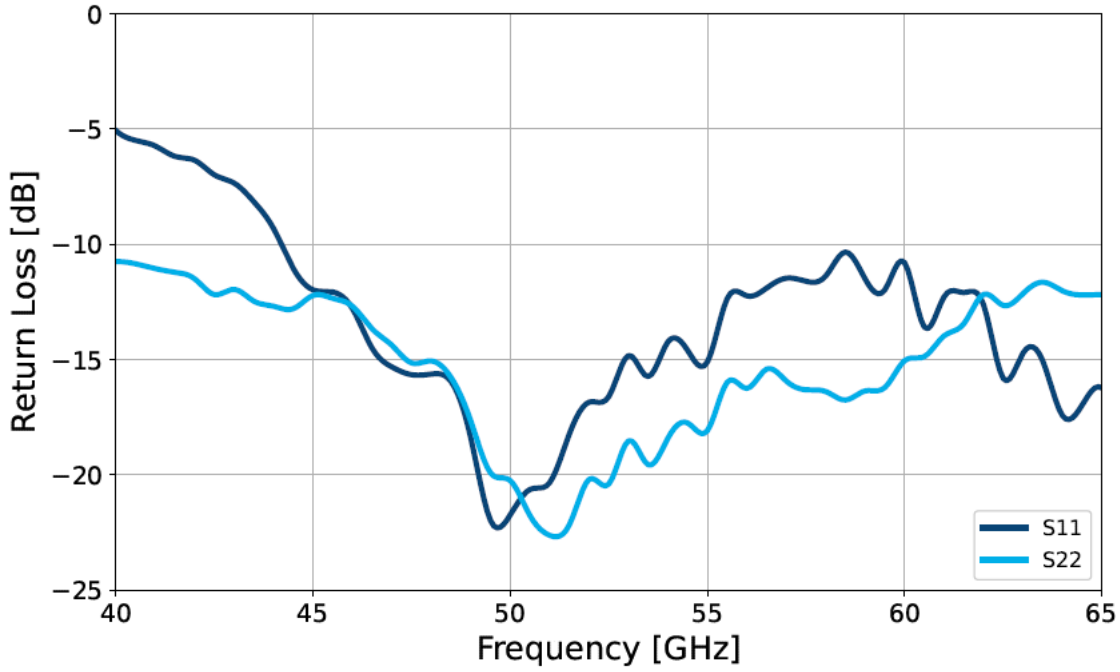
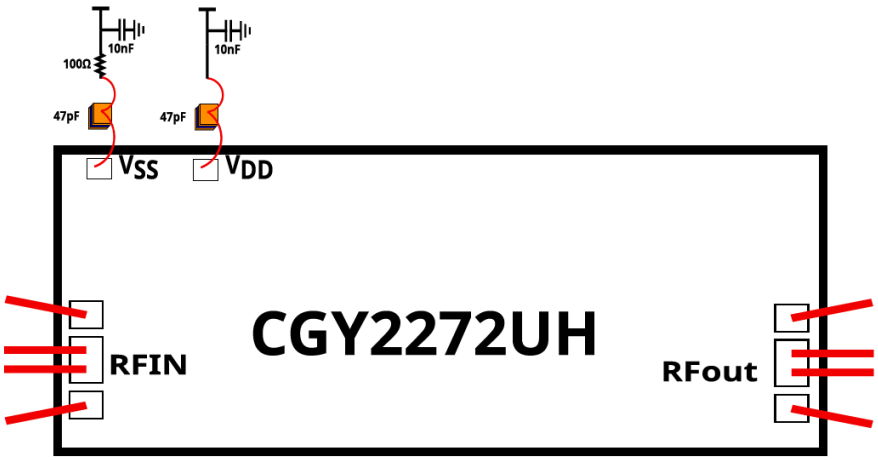


## Application Schematic

The decoupling network depends on supply, on grounding environment, on form factor, on all parasitics added by the customer environment. According to this, the appropriate network sometimes need to be fine-tuned in accordance with rules applicable in the high frequency domain.

Decoupling scheme depends on customer implementation, in order to prevent instability it is highly recommended to place a 47pF RF decoupling chip capacitor at each DC terminal with the shortest possible bonding wires. Additionally, a 10nF CMS capacitor can be added on the drain connection.

In the source 10 Ω / 100 nF RC series network may be added in series to improve source isolation and prevent unwanted oscillations. The resistors are introducing some low pass filtering in case of fast power switching using source control architecture.

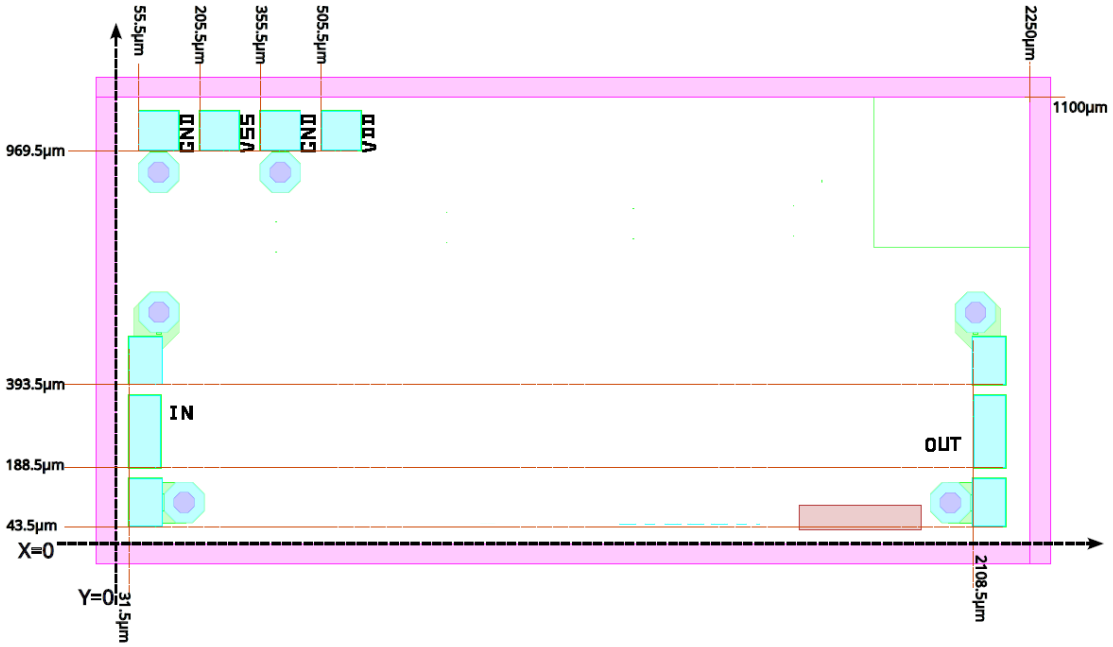



| Component Name | Value | Type | Comment |
|---|---|---|---|
| Capacitor | 47 pF | Chip | Chip capacitor PRESIDIO COMPONENTS P/N SA151BX470M2HX5 # 013B soldered close to the die with bonding as short as possible |
| Capacitor | 10 nF | CMS | Chip resistor US MICROWAVES RG1421-100-1 % soldered close to the 47 pF chip capacitor with bonding as short as possible |
| Resistor | 100 Ω | CMS | MURATA GMA085R71C103MD01T GM260 X7R 103M 16M100 PM520 |

## Die Layout

The Die is symmetrical on the RF axis. The die positioned top view with RF input on the left and RF output on the right show DC accesses on the top labelled south. VDD, VSS, are DC signals applied. Many ground accesses are complementing the pad layout. The backside is the ground reference plan.

Note: (0,0) have been taken on the bottom right corner of the MMIC without dicing street.



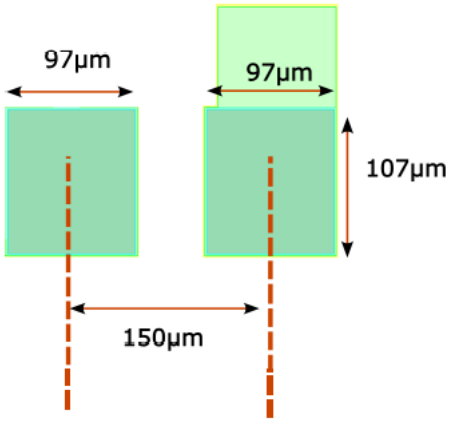

## Bonding Pad Coordinates & Description

| Pad | X Coordinate | Y Coordinate | Pad Size | Description |
|---|---|---|---|---|
| GND | 81.5 | 93.5 | 81 x 117 | Associated with RFIN pad |
| RFIN | 81.5 | 238.5 | 81 x 177 | RFIN pad |
| GND | 81.5 | 433.5 | 81 x 117 | Associated with RFIN pad |
| GND | 105.5 | 1019.5 | 97 x 97 | Ground |
| VSS | 255.5 | 1019.5 | 97 x 97 | Negative supply voltage |
| GND | 405.5 | 1019.5 | 97 x 97 | Ground |
| VDD | 555.5 | 1019.5 | 97 x 97 | Drain supply voltage |
| GND | 2158.5 | 93.5 | 81 x 117 | Associated with RFOUT pad |
| RFOUT | 2158.5 | 238.5 | 81 x 177 | RFOUT pad |
| GND | 2158.5 | 433.5 | 81 x 117 | Associated with RFOUT pad |

In order to ensure good RF performances and stability, it is key to connect to the ground the pad available on the backside of the die.

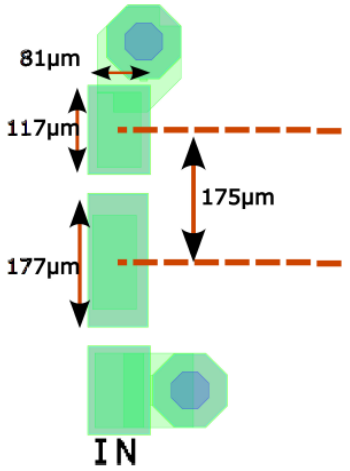
(0,0) have been taken on the bottom right corner of the MMIC with dicing street.

## DC Pad Dimension

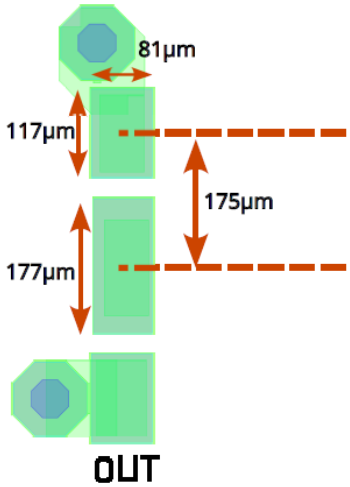



The same size is used of each DC pad (VD,VS) to bias the transistors. It is 97 x 97 µm

## RF Pad Dimension




The size is used of Input RF pad of the Low Noise Amplifier. It is 81 x 177 µm

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