

Phase Shifter, C-Band, 6-Bit 4.8 - 6.8 GHz



CGY2177AUH/C1

Rev. V1

Features

- Insertion Loss: 5 dB @ 5.4 GHz
- Phase Shift Range: 360°
- RMS Phase Error: 2° @ 5.4 GHz
- RMS Amplitude Variation: 0.25 dB @ 5.4 GHz
- Input P1dB: 20 dBm
- Return Loss: 15 dB @ 5.4 GHz (All states)
- 0 / 5 V Control Lines
- Chip Size: 3470 x 2220 μm
- Tested, Inspected Known Good Die (KGD)
- Samples Available
- Demonstration Boards Available
- Space and MIL-STD Available
- RoHS* Compliant

Applications

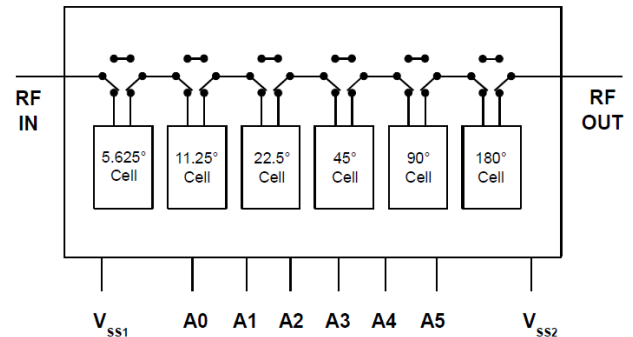
- Radar
- Telecommunication
- Instrumentation

Description

The CGY2177AUH/C1 is a high performance GaAs MMIC 6-bit phase shifter operating in C-band. It has a nominal phase shifting range of 0 - 360° in 5.625° steps and uses an optimum combination of switched line and high pass/low pass filters to obtain very low phase error and insertion loss variation. It covers the frequency range of 4.5 to 6.5 GHz.

This die is manufactured using 0.18 μm gate length pHEMT technology. The MMIC uses gold bond pads and backside metallization and is fully protected with Silicon Nitride passivation to obtain the highest level of reliability. This technology has been evaluated for Space applications and is on the European Preferred Parts List of the European Space Agency.

Block Diagram



Ordering Information

Part Number	Package
CGY2177AUH/C1	DIE

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications¹: Freq. = 4.8 - 6.8 GHz, V_{SS2} = -4.5 V, I_{SS2} = 8 mA, T_A = +25°C

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Source Supply Voltage	VS1 pad is open VS2 pad is open	V	-6 -5	-4.5 -3.5	-4 -3
Source Supply Current	—	mA	—	8	—
Insertion Loss	@ Reference State	dB	—	5	—
Phase Range	—	°	—	360	—
RMS Phase Error	5.0 - 6.5 GHz	°	—	2	—
RMS Attenuation Error	5.0 - 6.5 GHz	dB	—	0.25	—
Input Return Loss	50 Ω Source, All States	dB	—	15	—
Output Return Loss	50 Ω Load, All States	dB	—	15	—
P1dB	—	dBm	—	20	—

1. The RMS value is the root mean square of the error defined as below:
Where xi is the difference between the measured value and the expected value.

$$x_{\text{rms}} = \sqrt{\frac{1}{N} \sum_{i=1}^N x_i^2} = \sqrt{\frac{x_1^2 + x_2^2 + \dots + x_N^2}{N}}$$

Absolute Maximum Ratings^{2,3}

Parameter	Absolute Maximum
Phase Control Inputs	0 to +6 V
Source Supply Voltage when VS2 pad is not used when VS1 pad is no used	-5 to +0.5 V -6 to +0.5 V
Input Power	25 dBm
Junction Temperature	+150°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +150°C

2. Exceeding any one or combination of these limits may cause permanent damage to this device.
3. MACOM does not recommend sustained operation near these survivability limits.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

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Logic Truth Table

	A0	A1	A2	A3	A4	A5
Nominal Phase Shift	-5.6°	-11.25°	-22.5°	-45°	-90°	-180°
Phase Shift Activated	1	1	1	1	1	1
Reference State	0	0	0	0	0	0

Logic Truth Table (V)

	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Phase Shift (°)	-180°	-90°	-45°	-22.5°	-11.25°	-5.6°
0	0	0	0	0	0	0
-5.6	0	0	0	0	0	1
-11.25	0	0	0	0	1	0
-22.5	0	0	0	1	0	0
-45	0	0	1	0	0	0
-62	0	0	1	0	1	1
-90	0	1	0	0	0	0
-118	0	1	0	1	0	1
-180	1	0	0	0	0	0
-270	1	1	0	0	0	0
-354	1	1	1	1	1	1

Control Voltage

State	Min.	Max.	Unit
Low (0)	0	1	V
High (1)	4	6	V

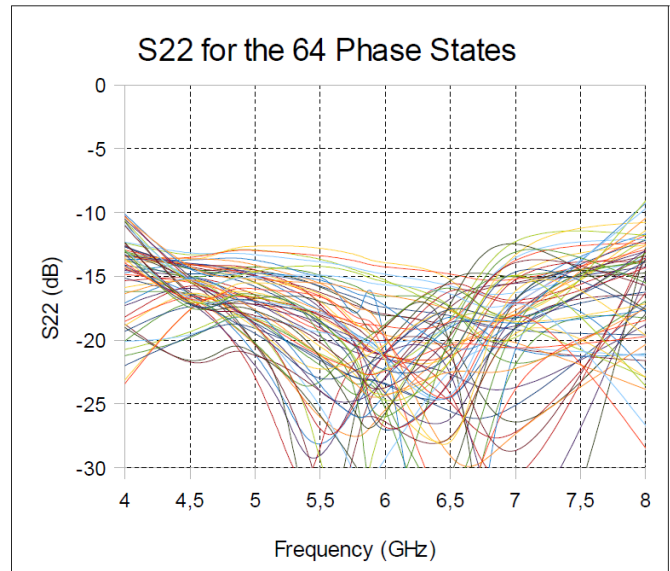
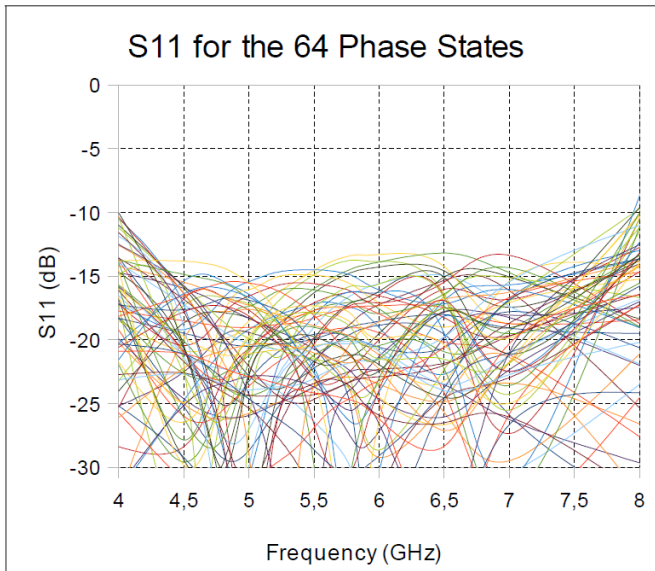
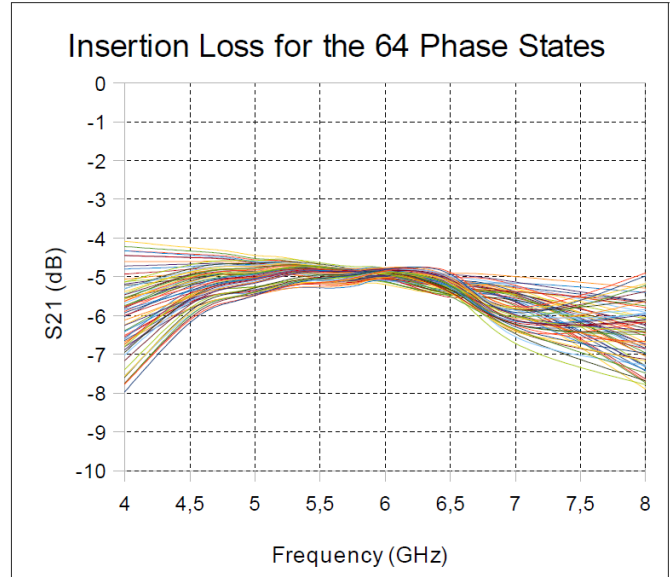
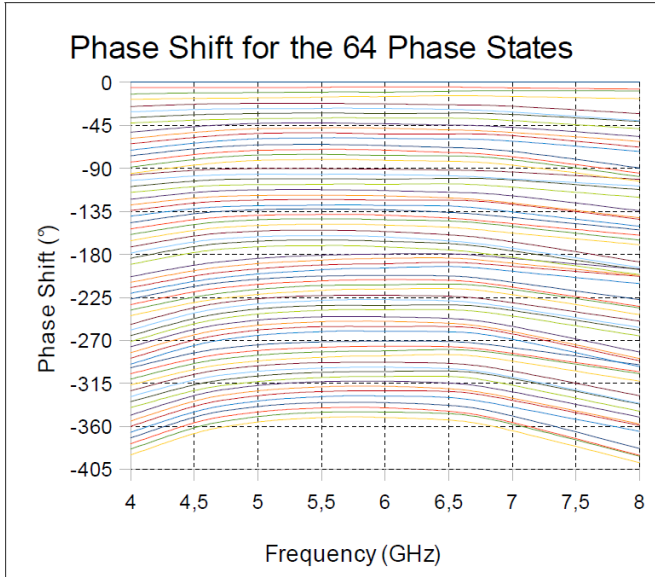
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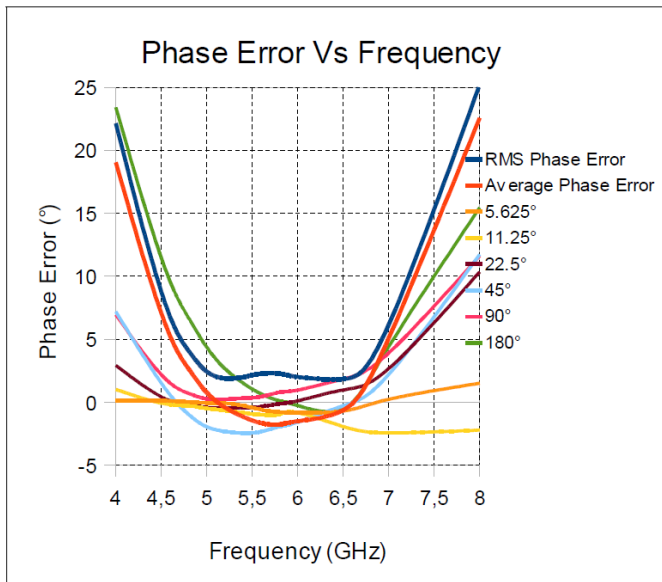
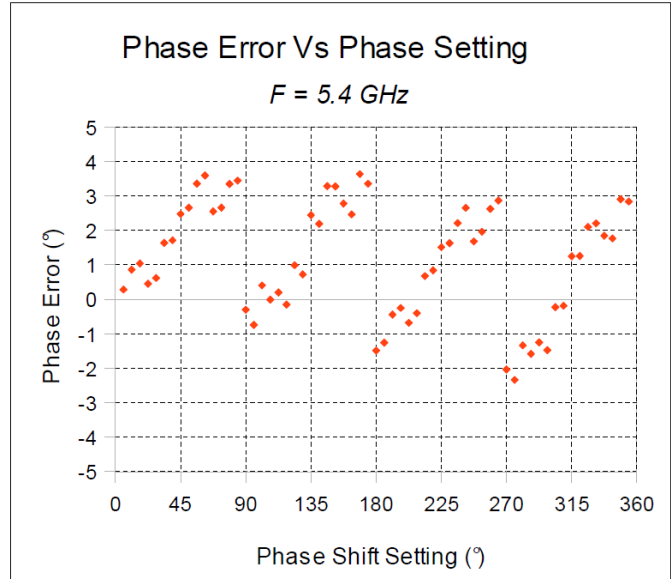
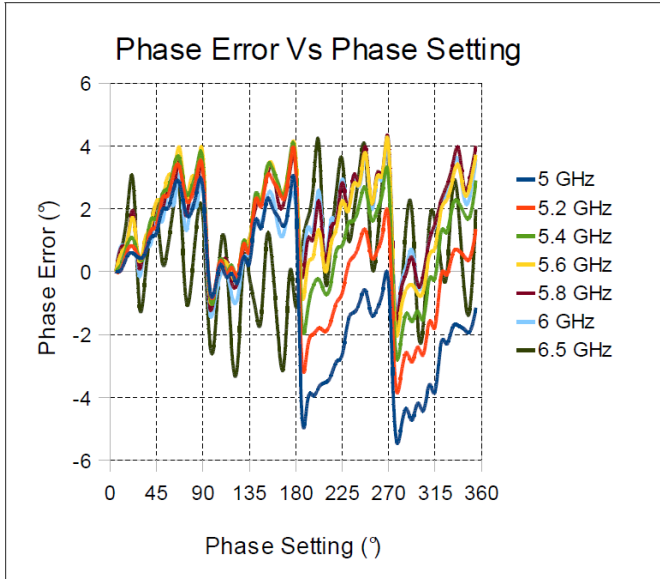
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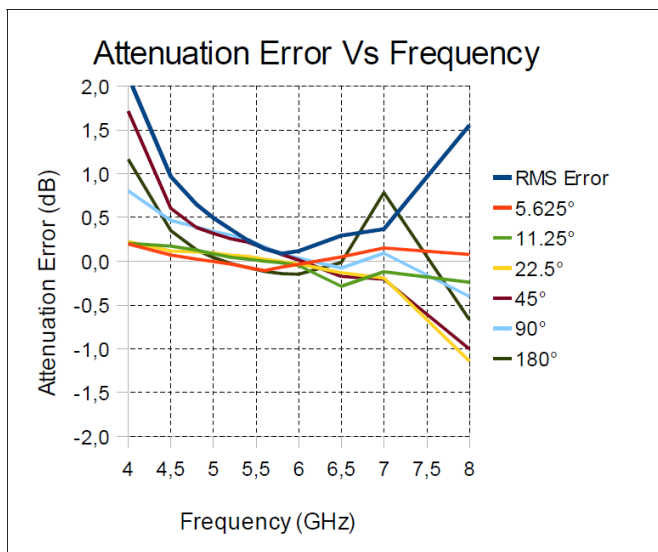
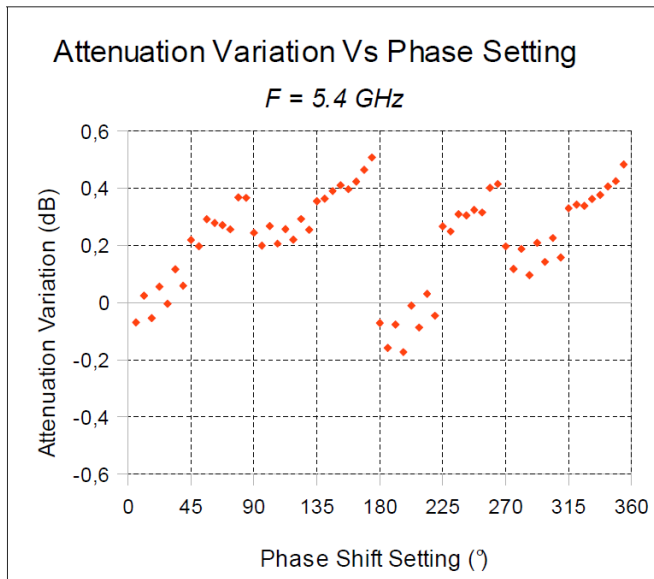
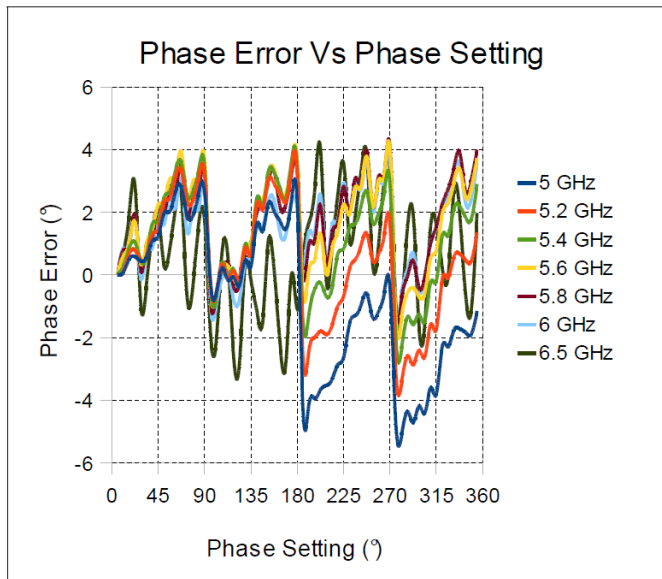
Typical Performance Curves:



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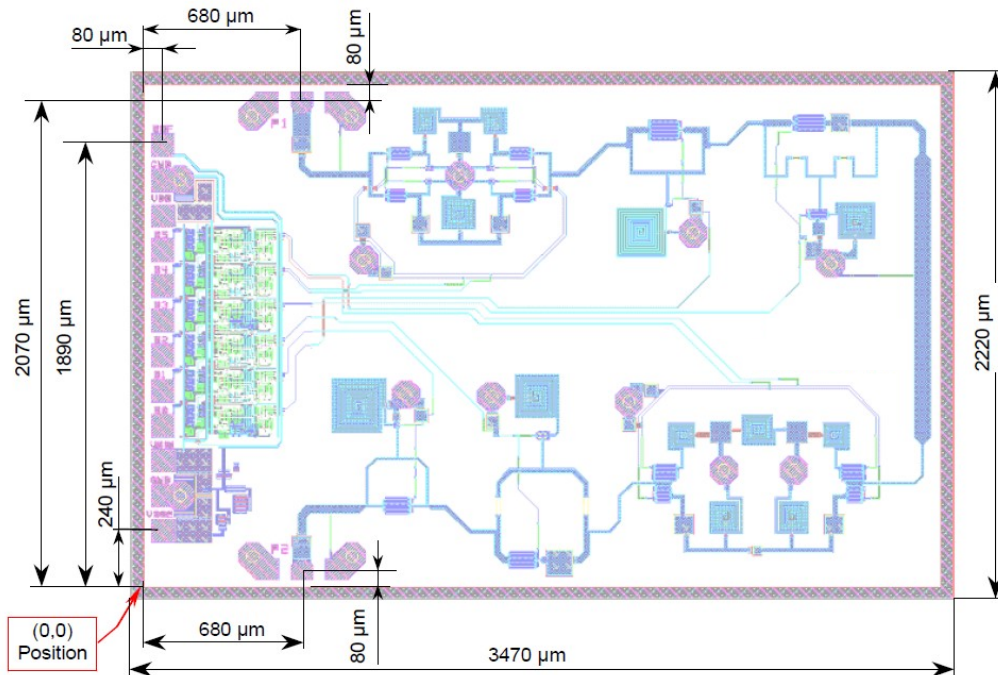
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Mechanical Information:



Chip Size = 3470 x 2220 μm ($\pm 5 \mu\text{m}$ after dicing)
 DC Pads = 100 x 100 μm , spacing = 150 μm , top metal = Au
 RF Pads = 100 x 100 μm , pitch = 150 μm , top metal = Au
 Chip Thickness = 100 μm

Pad Position⁴

Pad Name	Symbol	Coordinate		Description
		X	Y	
P2	RF _{OUT}	680	80	RF Port 2
P1	RE _{IN}	680	2070	RF Port 1
VSS2	V _{SS2}	08	240	V _{SS2} power supply
GND	GND	80	390	Ground (back side)
VSS1	V _{SS1}	80	540	V _{SS1} power supply
B0	A0	80	690	5.625° cell control
B1	A1	80	840	11.25° cell control
B2	A2	80	990	22.5° cell control
B3	A3	80	1140	45° cell control
B4	A4	80	1290	90° cell control
B5	A5	80	1440	180° cell control
VDD	V _D	80	1590	Do not use
GND	GND	80	1740	Ground (back side)
REF	V _{REF}	80	1890	Internal negative voltage (to be decoupled to ground)

7 4. X=0, Y=0 at bottom left corner. See Mechanical Information for more details.

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