Phase Shifter, X-Band, 6-Bit 8 - 12 GHz



CGY2172XAUH/C1

Rev. V1

Features

- Insertion Loss: 8 dB at 10 GHz
- Phase Shift Range = 360°
- RMS Phase Error 2° @ 10GHz
- Input P1dB +25 dBm
- S11 & S22 17 dB @ 10 GHz (All states)
- 0 / -3V Control Lines
- Chip Size: 3900 x 1300 μm ± 5 μm
- Tested, Inspected Known Good Die (KGD)
- Samples Available
- Demonstration Boards Available
- · Space and MIL-STD Available
- RoHS* Compliant

Applications

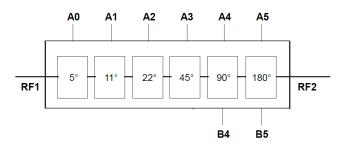
- Radar
- Telecommunication
- Instrumentation

Description

The CGY2172XAUH/C1 is a high performance GaAs MMIC 6-bit Phase Shifter operating in Xband. This device has a nominal phase shifting range of 0 - 360° in 5.625° steps and uses an optimum combination of switched line and high pass/low pass filters to obtain very low phase error and insertion loss variations. It covers the frequency range of 8 to 12 GHz.

The die is manufactured using 0.18 µm gate length pHEMT technology. The MMIC uses gold bond pads and backside metallization and is fully protected with Silicon Nitride passivation to obtain the highest level of reliability. This technology has been evaluated for Space applications and is on the European Preferred Parts List of the European Space Agency.

Block Diagram



Ordering Information

Part Number	Package
CGY2172XAUH/C1	DIE

For further information and support please visit: https://www.macom.com/support

^{*} Restrictions on Hazardous Substances, compliant to current RoHS EU directive.



Electrical Specifications: Measured On Wafer, Freq. = 10 GHz, T_A = +25°C

Parameter	Test Conditions	Units	Min.	Тур.	Max.
Insertion Loss	_	dB	_	8	_
Noise Figure	@ Reference State	dB	_	8	_
Phase Range	_	۰	_	360	_
Input & Output Return Loss	@ RF1 & RF2	dB	_	17	_
RMS Phase Error vs. Phase Setting ¹	_	٥	_	2	_
Maximum Phase Error vs. Phase Setting		dB	_	±5	_
RMS Attenuation variation with Phase setting ¹	_	dB	_	0.2	_
Maximum Attenuation Variation with Phase Setting	_	dB	_	±0.3	_
P1dB	_	dBm		25	

^{1.} The RMS value is the root mean square of the error defined as below: Where x_i is the difference between the measured value and the expected value.

$$x_{\text{rms}} = \sqrt{\frac{1}{N} \sum_{i=1}^{N} x_i^2} = \sqrt{\frac{x_1^2 + x_2^2 + \dots + x_N^2}{N}}$$

Absolute Maximum Ratings^{2,3}

Parameter	Absolute Maximum
Phase Control Inputs	-4 to 0 V
Input Power	TBD dBm
Junction Temperature	+150°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +150°C

^{2.} Exceeding any one or combination of these limits may cause permanent damage to this device.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

MACOM does not recommend sustained operation near these survivability limits.

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Logic Truth Table

	A0	A1	A2	А3	A4	B4	A5	B5
Nominal Phase Shift	-5.625°	-11.25°	-22.5°	-45°	-90°	-90°	-180°	-180°
Pad	P5	P11	P22	P45	P90	P90B	P180	P180B
Phase Shift Activated	-3 V	-3 V	-3 V	-3 V	-3 V	0 V	-3 V	0 V
Reference State	0 V	0 V	0 V	0 V	0 V	-3 V	0 V	-3 V

Logic Truth Table (V)

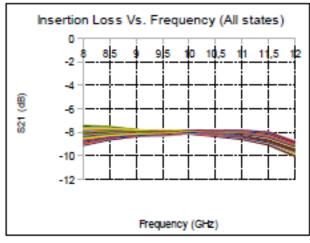
	B5	A5	B4	A4	А3	A2	A1	A0
Phase Shift (°)	-180°	-180°	-90°	-90°	-45°	-22°	-11°	-5°
0	1	0	1	0	0	0	0	0
-5.625	1	0	1	0	0	0	0	1
-11.25	1	0	1	0	0	0	1	0
-22.5	1	0	1	0	0	1	0	0
-45	1	0	1	0	1	0	0	0
-61	1	0	1	0	1	0	1	1
-90	1	0	0	1	0	0	0	0
-180	0	1	1	0	0	0	0	1
-270	0	1	0	1	0	0	0	0
-354	0	1	0	1	1	1	1	1

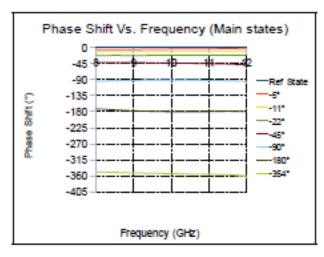
Control Voltage

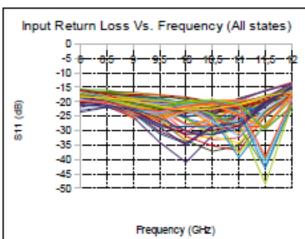
State	Min.	Тур.	Max.	Unit
Low (0)	-3.25	-3.00	-2.75	V
High (1)	-0.1`	0	+0.1	V

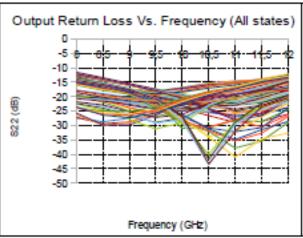


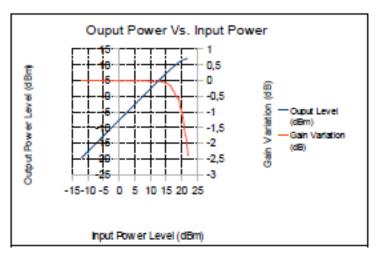
Typical Performance Curves:





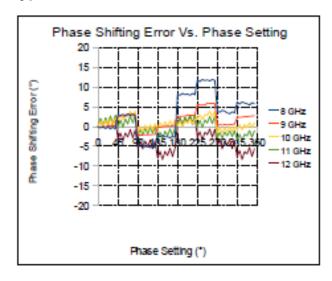


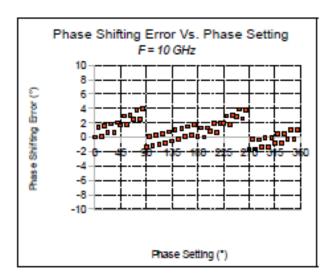


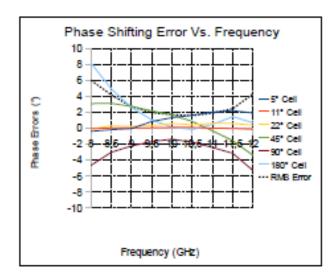




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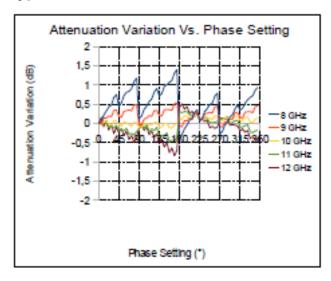


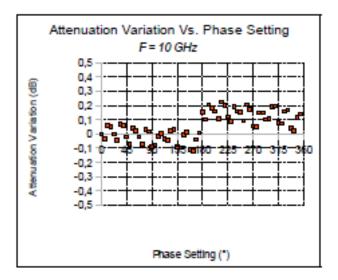


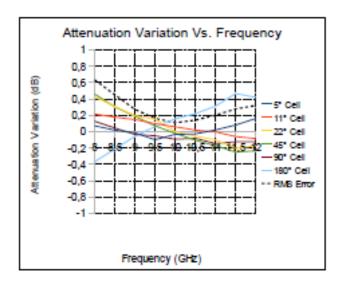




Typical Performance Curves:



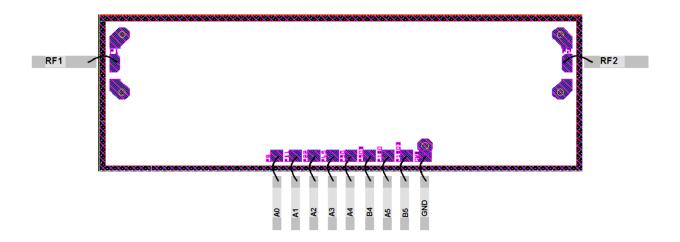




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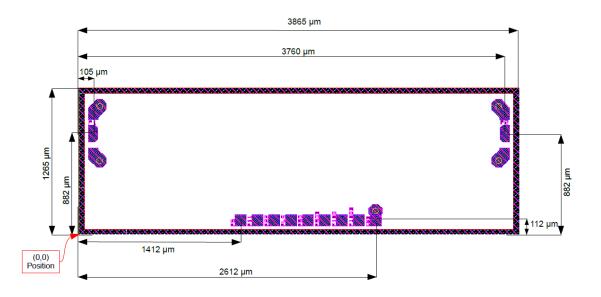
Bonding Diagram & Assembly Information:



RF interface : coplanar or microstrip, bonding $\approx 400/500 \ \mu m$.



Mechanical Information:



Chip Size = $3900 \times 1300 \ \mu m \ (\pm 5 \ \mu m)$ DC Pads = $100 \times 100 \ \mu m$, spacing = $150 \ \mu m$, top metal = Au RF Pads = $85 \times 150 \ \mu m$, top metal = Au Chip Thickness = $100 \ \mu m$

Pad Position⁴

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Pad Name	Symbol	X	Y	Description
P1	RF1	105	882	RF Port 1
P2	RF2	3760	882	RF Port 2
P5	A0	1412	112	5° cell control
P11	A1	1562	112	11° cell control
P22	A2	1712	112	22° cell control
P45	A3	1862	112	45° cell control
P90	A4	2012	112	90° cell control
P90B	B4	2162	112	90° cell control
P180	A5	2312	112	180° cell control
P180B	B5	2462	112	180° cell control
GND	GND	2612	112	Ground (back side)

^{4.} X=0, Y=0 at bottom left corner. See Mechanical Information for more details.

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