Features

- Gain Tx/Rx: 6 dB @ 10 GHz
- RMS Phase Error: 3.0° @ 9 - 10 GHz
- RMS Amplitude Error: 0.4 dB @ 8 - 11 GHz
- Output P1dB Tx: 11 dBm
- Output P1dB Rx: 11 dBm
- Return Loss: < -17 dB @ 10 GHz (all states)
- Total Power Consumption: 0.36 W
- Chip Size: 4700 x 3800 µm
- Tested, Inspected Known Good Die (KGD)
- Samples Available
- RoHS* Compliant

Applications

- Radar
- Telecommunication
- Instrumentation

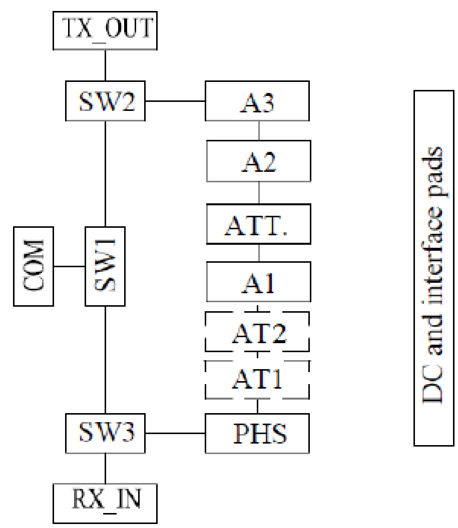
Description

The CGY2170YUH/C1 is a high performance GaAs MMIC T/R 6–bit core chip operating in X-band. It exhibits 3 RF ports including 3 switches. It includes a 6-bit phase shifter, a 6-bit attenuator, and switches. It has a phase shifting range of 360° and a gain setting range of 31.5 dB. It covers the frequency range from 8 to 12 GHz and provide 6 dB of gain at 10 GHz

The on-chip control logic with serial input register minimizes the number of bonding pads and greatly simplifies the interfacing to this device.

This die is manufactured using 0.18 µm gate length ED02AH pHEMT Technology. The MMIC uses gold bond pads and backside metallization and is fully protected with Silicon Nitride passivation to obtain the highest level of reliability. This technology has been evaluated for Space applications and is on the European Preferred Parts List of the European Space Agency.

Block Diagram



Ordering Information

Part Number	Package
CGY2170YUH/C1	Die

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications:
Freq. = 8 - 12 GHz (unless otherwise specified), T_A = +25°C

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Supply Voltage	Positive Negative Digital Negative Gate Drain	V	+2.5 -2.5 — -1.0 +2.5	+3.0 -3.0 -3.0 -0.8 +3.0	+3.5 -3.5 — 0 +3.5
Gain TX/RX	8 GHz 10 GHz 12 GHz	dB	5.0	5.8 6.0 6.5	7.5
Noise Figure	@ Reference State	dB	—	TBD	—
Return Loss	All States	dB	-20	-15	-12
Isolation	—	dB	35	—	—
Attenuation Range	—	dB	—	31.5	—
RMS Attenuation Error	64 Attenuation States & at Reference Phase State	dB	—	0.4	0.6
Attenuation Variation	64 Phase State & at Reference Attenuation State	dB	—	1.2	1.5
Phase Range	—	°	—	-354	—
RMS Phase Error	64 Phase State & at Reference Attenuation State 8 GHz 9 - 11 GHz 8 - 12 GHz	°	—	— 3.0 4.0	4.5 4.0 5.0
Phase Variation	64 Attenuation States & at Reference Phase State 0 - 24 dB 24 - 31.5 dB	°	—	—	±5 ±8
P1dB	—	dBm	11	13	—
Switching Time	—	ns	—	30	—
Serial Data Rate		Mbps	—	20	>230

1. The RMS value is the root mean square of the error defined as below:
2. Where x_i is the difference between the measured value and the theoretical value, x_i is the mean value of the N x_i, and σxi is the standard deviation of x_i.

$$x_{RMS} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} x_i^2} = \sqrt{\bar{x_i}^2 + \sigma_{x_i}^2}$$

Absolute Maximum Ratings[3,4]

Parameter	Absolute Maximum
Supply Voltage Positive Negative Digital Negative Gate Drain	 -1 to +5 V -5 to +1 V -6 to 0 V -2.5 - 0 V 0 to +6 V
Digital Data Input	-1 to +7 V
Input Power	25 dBm
Junction Temperature	+150°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +150°C

3. Exceeding any one or combination of these limits may cause permanent damage to this device.
4. MACOM does not recommend sustained operation near these survivability limits.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Data (Reference State HIGH)

Bit #	Name	Value	Description
B0	SD0	Standby for Rx	ST_RX
B1	ST1	5.625°	Shifter on TX
B2	ST2	11.25°	
B3	ST3	22.5°	
B4	ST4	45°	
B5	ST5	90°	
B6	ST6	180°	
B7	SR1	5.625°	Shifter on RX
B8	SR2	11.25°	
B9	SR3	22.5°	
B10	SR4	45°	
B11	SR5	90°	
B12	SR6	180°	
B13	ATT1	0.5 dB	Attenuation on TX
B14	ATT2	1 dB	
B15	ATT3	2 dB	
B16	ATT4	4 dB	
B17	ATT5	8 dB	
B18	ATT6	16 dB	
B19	ATR1	0.5 dB	Attenuation on RX
B20	ATR2	1 dB	
B21	ATR3	2 dB	
B22	ATR4	4 dB	
B23	ATR5	8 dB	
B24	ATR6	16 dB	
B25	SD1	Standby for Tx	ST_TX

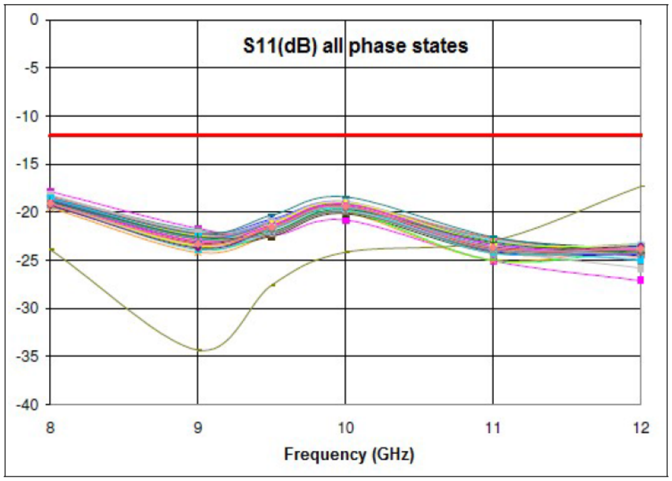
Control Voltage (CMOS Standard Logic)[5]

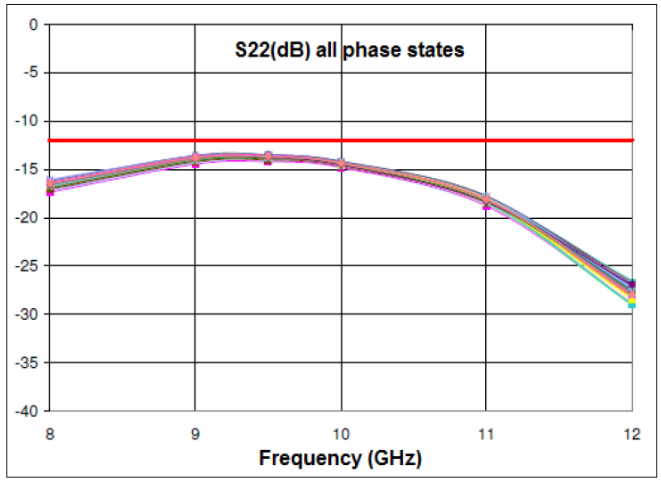
State	V Min.	V max.
Low	0 V	1 V
High	2.5 V	V_{DN}

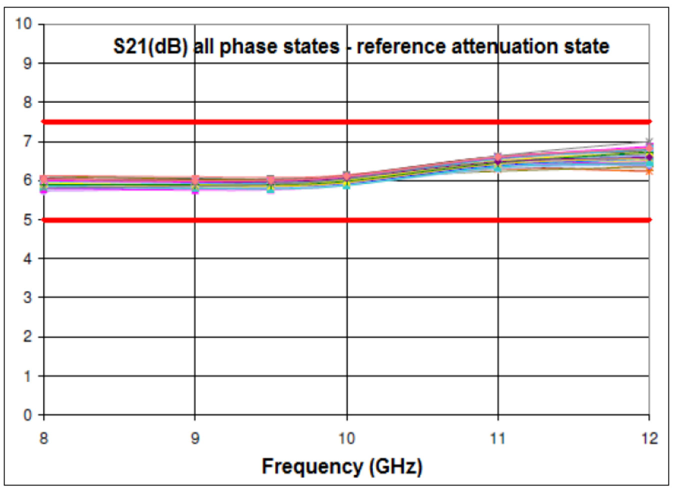
5. To compensate process variation, two variable attenuators are inserted between phase-shifter and first amplifier. The 2 x 1 dB gain adjustment is obtained with an analog voltage applied on two additional PAD: AT1 and AT2. The core-chip gain is 6 dB for AT1 = -0.9 V and AT2 = -0.9 V.

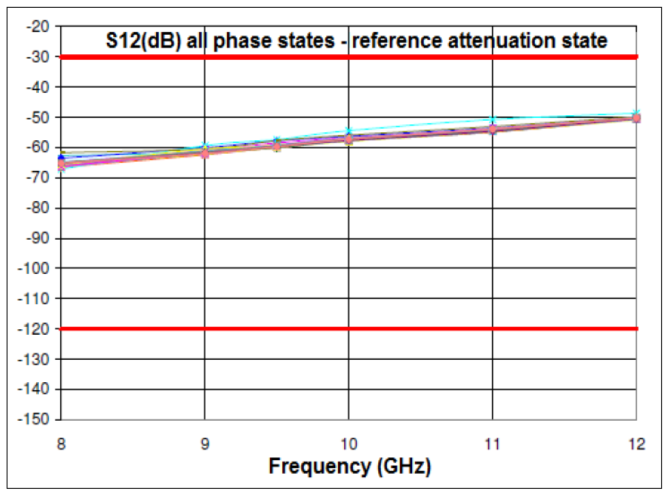
Typical Performance Curves: On Wafer Measurements

Calculated with input and output inductance of 0.5 nH to take into account the bond inductance.









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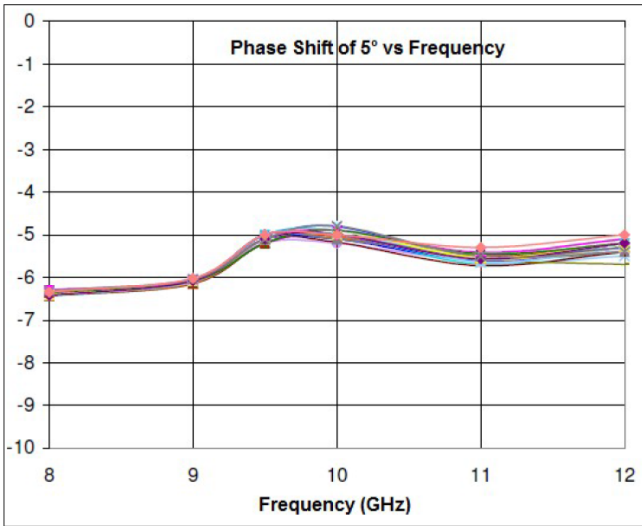
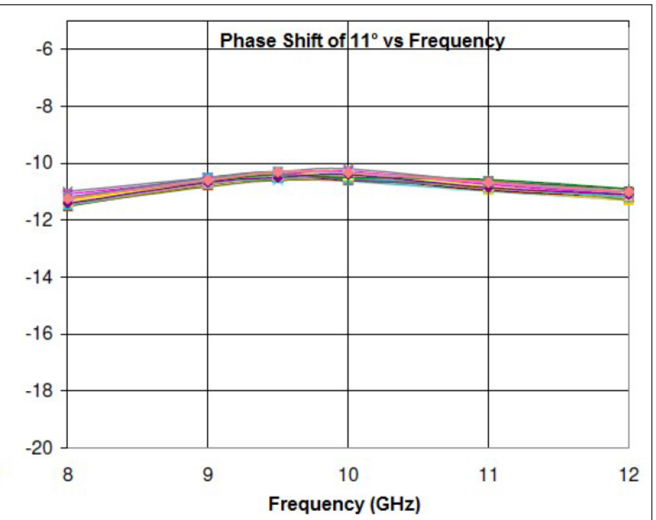
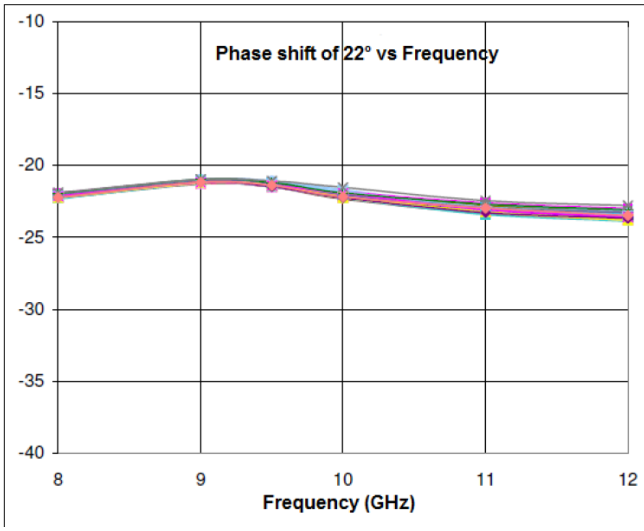
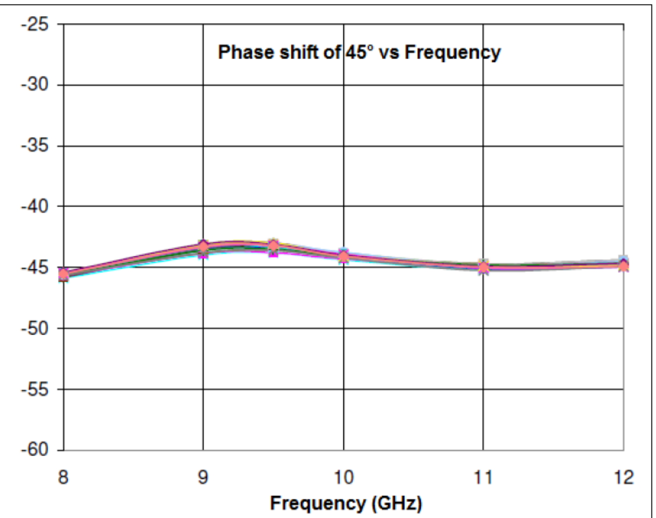
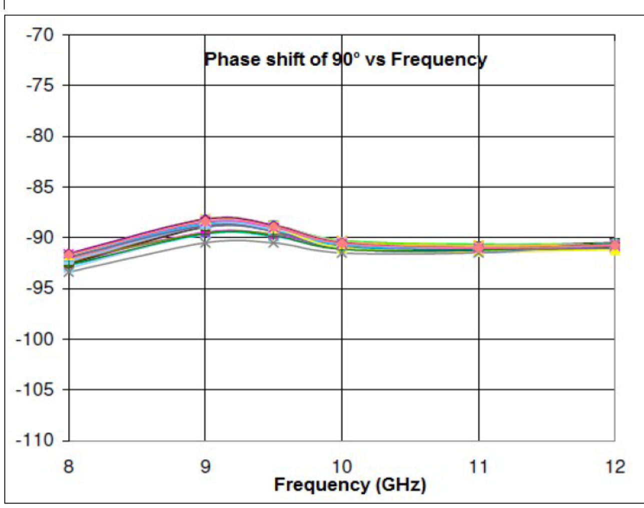
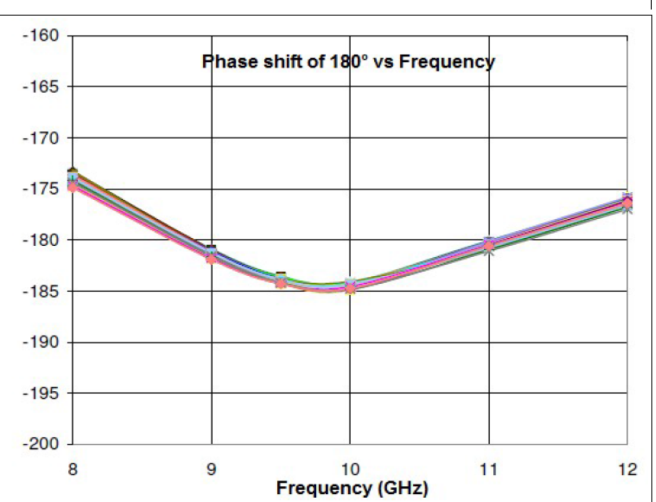






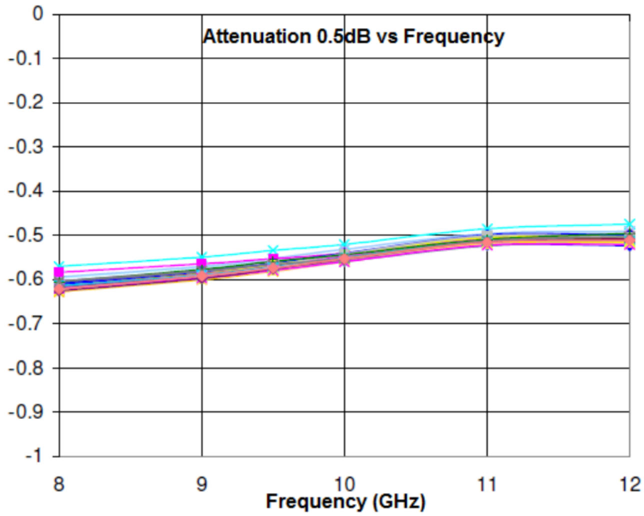


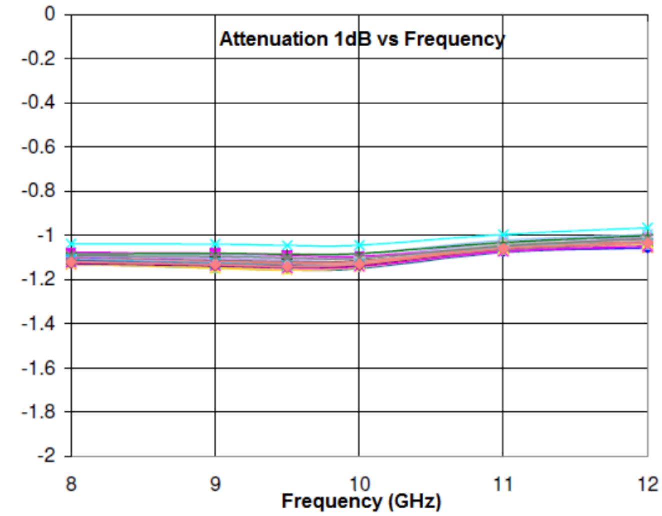


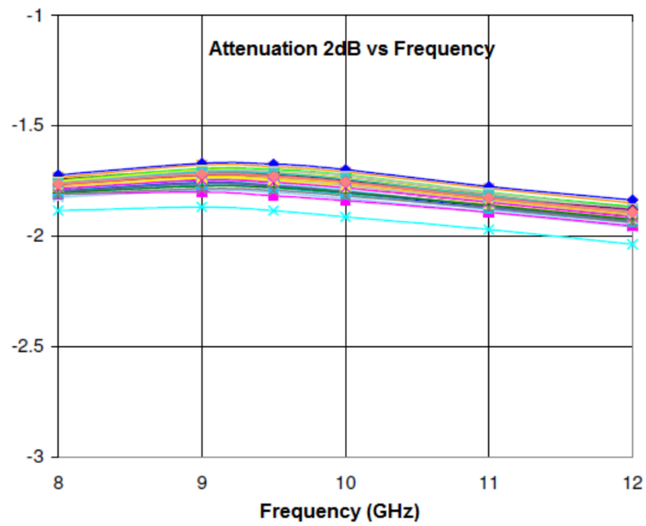


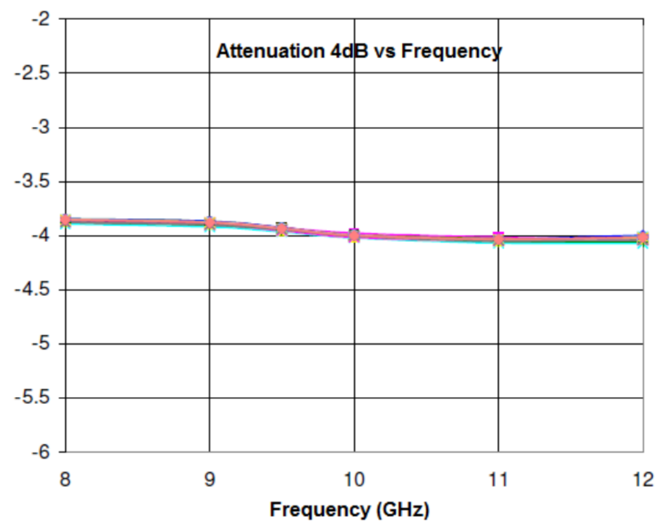
Typical Performance Curves: On Wafer Measurements

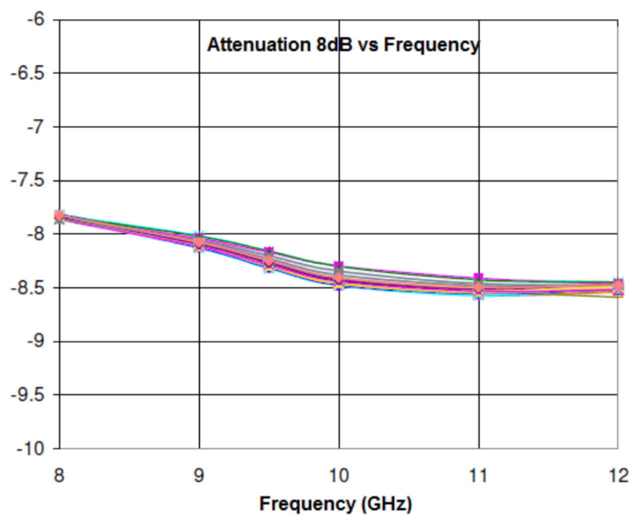
On wafer measurements embedding 500pH of wire bonding.

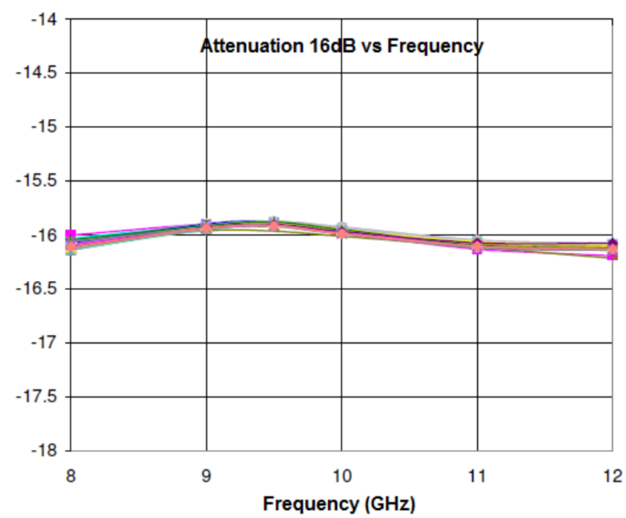












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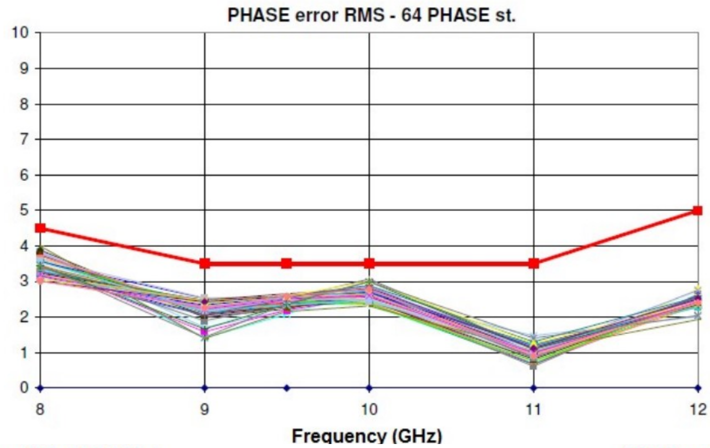
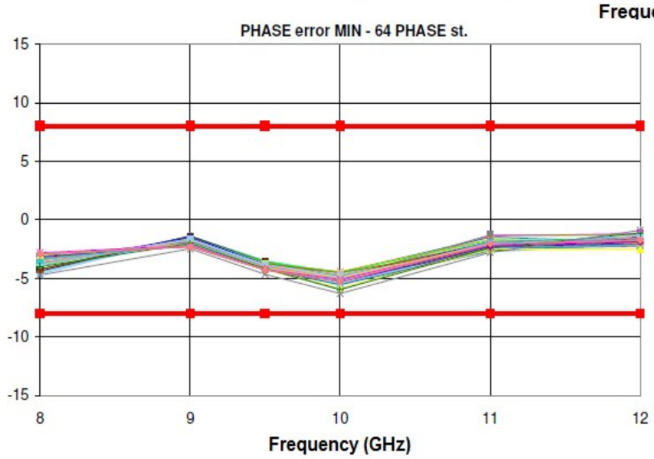
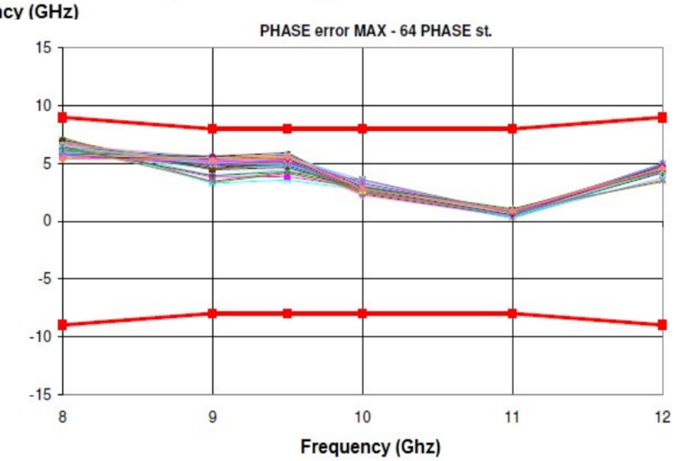
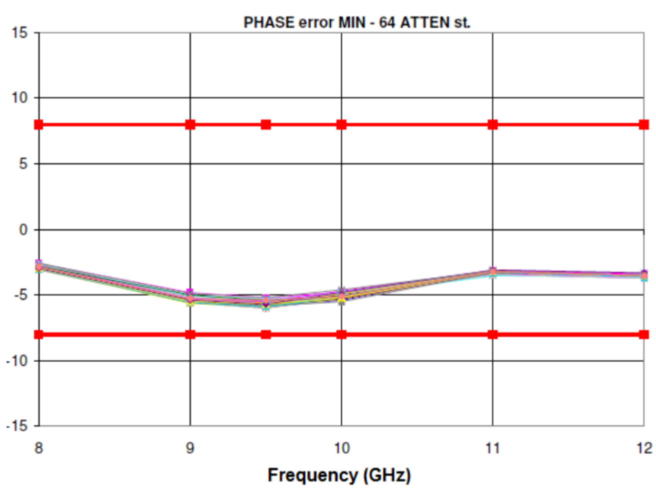
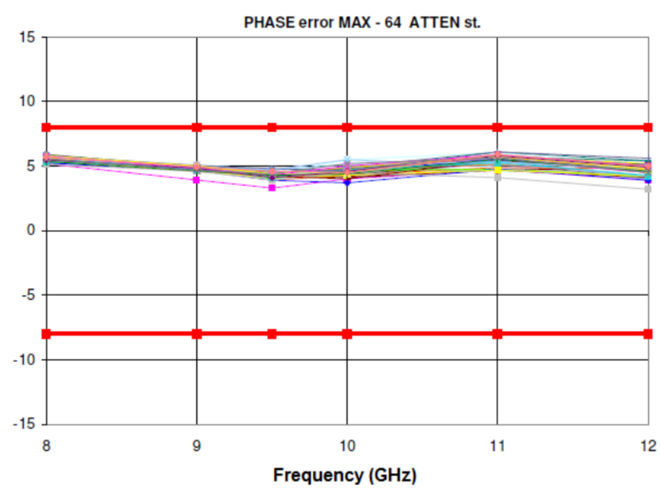
On wafer measurements embedding 500pH of wire bonding.











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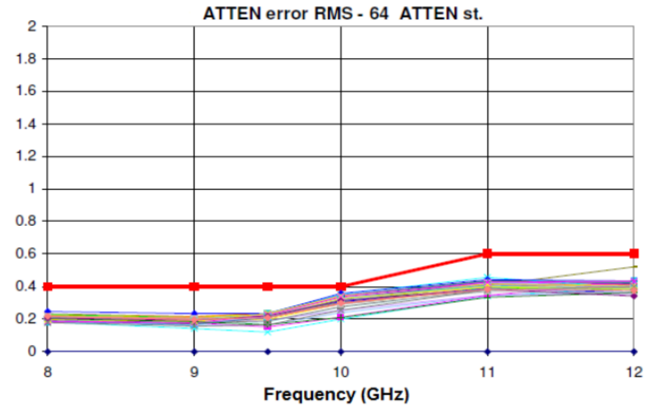
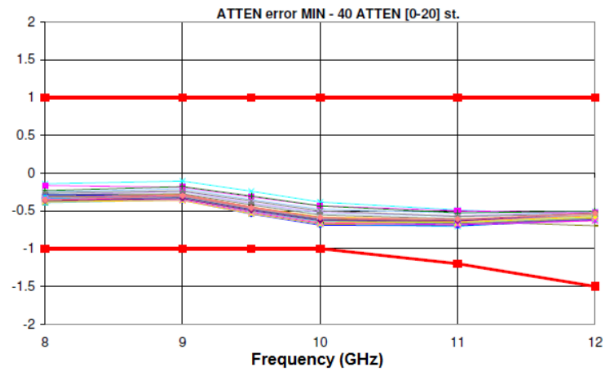
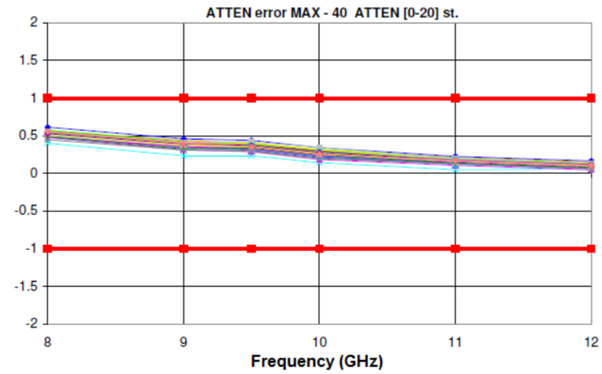
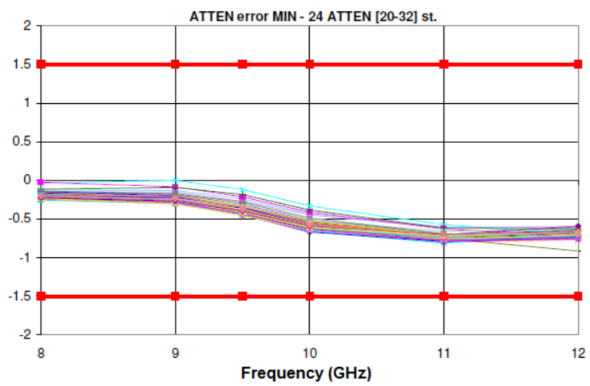
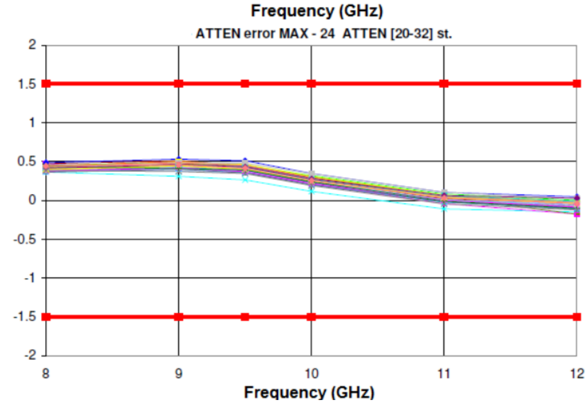
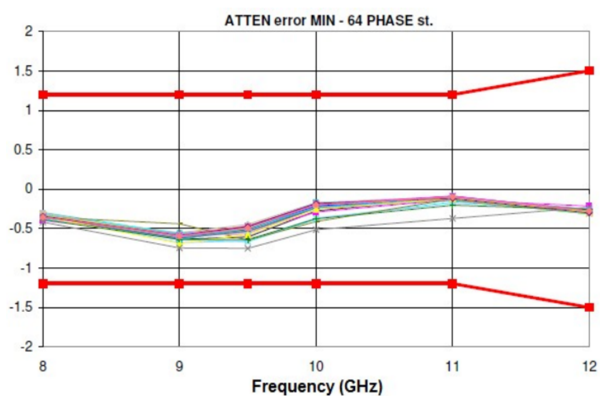


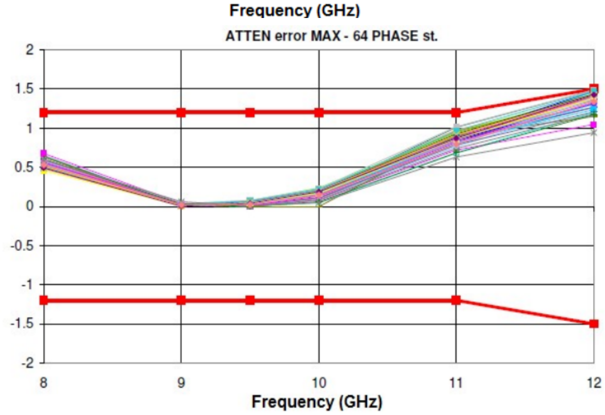




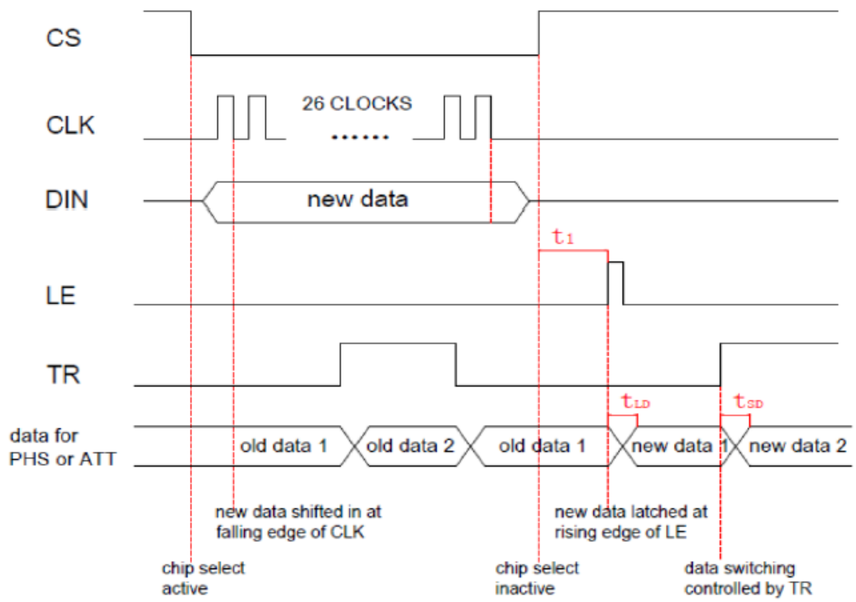








Timing Diagram



- The serial data input is controlled by falling edge of signal CLK and will be shifted into a 26-bit shift register and will be latched on LE rising edge and complete data update.

- The control data during transmission and receiving are saved in two independent latches. Under the control of the T/R switch pulse, the control data will control phase shifter and attenuator in Time division Multiplexer (TDM).

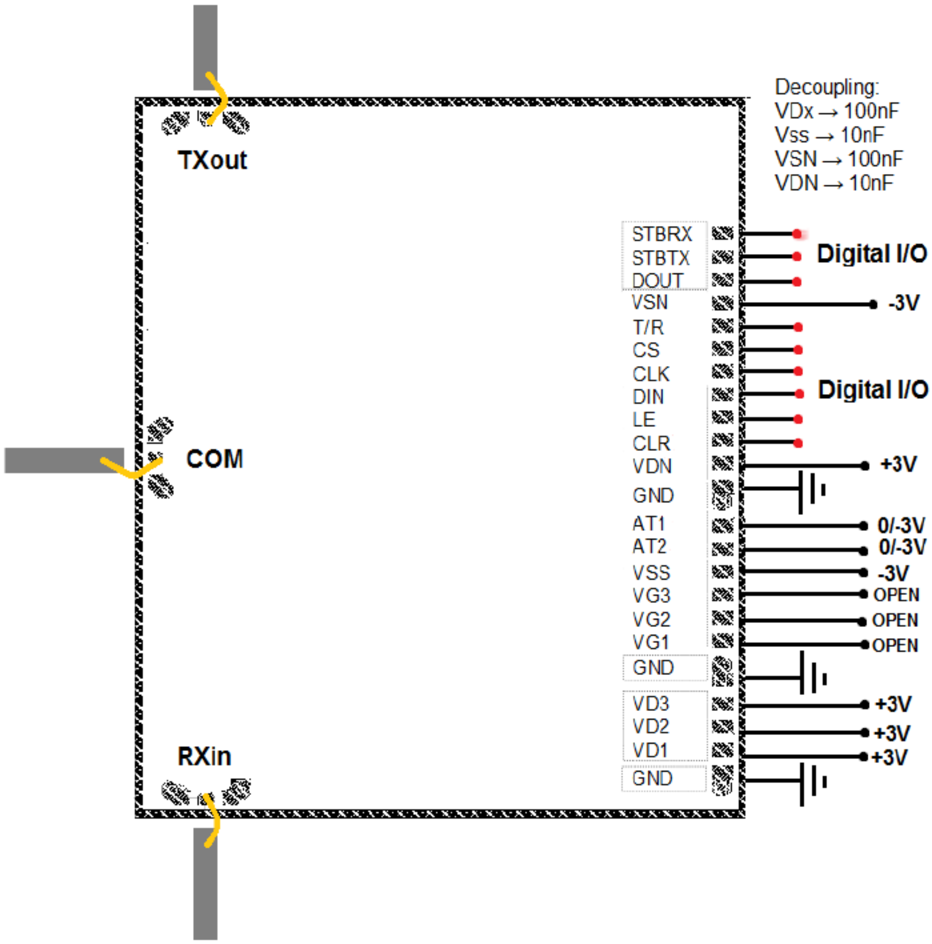
  new data 1: SR1~SR6 for PHS;ATR1~ATR6 for ATT(TR="0",in Rx mode).
  new data 2: ST1~ST6 for PHS;ATT1~ATT6 for ATT(TR="1",in Tx mode).

  The delay time [t1] is defined by the user.
  [tSD] : Tx/Rx switching time
  [tLD] : [tDU] data latching time

Switching Control

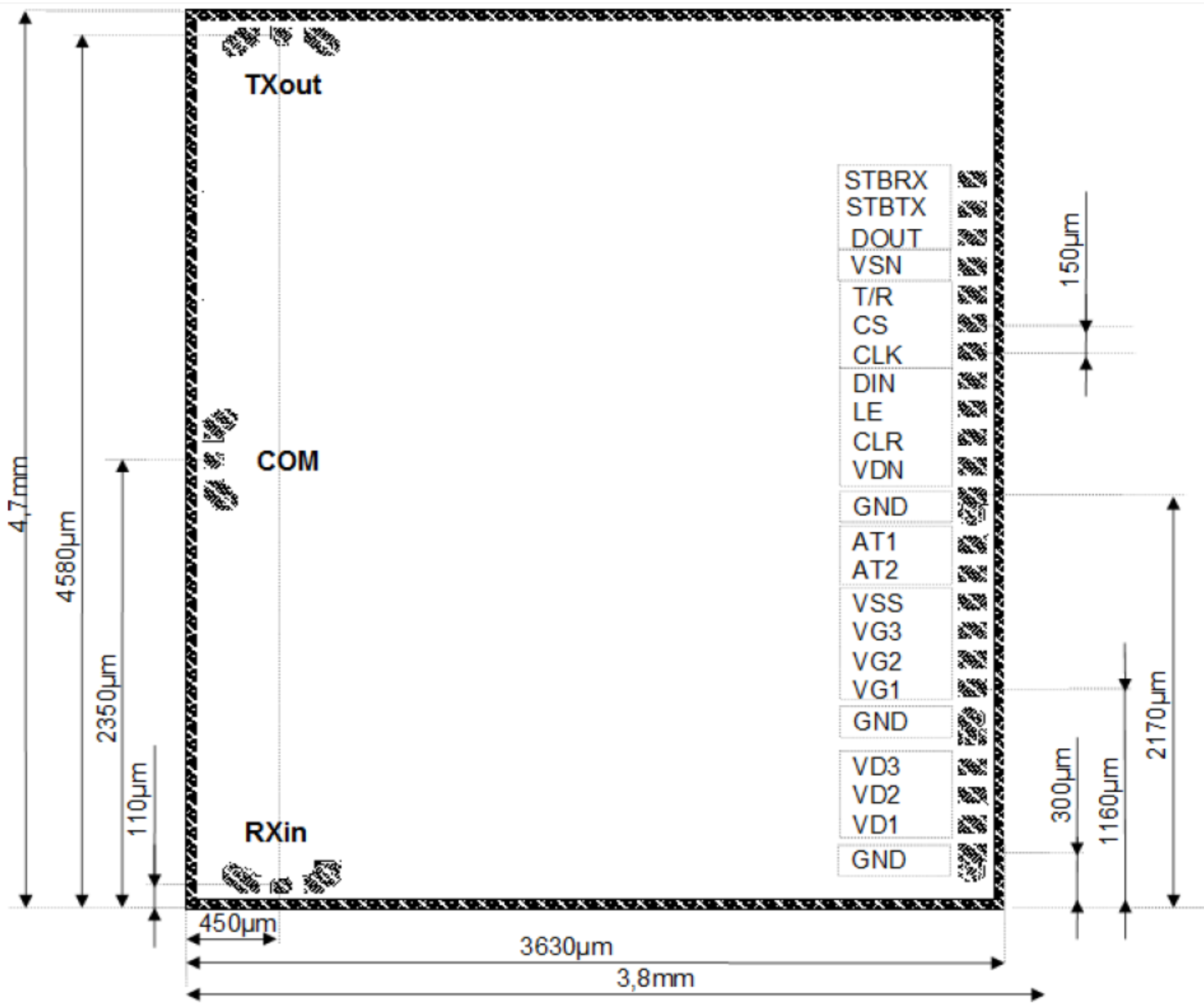
Voltage	Tx Mode	Rx Mode
Low (0 V)	—	T/R
High (3 V)	T/R	—

Bonding Diagram & Assembly Information



VG1 VG2 and VG3 can be used to tune currents but should be left open.
The RF interfacing bond wires or ribbon should be kept as short as possible, The RF lines should be 300 µm wide or less to minimize discontinuities associated with the connection to the MMIC bond pads.

Mechanical Information



Chip Size = 3800 x 4700 µm (before wafer sawing)
DC Pads = 100 x 140 µm, spacing = 150 µm, top metal = Au
RF Pads = 90 x 90 µm, pitch = 150 µm, top metal = Au
Chip Thickness = 100 µm
Backside Metal = TiAu

Pad Position[6]

Pad Name	Coordinate		Description
	X	Y	
RXIN	450	110	Rx Input
COM	110	2350	Com Port
TXOUT	450	4580	Tx Output
GND	3630	300	Ground
VD1	3630	450	Drain Voltage Supply 1
VD2	3630	600	Drain Voltage Supply 2
VD3	3630	750	Drain Voltage Supply 3
GND	3630	900	Ground
VG1	3630	1160	Gate Voltage Supply 1
VG2	3630	1310	Gate Voltage Supply 2
VG3	3630	1460	Gate Voltage Supply 3
VSS	3630	1610	Gate Voltage Supply
AT2	3630	1760	Input of external control of additional attenuator 2 (1 dB)
AT1	3630	1910	Input of external control of additional attenuator 1 (1 dB)
GND	3630	2170	Ground
VDN	3630	2320	Positive Voltage Supply
CLR	3630	2470	Clear Function for Register
LE	3630	2620	Data Latch Enable
DIN	3630	2770	Serial Data Input
CLK	3630	2920	Clock
CS	3630	3070	Chip Select
T/R	3630	3220	Tx/Rx Switch
VSN	3630	3370	Negative Voltage Supply
DOUT	3630	3520	Serial Data Output
STBTX	3630	3670	Standby Tx Output
STBRX	3630	3820	Standby Rx Output

6. X = 0, Y = 0 at bottom left corner.