6-Bit, X-Band Core Chip
8 - 12 GHz

CGY2170YHV/C1
Rev. V1

Features
- Gain Tx/Rx: 5.8 dB @ 10 GHz
- RMS Phase Error: 4.0° @ 9 - 10 GHz
- RMS Amplitude Error: 0.5 dB @ 8 - 11 GHz
- Output P1dB Tx: 12 dBm
- Output P1dB Rx: 12 dBm
- Return Loss: < -12 dB @ 10 GHz (all states)
- Total Power Consumption: 0.36 W
- QFN Size: 7 x 7 x 0.9 mm
- Tested, Inspected Known Good Die (KGD)
- Samples Available
- RoHS* Compliant

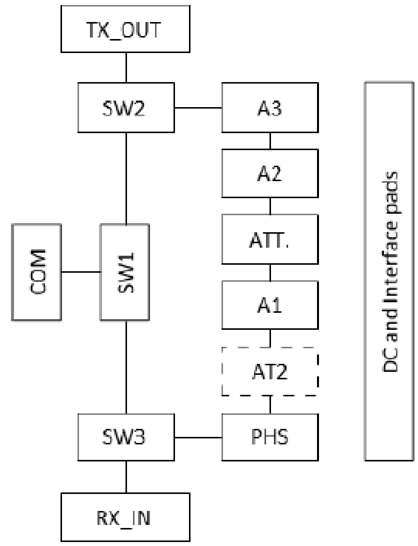
Applications
- AESA Radar
- Telecommunication
- Instrumentation

Description
The CGY2170YHV/C1 is a high performance GaAs MMIC T/R 6-bit core chip operating in X-band. It exhibits 3 RF ports including 3 switches. It includes a 6-bit phase shifter, a 6-bit attenuator, and switches. It has a phase shifting range of 360° and a gain setting range of 31.5 dB. It covers the frequency range from 8 to 12 GHz and provide 5.8 dB of gain at 10 GHz.

The on-chip control logic with serial input register minimizes the number of bonding pads and greatly simplifies the interfacing to this device.

This die is manufactured using 0.18 µm gate length ED02AH pHEMT technology. The MMIC uses gold bond pads and backside metallization and is fully protected with silicon nitride passivation to obtain the highest level of reliability. This technology has been evaluated for space applications and is on the European preferred parts list of the European space agency.

Block Diagram



Ordering Information

Part Number	Package
CGY2170YHV/C1	

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications:
Freq. = 10 GHz (unless otherwise specified), T_A = +25°C

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Supply Voltage	Positive Negative Digital Negative Drain	V	+2.5 -3.5 — +2.5	+3.0 -3.0 -3.0 +3.0	+2.5 -2.5 — +3.5
Gain TX/RX	8 GHz 10 GHz 12 GHz	dB	5.0	5.6 5.8 6.3	7.5
Noise Figure	@ Reference State	dB	—	TBD	—
Input Return Loss	All States	dB	—	-12	-10
Isolation	—	dB	35	—	—
Attenuation Range	—	dB	—	31.5	—
RMS Attenuation Error	64 Attenuation States & at Reference Phase State	dB	—	0.5	0.7
Attenuation Variation	64 Phase State & at Reference Attenuation State	dB	—	1.25	1.55
Phase Range	—	°	—	-354	—
RMS Phase Error	64 Phase State & at Reference Attenuation State 8 GHz 9 - 11 GHz 8 - 12 GHz	°	—	— 4.0 4.5	5.0 4.8 5.2
Phase Variation	64 Attenuation States & at Reference Phase State 0 - 24 dB 24 - 31.5 dB	°	—	—	±5 ±8
P1dB	—	dB	11	13	—
Switching Time	—	ns	—	30	—
Serial Data Rate		Mbps	—	20	>230

1. The RMS value is the root mean square of the error defined as below:
2. Where x_i is the difference between the measured value and the theoretical value, $\bar{x}_i$ is the mean value of the N x_i, and σxi is the standard deviation of x_i.

$$x_{RMS} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} x_i^2} = \sqrt{\bar{x}_i^{\,2} + \sigma_{x_i}^2}$$

Absolute Maximum Ratings[3,4]

Parameter	Absolute Maximum
Supply Voltage Positive Negative Digital Negative Drain	 -1 to +5 V -5 to +1 V -6 to 0 V 0 to +6 V
Digital Data Input	-1 to +7 V
Input Power	25 dBm
Junction Temperature	+150°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +150°C

3. Exceeding any one or combination of these limits may cause permanent damage to this device.
4. MACOM does not recommend sustained operation near these survivability limits.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Control Word Definition (Reference State HIGH)

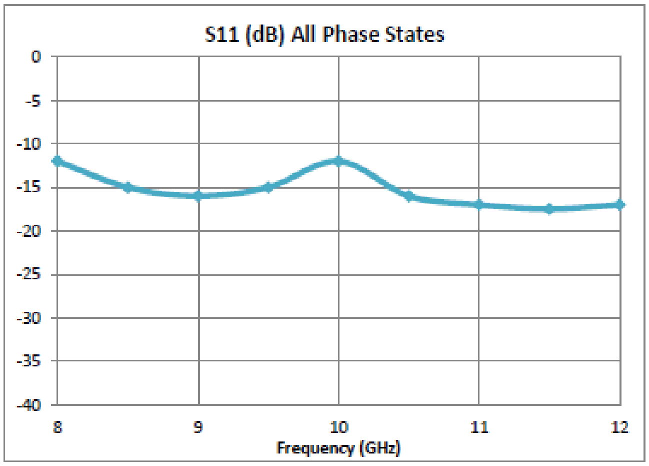
Bit #	Name	Value	Description
B0	SD0	Standby for Rx	ST_RX
B1	ST1	5.625°	TX Phase
B2	ST2	11.25°	
B3	ST3	22.5°	
B4	ST4	45°	
B5	ST5	90°	
B6	ST6	180°	
B7	SR1	5.625°	RX Phase
B8	SR2	11.25°	
B9	SR3	22.5°	
B10	SR$	45°	
B11	SR5	90°	
B12	SR6	180°	
B13	ATT1	0.5 dB	TX Attenuation
B14	ATT2	1 dB	
B15	ATT3	2 dB	
B16	ATT4	4 dB	
B17	ATT5	8 dB	
B18	ATT6	16 dB	
B19	ATR1	0.5 dB	RX Attenuation
B20	ATR2	1 dB	
B21	ATR3	2 dB	
B22	ATR4	4 dB	
B23	ATR5	8 dB	
B24	ATR6	16 dB	
B25	SD1	Standby for Tx	ST_TX

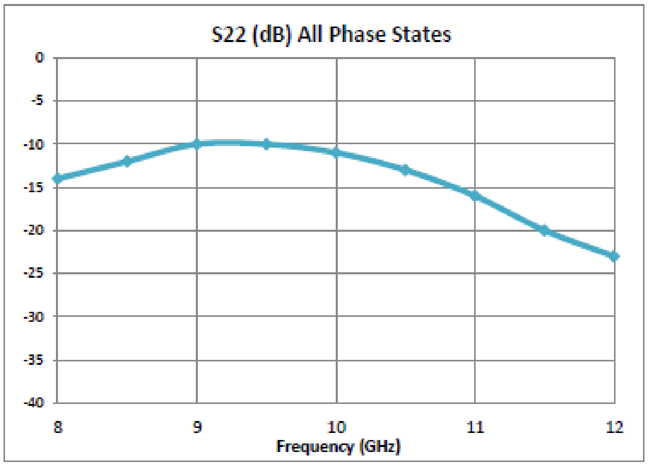
Control Voltage (CMOS Standard Logic)[5]

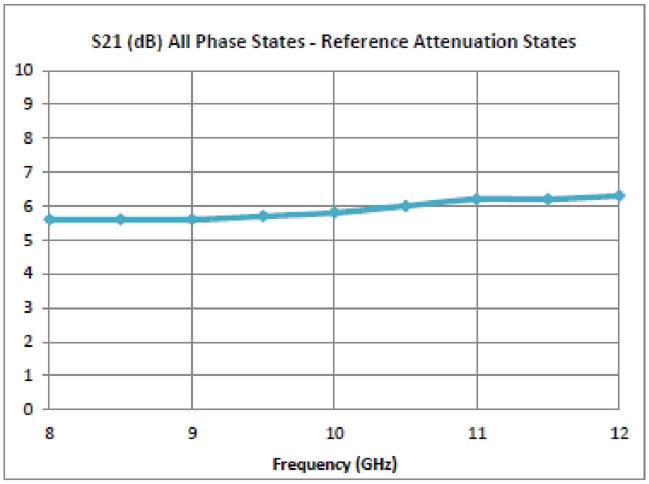
State	V Min.	V max.
Low	0 V	1 V
High	2.5 V	V_{DN}

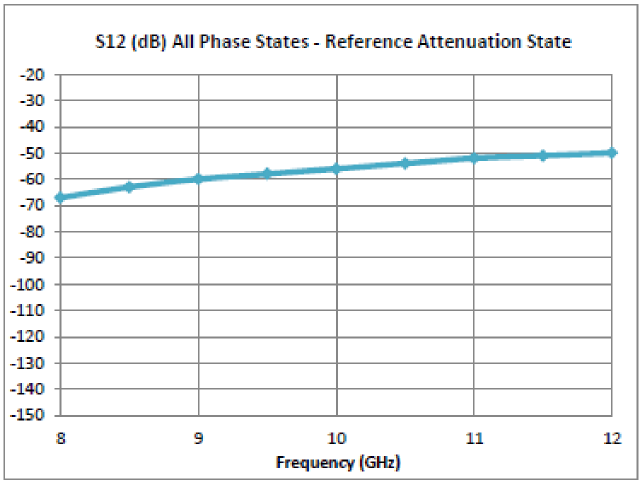
5. To compensate process variation, one variable attenuator is inserted between phase-shifter and first amplifier. The 2 x 1 dB gain adjustment is obtained with an analog voltage applied on 1 additional PAD: AT2. The core-chip gain is 5.8 dB for AT2 = -0.9 V.

Typical Performance Curves: On Wafer Measurements

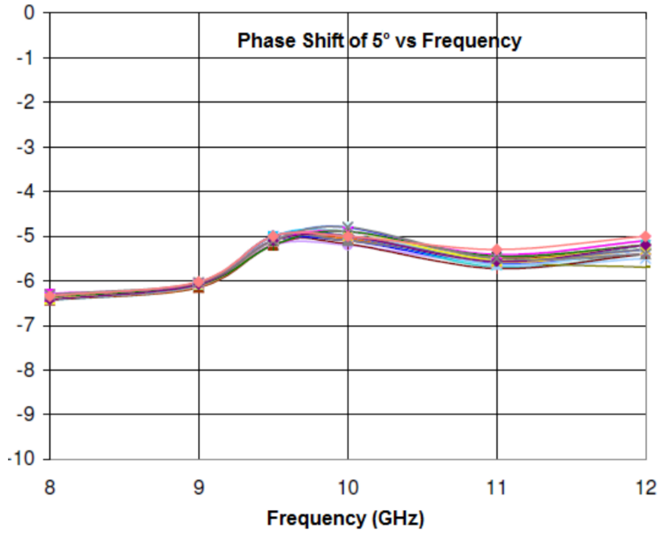


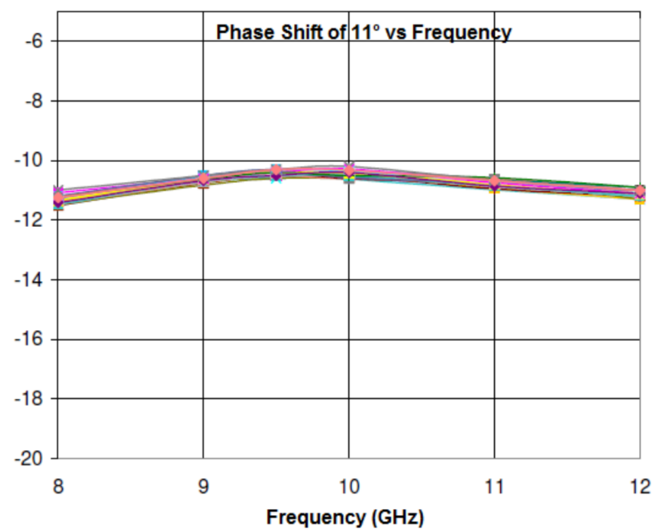


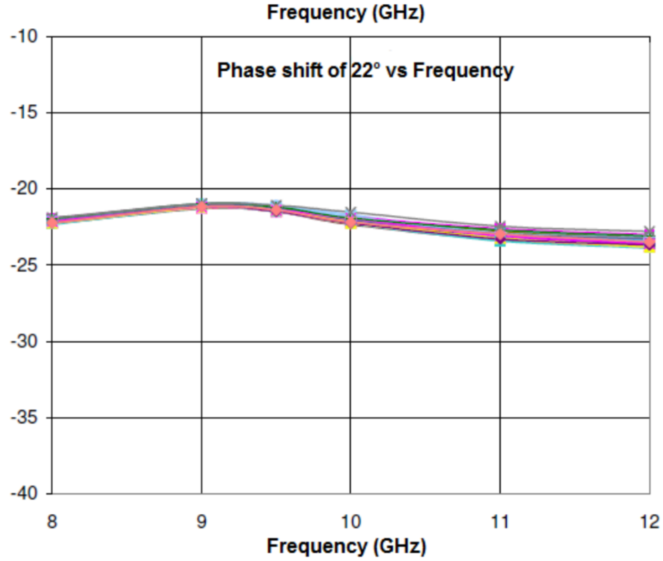


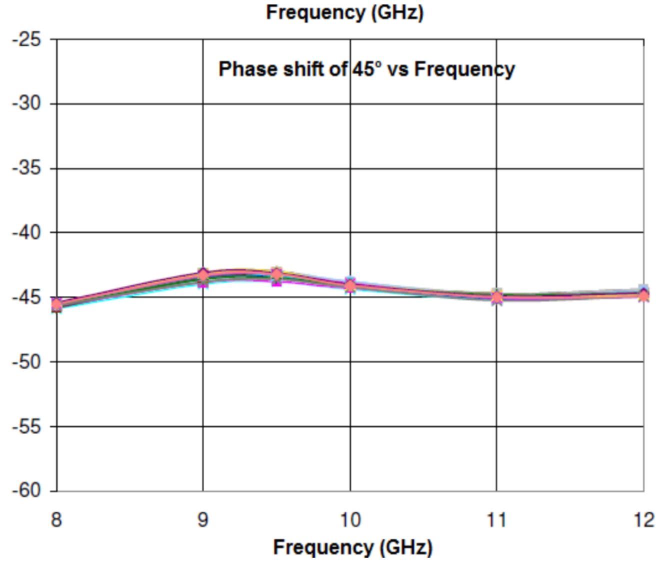


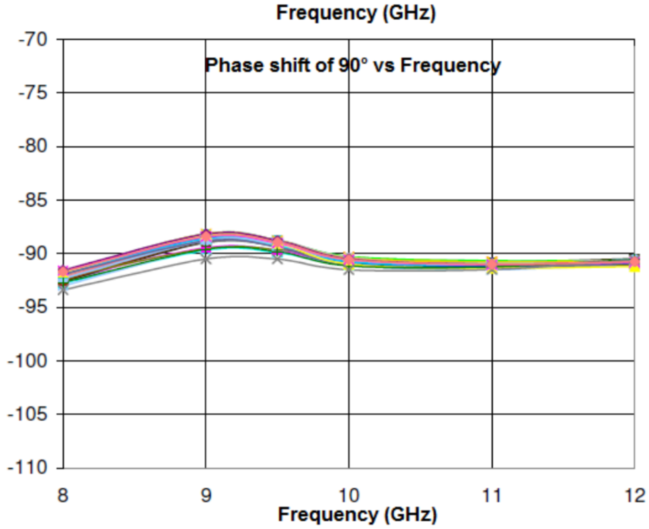
Typical Performance Curves: On Board Measurements—Phase Shifter Response

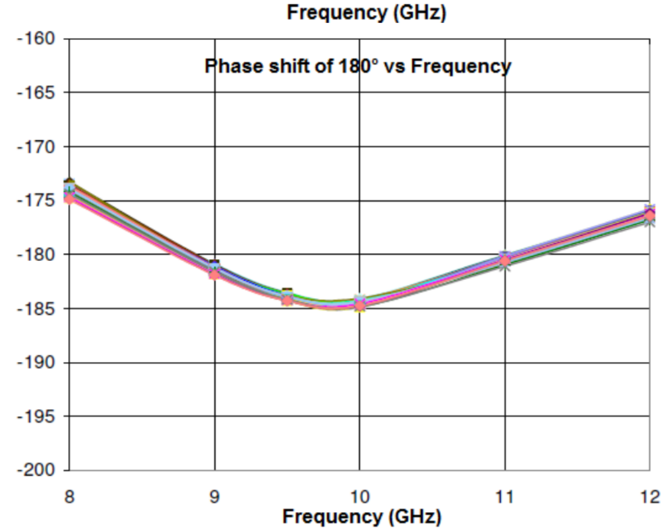




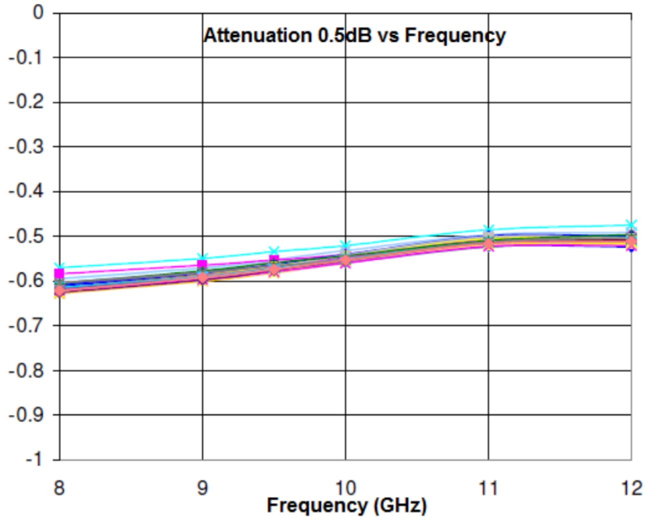


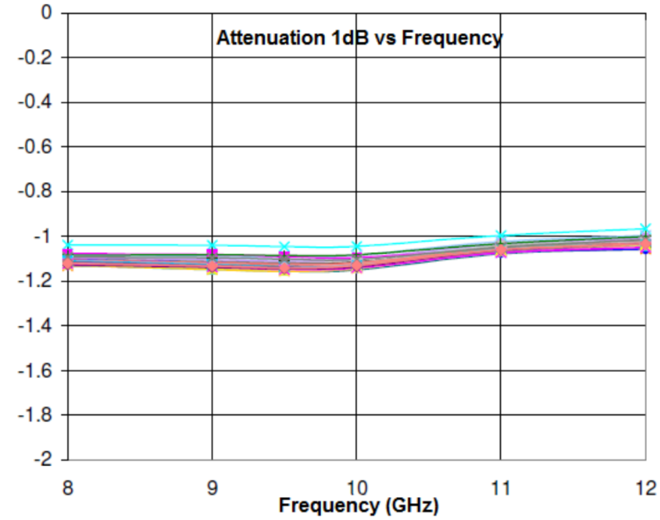


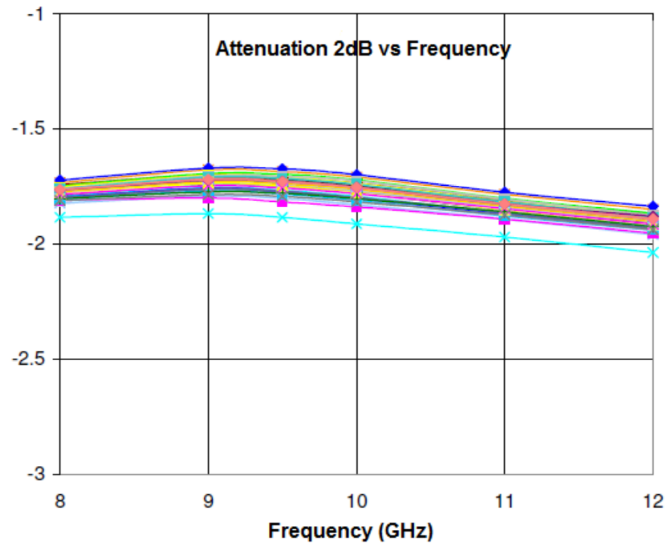


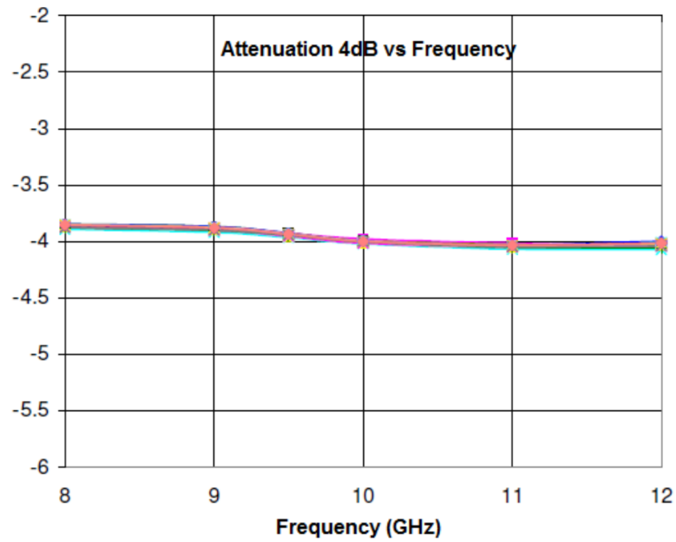


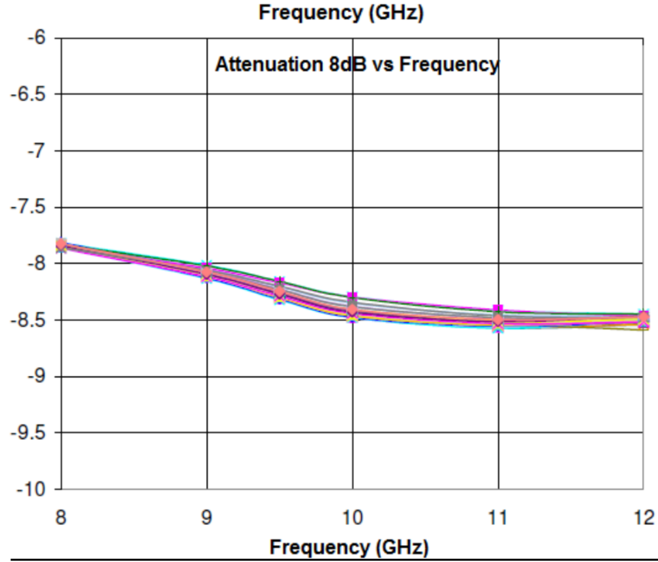
Typical Performance Curves: On Board Measurements—Attenuator Response

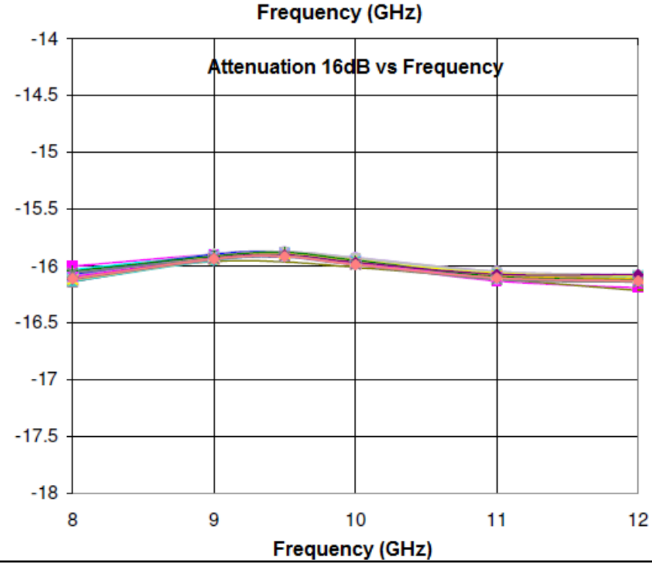




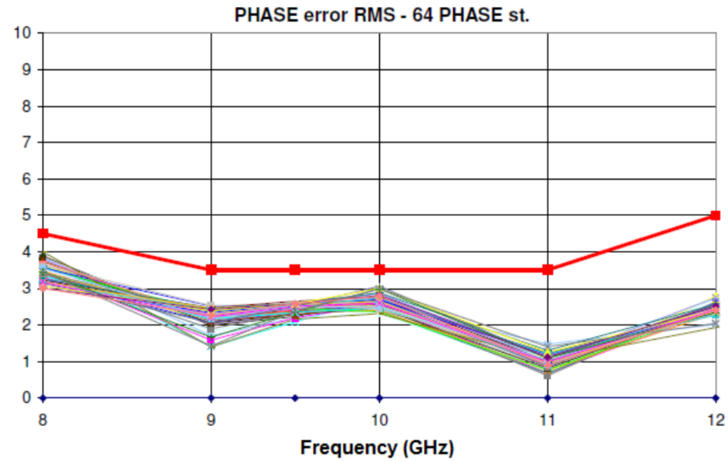


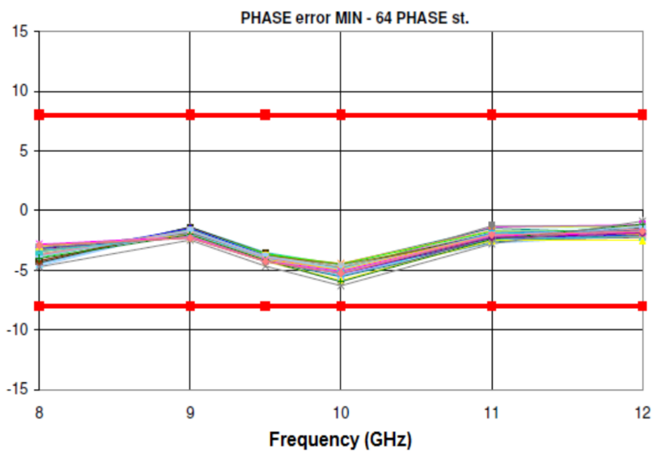


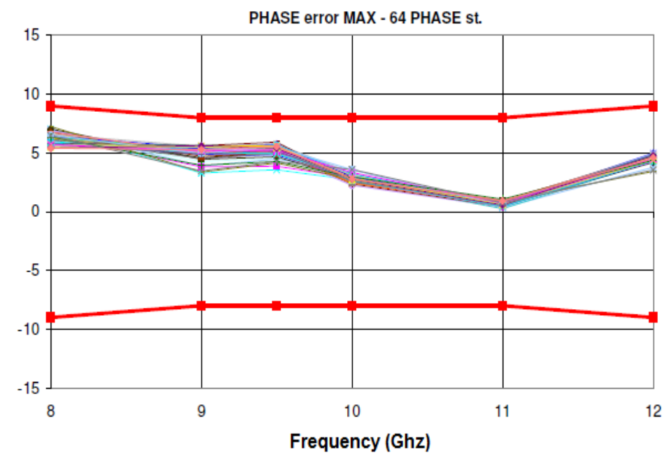


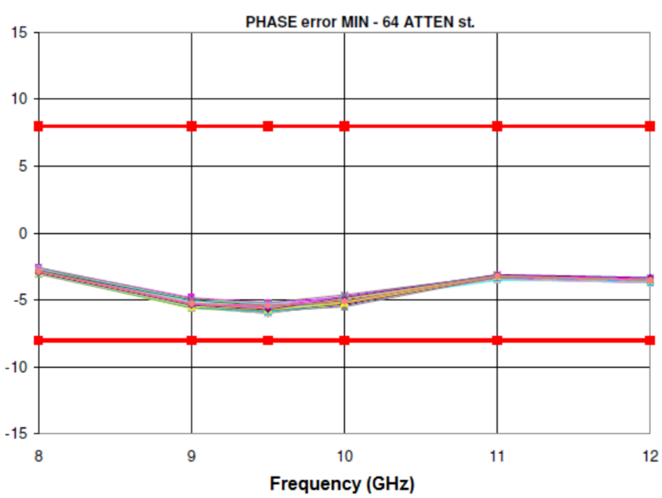


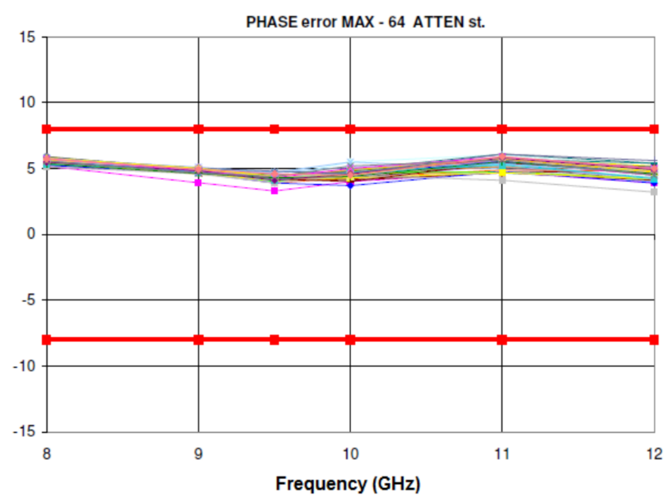
Typical Performance Curves: On Board Measurements—Phase Shifter Errors



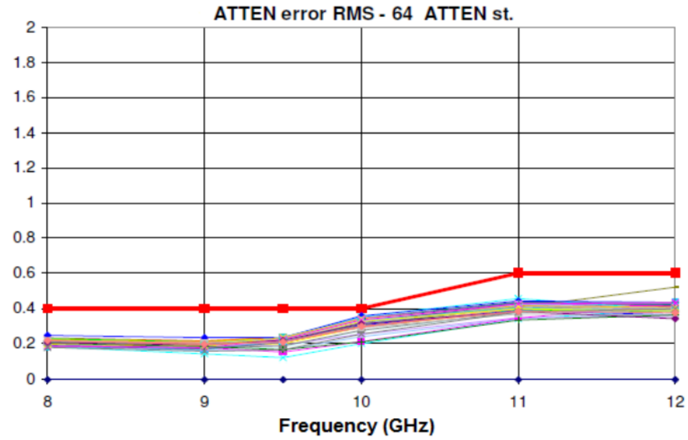


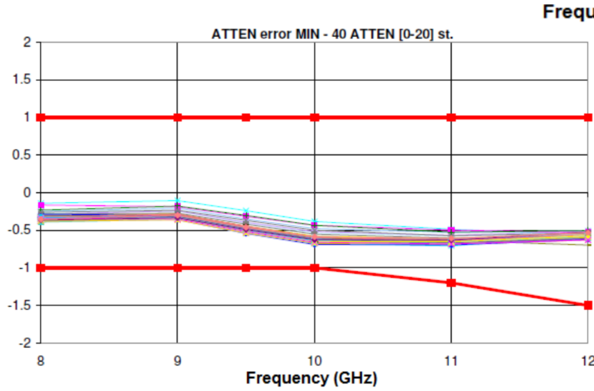


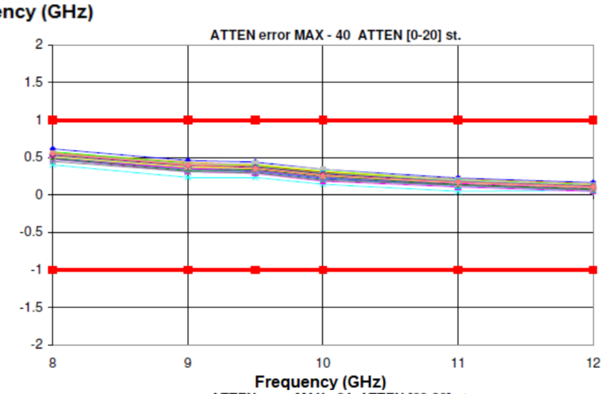


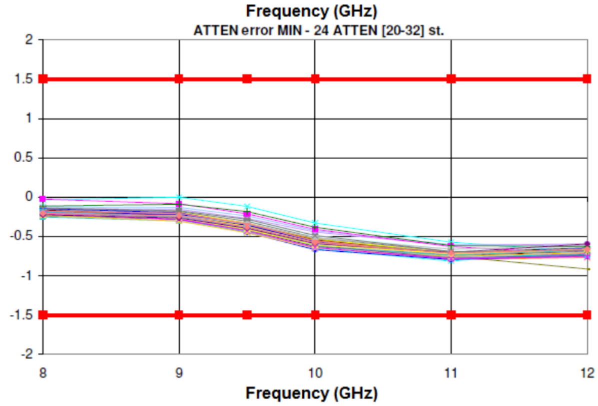


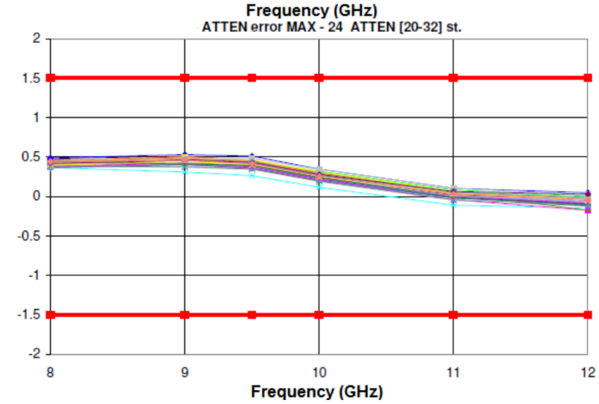
Typical Performance Curves: On Board Measurements—Attenuation Errors

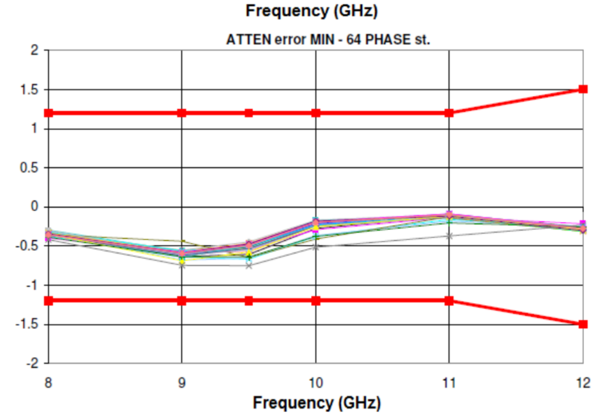


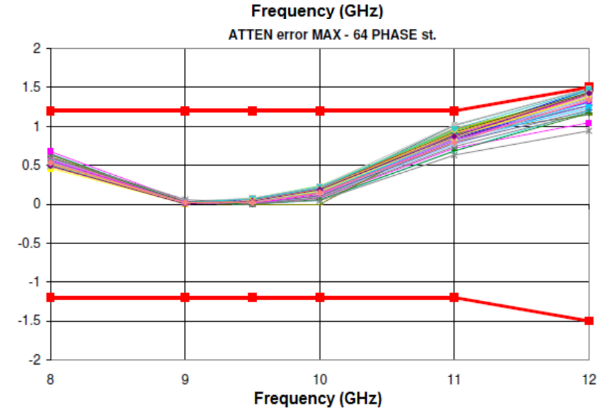




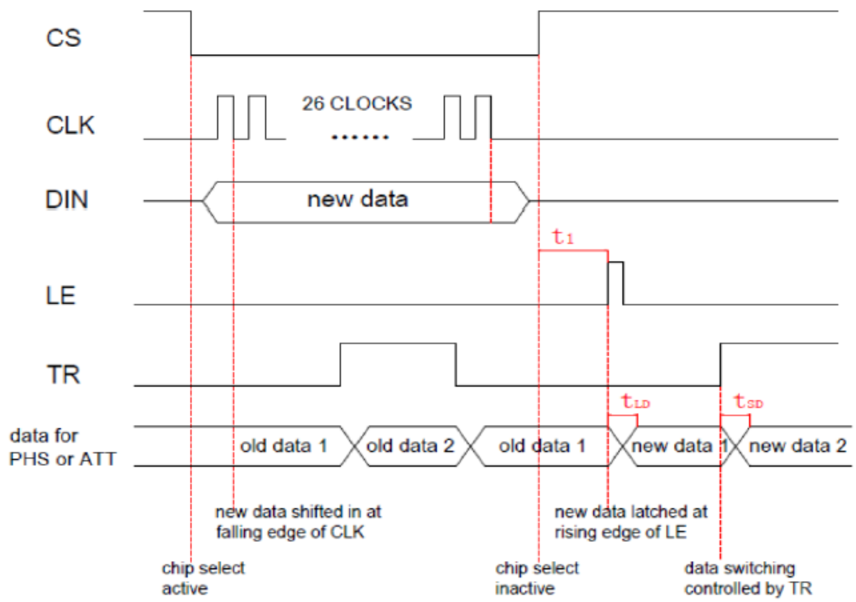








Timing Diagram



- The serial data input is controlled by falling edge of signal CLK and will be shifted into a 26-bit shift register and will be latched on LE rising edge and complete data update.

- The control data during transmit and receive are saved in two independent latches. Under the control of the T/R switch pulse, the control data will control phase shifter and attenuator with Time Division Multiplexing (TDM).

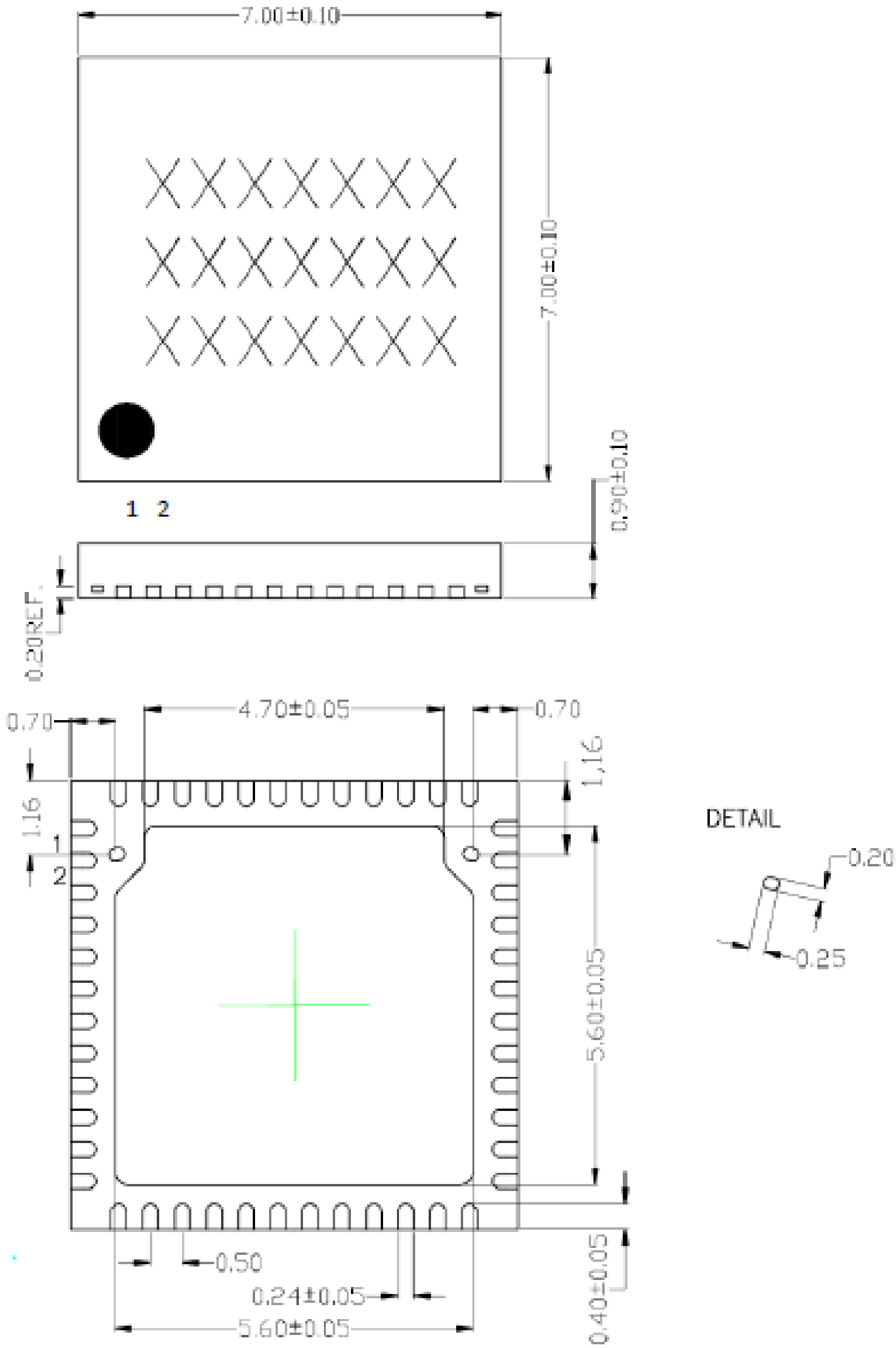
  new data 1: SR1~SR6 for PHS;ATR1~ATR6 for ATT(TR="0",in Rx mode).
  new data 2: ST1~ST6 for PHS;ATT1~ATT6 for ATT(TR="1",in Tx mode).

  The delay time [t1] is defined by the user.
  [tSD] : Tx/Rx switching time
  [tLD] : [tDU] data latching time

Switching Control

Voltage	Tx Mode	Rx Mode
Low (0 V)	—	T/R
High (3 V)	T/R	—

Mechanical Information



Mechanical Information[6]

Pin #	Symbol	Description
1,3,9,34,36, 42, 44	GND	Ground
2	RX_{IN}	Rx Input
4 - 8, 10 - 12, 29 - 33, 37 - 41, 45 - 48	NC	Not Connected
13	VD1	Drain Voltage Supply 1
14	VD2	Drain Voltage Supply 2
15	VD3	Drain Voltage Supply 3
16	VSS	Negative Supply Voltage
17	AT2	Input for external control of additional attenuator
18	VDN	Positive Supply Voltage
19	CLR	Clear function for register
20	LE	Latch Enable Input
21	DIN	Data Input
22	CLK	Clock Input
23	CS	Chip select
24	T/R	T/R switch pulse
25	VSN	Negative supply voltage
26	D_{OUT}	Data Output
27	STBRX	Rx standby control for exterior using
28	STBTX	Tx standby control for exterior using
35	TX_{OUT}	Tx Output
43	COM	COM

6. The RF bond wires or ribbon should be kept as short as possible. The RF lines should be 300 μm wide or less to minimize discontinuities associated with the connection to the MMIC bond pads.