Features

- Wide Frequency Range: 0.5 - 45 GHz
- Small Signal Gain: 12.7 dB
- Noise Figure: 2.6 dB @ 20 GHz
- Noise Figure Minimum: 1.8 dB @ 9 GHz
- Power Consumption: 420 mW
- Input Return Loss: >13.5 dB @ 20 GHz
- Output Return Loss: >16.5 dB @ 20 GHz
- P1dB: 18 dBm @ 20 GHz
- Chip Size: 1850 x 1060 µm
- 100% RF Tested, Inspected Known Good Die
- Space & MIL-STD Available
- RoHS* Compliant

Applications

- Radar
- Space
- Telecommunication
- Instrumentation
- General Purpose Wide Band Amplifier

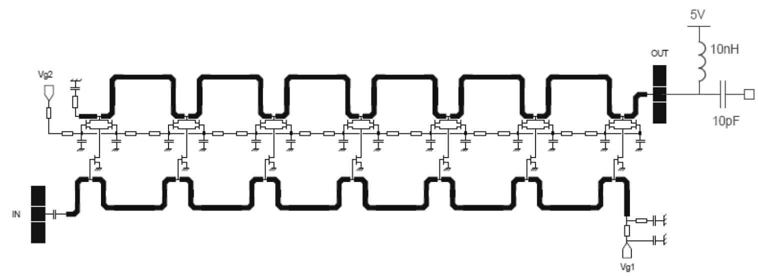
Description

The CGY2145UH/C1 is a GaAs very wide band low noise amplifier MMIC. This amplifier has a low noise figure of 2.6 dB and a P1dB of 18 dBm at 20 GHz. This LNA exhibits a small signal gain of 12.7 dB from 100 MHz to 28 GHz and >12 dB up to 44 GHz.

This device features single-ended input and output and operates with a 5 V supply voltage via an external bias tee.

The MMIC is manufactured using the qualified 0.13 µm pHEMT GaAs D01PH technology. The D01PH process has been evaluated for Space applications and is on the European Preferred Parts List of the European Space Agency.

Block Diagram



Ordering Information

Part Number	Package
CGY2145UH/C1	Die

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

DC Electrical Specifications: Freq. = 0.5 - 45 GHz, V_{DD} = 5 V, R_L = 50 Ω, T_A = +25°C

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Supply Voltage	—	V	+4.75	+5.00	+5.25
Supply Current	—	mA	—	85	90
Gate Supply Voltage 1	See note 1	V	-3.0	-0.3	0.0
Gate Supply Voltage 2	—	V	0.0	+3.0	+3.0

1. VG1 determines the typical drain current. VG1 should be raised from -3 V until the drain DC current reaches 85 mA.

AC Electrical Specifications: On Wafer, Freq. = 0.5 - 45 GHz, V_{DD} = 5 V, V_{G2} = 2.3 V, V_{G1} = -0.3 V, I_{DD} = 85 mA, RL = 50 Ω, T_A = +25°C

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Reference Gain	3 GHz[2]	dB	—	12.6	—
Gain Ripple[3]	100 MHz - 35 GHz 35 GHz - frequency cutoff	dB	-0.6 -1.0	—	+1.5 —
Frequency Cutoff	High (Gain 3 GHz - 3 dB) Low (See note 4)	GHz kHz	44 —	46 —	— 50
Input Return Loss	100 MHz - 22 GHz 22 - 35 GHz 35 - 45 GHz	dB	—	-16.0 -14.0 -11.5	-13.5 -12.0 -10.0
Output Return Loss	100 MHz - 30 GHz 30 - 40 GHz 40 - 45 GHz	dB	-35 — —	-16 -13 -14	-15 -10 -12
Noise Figure	5 - 35 GHz	dB	—	<4.5	—
Output P1dB	1 - 30 GHz	dBm	—	18	—
Microwave Stability Factor	-10°C to +85°C, All passive source and load	-	1.2	—	—

2. Measurement is guaranteed by correlation down to the lower frequency cut-off. 3 GHz is specified as a reference for convenience of measurement.
3. Low frequency gain ripple assumes the use of drain decoupling close to the chip, as proposed on the bonding pattern.
4. The input and output are DC coupled. The low frequency cut-off is set by the choice of the input blocking capacitor or by the output bias tee used for drain current supply voltage.

Absolute Maximum Ratings[5,6]

Parameter	Absolute Maximum
Supply Voltage	-0.5 V to +8.0 V
Supply Current	240 mA
Gate Voltage 1	-5 to 0 V
Gate Voltage 2	-5 to +5.0 V
Junction Temperature	+150°C
Operating Temperature	-10°C to +85°C
Storage Temperature	-55°C to +150°C

5. Exceeding any one or combination of these limits may cause permanent damage to this device.
6. MACOM does not recommend sustained operation near these survivability limits.

Handling Procedures

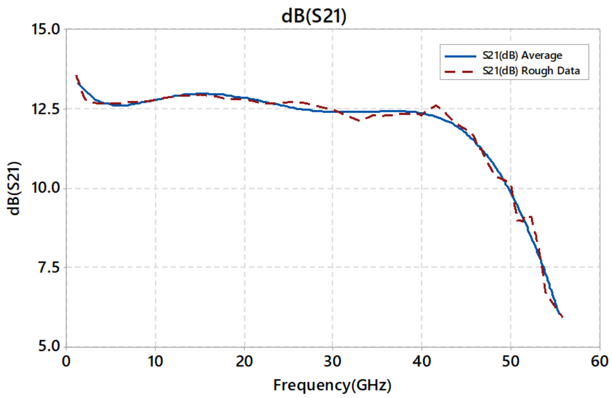
Please observe the following precautions to avoid damage:

Static Sensitivity

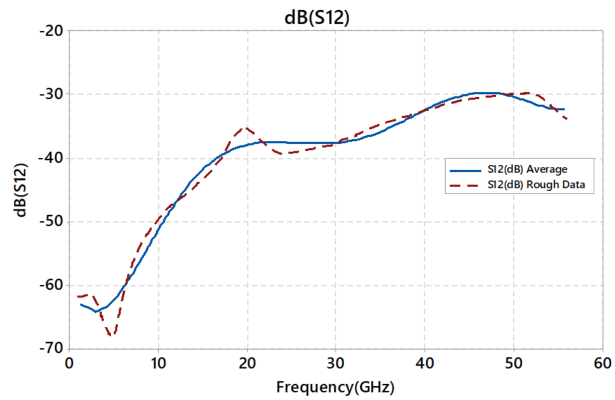
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Typical Performance Curves: On Wafer, V_{DD} = 5 V, V_{G2} = 2.3 V, I_{DD} = 85 mA, T_A = +25°C

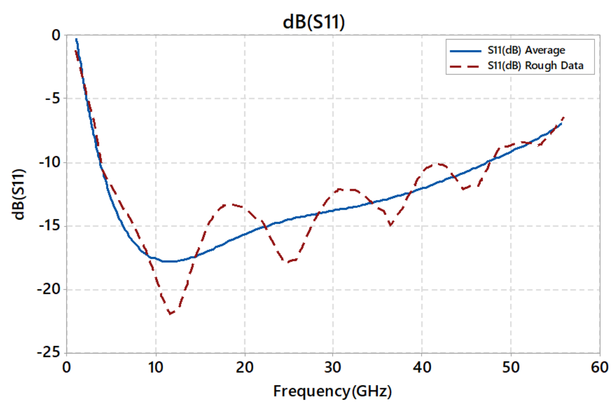
Gain



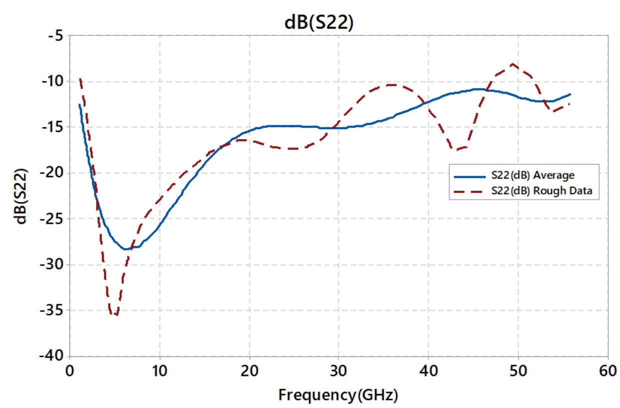
Reverse Isolation



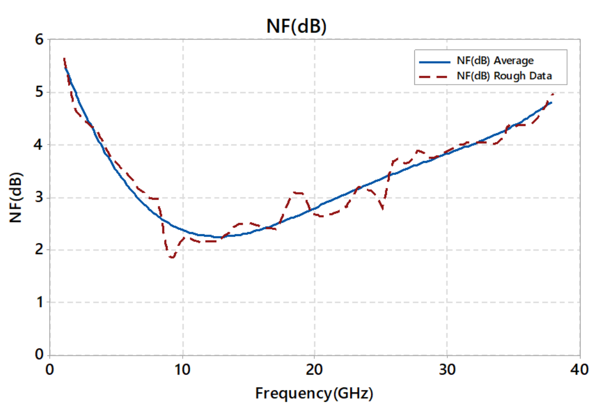
Input Return Loss



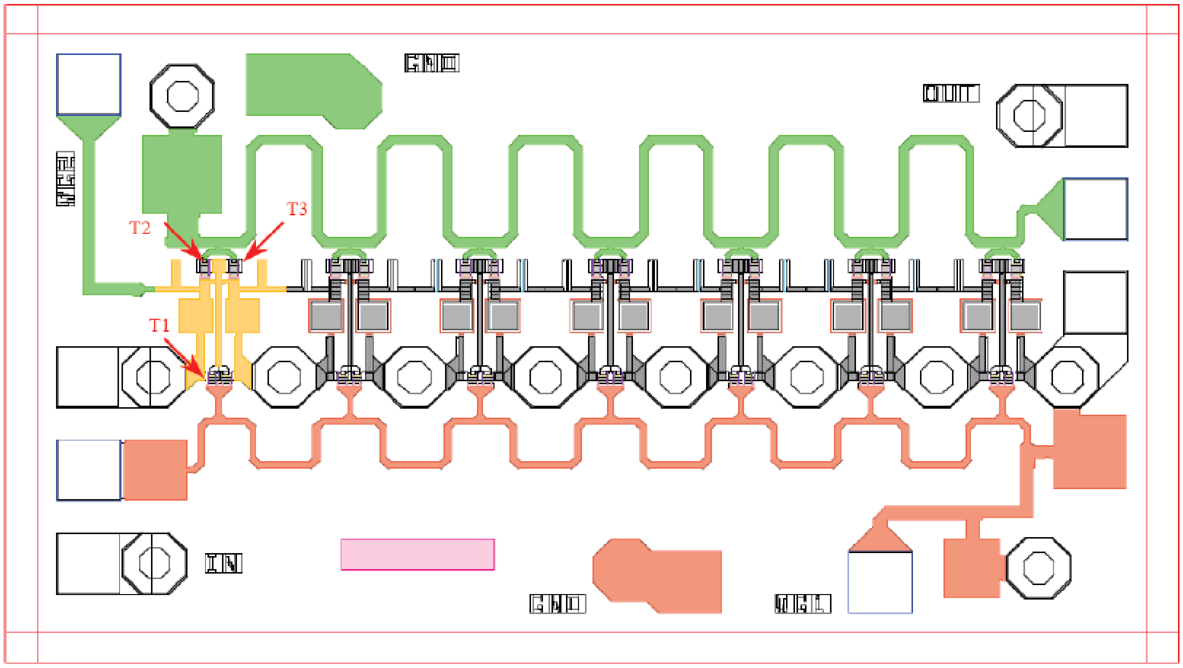
Output Return Loss



Noise Figure



Application Information: Bonding Pattern



Operating & Handling Instructions

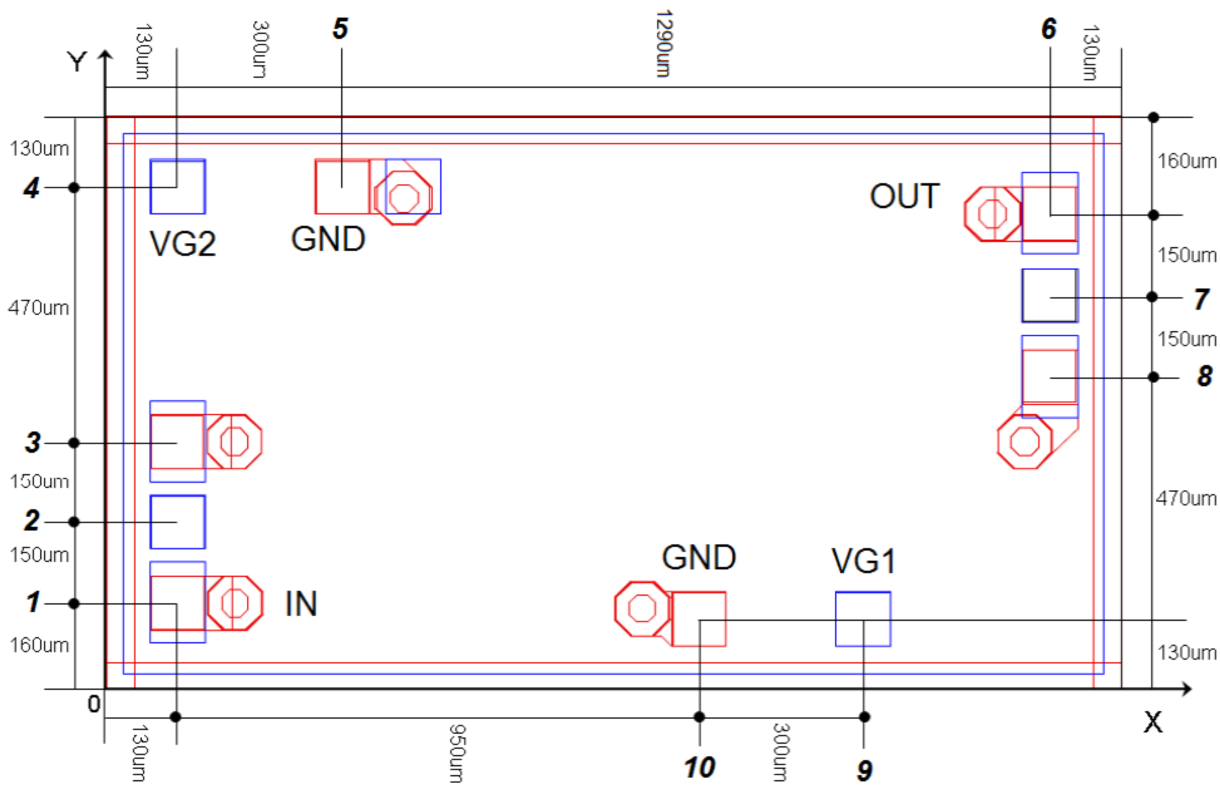
This device is a very high performance GaAs device and as such, care must be taken at all times to avoid damage due to inappropriate handling, mounting, packaging and biasing conditions.

1- Power Supply Sequence

The following power supply sequence is recommended.

a) Make sure the transient peaks from DC supply voltages do not exceed the limiting values.
b) Pinch off the device by setting Vg1 to –4.5 V and Vg2 to 0.0 V.
c) Increase Vdd = 5.0 V while monitoring the drain current.
d) Increase Vg2 to 2.3 V
e) Increase Vg1 slowly from -3 V until the drain current reaches 84 mA.
f) Apply the RF input signal.

Mechanical Information



Chip Size = 1850 x 1060 µm (Tolerance ±15 µm)
GND, V_{G1}, V_{G2}, IN, OUT Pads = 100 x 100 µm
Chip Thickness = 100 µm
Backside Metal = TiAu
Passivation: PECVD deposited Si_3N_4

Pad Position[7]

Pad Name	Pad#	Coordinate		Description
		X	Y	
GND	1	160	130	Connected to ground with on-chip via holes
IN	2	310	130	RF Input
GND	3	460	130	Connected to ground with on-chip via holes
V_{G2}	4	930	130	Gate Supply Voltage 2, must be decoupled to ground using external capacitors
GND	5	930	430	Connected to ground with on-chip via holes
GND	6	900	1720	Connected to ground with on-chip via holes
OUT	7	750	1720	RF Output
GND	8	600	1720	Connected to ground with on-chip via holes
V_{G1}	9	130	1380	Gate Supply Voltage 2, must be decoupled to ground using external capacitors
GND	10	130	1080	Connected to ground with on-chip via holes

7. X = 0, Y = 0 at bottom left corner.