Ultra Low Noise Amplifier, C-Band
5 - 7 GHz

Features

- Noise Figure: 0.5 dB @ 6 GHz
- Gain: 13.2 @ 6 GHz
- Input Return Loss: 6 dB @ 6 GHz
- Output Return Loss: 12 dB @ 6 GHz
- Chip Size: 1.5 x 2.0 mm
- 100% Tested, Inspected Known Good Die
- Samples Available
- RoHS* Compliant

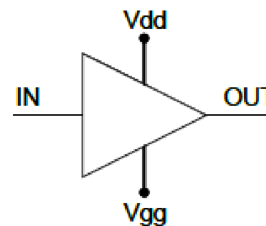
Applications

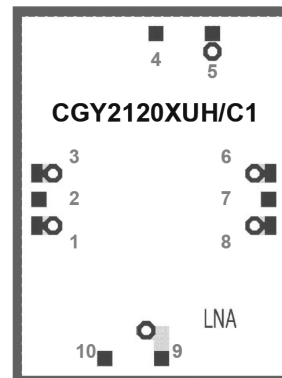
- Radar
- Telecommunication
- Instrumentation

Description

The CGY2120XUH/C1 is a high performance GaAs single stage low noise amplifier MMIC designed to operate on the C band. This device has an exceptionally low noise figure of 0.5 dB with 13 dB of gain.

The die is manufactured using an advanced 70 nm gate length high Indium content MHEMT technology. The MMIC uses gold bonding pads and backside materialization and is fully protected with Silicon Nitride passivation to obtain the highest level of reliability.





Pad Configuration[1]

Pad	Function
1,3,5,6,8,9	Ground
2	RF Input
4	Drain Supply Voltage
7	RF Output
10	Gate Supply Voltage

1. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

Ordering Information

Part Number	Package
CGY2120XUH/C1	Die

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

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Electrical Specifications: On Wafer Measurements, using 50 Ω probes
Freq. = 5 - 7 GHz, T_A = +25°C, V_{DD} = +1 V, V_{GG} = -0.15 V, I_{DD} = 50 mA

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	6 GHz	dB	—	13.2	—
Noise Figure	6 GHz	dB	—	0.5	—
Input Return Loss	50 Ω	dB	6.0	6.8	—
Output Return Loss	50 Ω	dB	6.0	12.0	—
Reverse Isolation	—	dB	—	-19	—
Output P1dB	—	dBm	—	12	—

Absolute Maximum Ratings[2,3]

Parameter	Absolute Maximum
Gate Voltage	-2.5 to 0 V
Drain Voltage	0 to +1.2 V
Drain Current	60 mA
Junction Temperature	+150°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +150°C

2. Exceeding any one or combination of these limits may cause permanent damage to this device.
3. MACOM does not recommend sustained operation near these survivability limits.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

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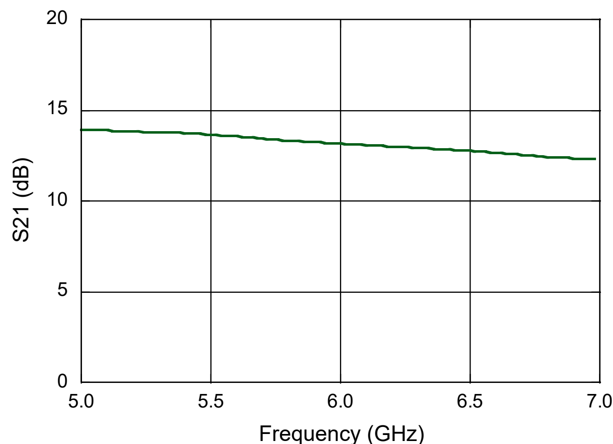
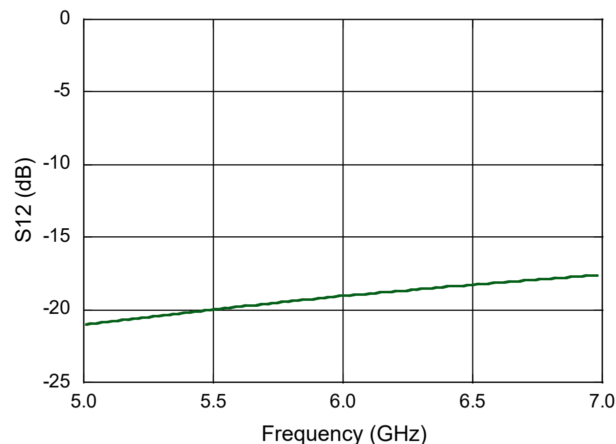
Typical Performance Curves: On Wafer Measurements, using 50 Ω Probes

V_{DD} = 1 V, I_{DD} = 50 mA, T_A = +25°C

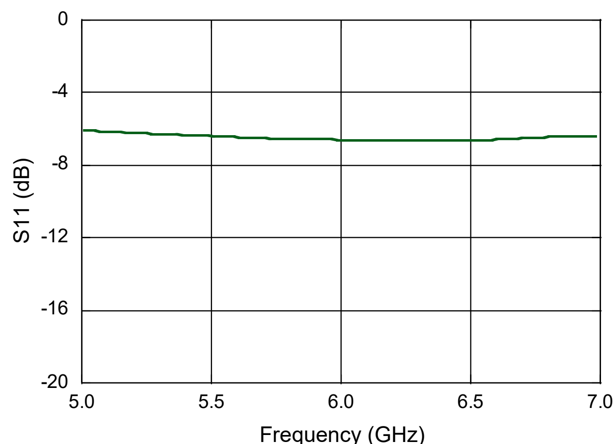
Gain



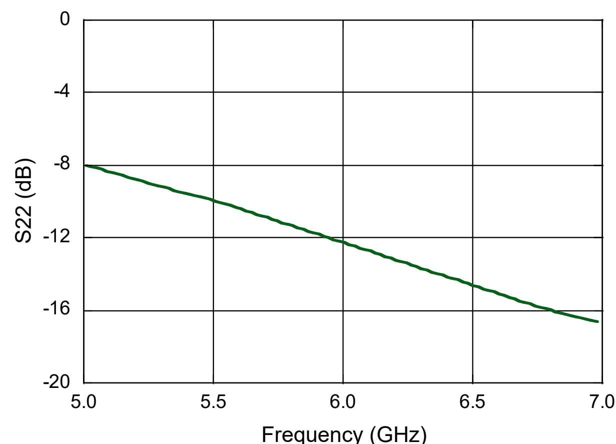
Isolation



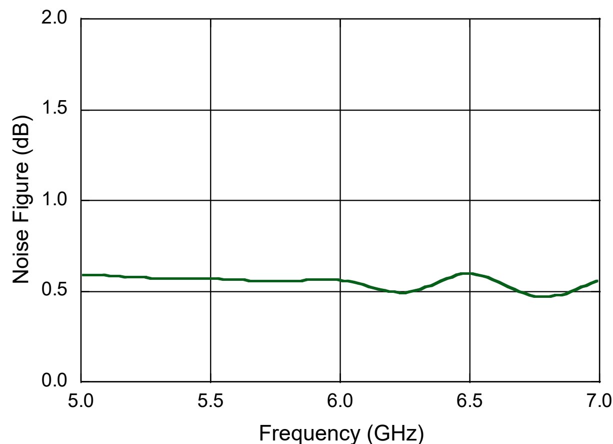
Input Return Loss



Output Return Loss



Noise Figure



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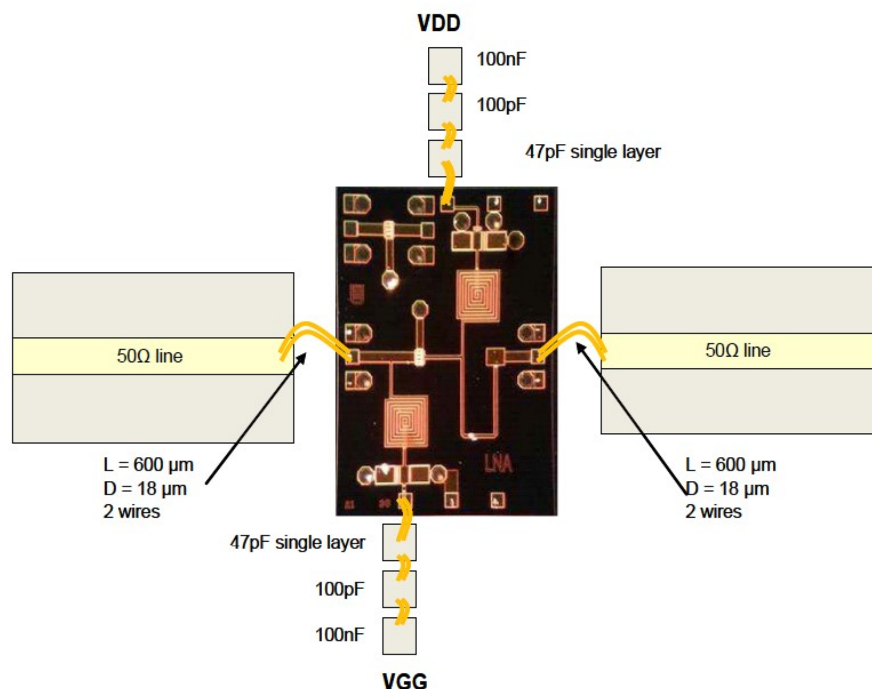
Application Schematic

A reference module layout is shown below, where RF input and output microstrip transmission lines are used. However, coplanar transmission lines with similar performance may also be used. All path lengths and physical sizes of the components should be minimized.

All RF input and output bonding inductances should be minimized to give the best performance. Overall wire length should be kept as small as possible to reduce parasitic inductance. Higher RF input / output inductance may result in a degradation of gain and match. Ribbon bonding technique can also be used. All others bondings (pads V_{DD} and V_{GG}) should be kept as short as possible.

Decoupling 47 pF and 100 pF chip capacitors (close to the chip) and 100 nF chip or surface mount device capacitors (positioned at around 4 mm from the chip) are used to improve the power supply rejection.

The chip itself has via holes connecting the front side to the back side of the chip. A good RF grounding connection should be maintained between the backside of the chip and system ground. It is extremely important to use an uninterrupted ground plane. AuSn or silver conductive epoxy material can be used for die attachment.



Operating and Handling Instructions

The CGY2120XUH/C1 is a very high performance MHEMT device and as such, care must be taken at all times to avoid damage due to inappropriate handling, mounting and biasing conditions.

1- Power Supply Sequence

The following power supply sequence is recommended:

a) Make sure the transient peaks from DC supply voltages do not exceed the limiting values.
b) Pinch off the device by setting V_{GG} to -2 V.
c) Increase V_{DD} to +1 V
d) Increase the gate voltages V_{GG} from -2 V until the drain current reaches 50 mA.
e) Apply the RF input signal.

2- Mounting and ESD handling precautions

For high performance Integrated Circuits, such as the CGY2120XUH/C1, care must be taken when mounting GaAs MMICs so as to correctly mount, bond and hence obtain the most reliable long-term operation.

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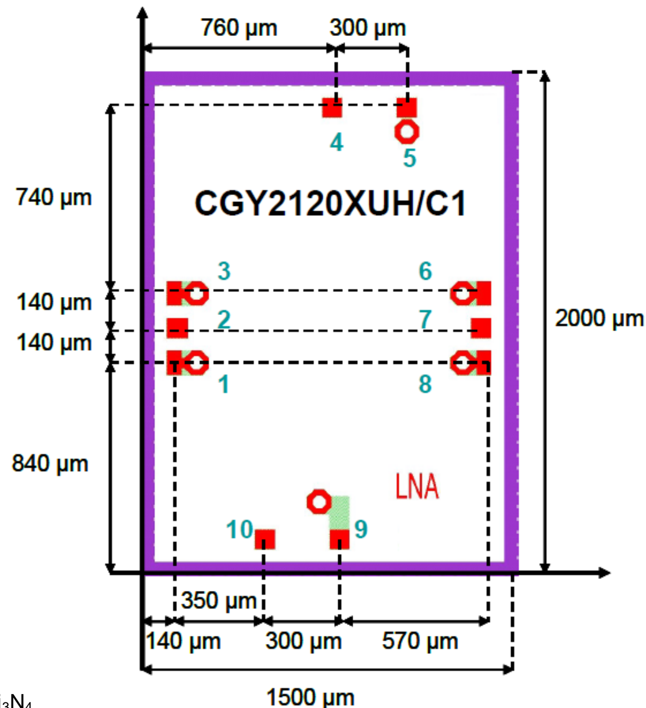
Die Layout



Chip Size = 1500 x 2000 µm
DC Pads = 80 x 100 µm
RF Pads = 80 x 80 µm
Chip Thickness = 100 µm
Backside Material = TiAu
Passivation = PECVD deposited onSi_3N_4

Bonding Pad Coordinates

Pad #	Pad	X Coordinate	Y Coordinate	Description
1	GND	140	840	Connected to ground with on-chip via hole
2	RF_{IN}	140	980	RF Input
3	GND	140	1120	Connected to ground with on-chip via hole
4	V_{DD}	760	1860	Drain supply voltage must be decoupled to ground using external capacitor(s)
5	GND	1060	1860	Connected to ground with on-chip via hole
6	GND	1360	1120	Connected to ground with on-chip via hole
7	RF_{OUT}	1360	980	RF Output
8	GND	1360	840	Connected to ground with on-chip via hole
9	GND	790	140	Connected to ground with on-chip via hole
10	V_{GG}	490	140	Gate supply voltage must be decoupled to ground using external capacitor(s)

The die size and all pad positions refer to the mask layout, with (X=0, Y=0) at the bottom left corner of the layout.
For each pad, the (X,Y) coordinates refer to the center of the pad.
Wafers are diced by sawing, with a sawline width of 35 µm (±5 µm). A misalignment of the sawline with the middle of the dicing street (± 20 µm on all sides) may also result in a variation of ±20 µm of the actual positions of the pads on the diced chip and an additional tolerance of ±40 µm on the die size.

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