Transimpedance Amplifier, 10 Gb/s

CGY2110UH/C1
Rev. V1

Features

- Suitable for 10 Gb/s Optical Fiber Links
- Single Supply Voltage: 5.7 V
- Differential Transimpedance Gain: 72 dBΩ
- Differential Output
- Low Power Consumption: 400 mW
- Tested, Inspected Known Good Die (KGD)
- Samples Available
- Demonstration Boards Available
- Space and MIL-STD also Available
- RoHS* Compliant

Applications

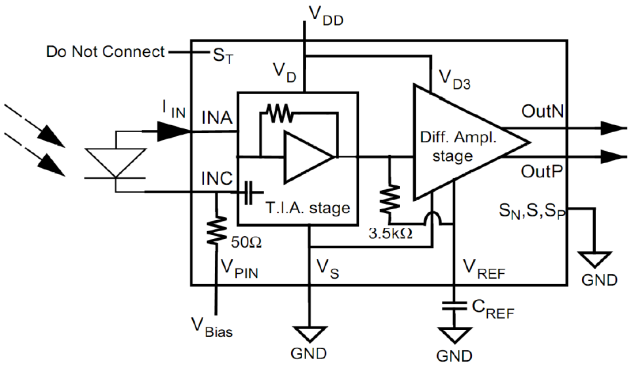
- Digital Fiber Optic Receiver for Optical Telecommunications (STM64 or OC192 systems)
- High Sensitivity & High Gain Amplifier

Description

The CGY2110UH/C1 is a 10 Gb/s TransImpedance Amplifier (TIA). Typical use is as a low noise preamplifier for lightwave receiver modules in optical fiber networks. The device is intended to be used with a PIN or APD photodetector and is capable of amplifying input current up to 2 mA p.p. at BER of 10^{-12}.The circuit also exhibits exceptional sensitivity. A biasing circuit for PIN photodiode is integrated in the CGY2110UH.

The die is manufactured using 0.18 µm gate length pHEMT technology. The MMIC uses gold bond pads and backside metallization and is fully protected with silicon nitride passivation to obtain the highest level of reliability. This technology has been evaluated for Space applications and is on the European Preferred Parts List of the European Space Agency.

Block Diagram



Ordering Information

Part Number	Package
CGY2110UH/C1	10 Gb/s transimpedance amplifier

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

DC Characteristics:

Minimum/Maximum values are defined at V_{DD} = 5.7 V ± 0.3 V, T_A = -10°C to +85°C; Typical data is defined at T_A = 25°C, V_{DD} = 5.7 V ; unless otherwise stated.

Parameter	Units	Min.	Typ.	Max.
Supply Current	mA	40	70	100
DC Input Voltage (IN Pad)	V	—	1.35	—
DC Output Voltage Level	V	—	3.5	—
Voltage Offset Between the 2 Outputs	V	-0.7	—	+0.7

AC Characteristics:

All measured data is at V_{DD} = 3.3 V; T_A = 25°C; RL = 50 Ω. The TIA is measured on-wafer using RF probes. AC characteristics are guaranteed for both OUTP and OUTN ; Unless otherwise stated.
C_P = 0.22 pF, L_B = 0.6 nH, R_S = 8 Ω

Parameter	Conditions	Units	Min.	Typ.	Max.
Low Frequency Transimpedance Gain	100 MHz, single ended 100 MHz, differential	dBΩ	62 —	66 72	70 —
Transimpedance Ripple	1 MHz - 3 GHz 3 GHz - 6 GHz 6 GHz - 10 GHz	dBΩ	-1.5 -1.5 —	0 1 —	+1.5 +3.0 +3.0
Transimpedance Cut-Off Frequency	$\|Z_T\| = \|Z_T\|_{LF}$ –3 dB $\|Z_T\| = \|Z_T\|_{LF}$ –3 dB, C_P = 0.14 pF	GHz	8 —	9.0 10.1	—
Low Frequency Cut-Off	AC Coupled at All Outputs (see note 1)	KHz	—	—	32
Group Delay, relative to 2.5 GHz	1 - 3 GHz 4 GHz 5 GHz 6.5 - 9 GHz	Ps	-20 -10 0 +15	—	20 35 50 75
Maximum Peak Input Current	Before Input Overload	mApp	2	—	—
Output Reflection Coefficient[2]	100 MHz - 10 GHz	dB	—	-15	-10
Total integrated input RMS noise	1 - 4 GHz 7 GHz 10 GHz, CP = 0.14 pF	pA/Hz	—	4.7 6.5 8.0	7 10 —
Optical Input Sensitivity	10 MHz - 8 GHz 10 MHz - 10 GHz, CP = 0.14 pF	nA	—	450 500	650 —
Output Load Termination	OUTN, OUTP	Ω	—	50	—

1. The CGY2110UH is AC coupled at its outputs via an external capacitor, C. So the lower cut-off frequency is determined by the time constant RC, where R is the 50 Ω load. Assuming that C is 100 nF, the lower cutoff frequency is given by : Fc_low = 1/(2*pi*R*C) = 32 kHz.
2. The |S22| specification given in this table is based on RF on-wafer measurements with low-inductance probes.

Absolute Maximum Ratings[1,2]

Parameter	Absolute Maximum
Supply Voltage	-0.5 V to +8.0 V
Photodiode Biasing Voltage	-15 V to +15 V
Input Average Photo Current[3]	-1 mA to +6 mA
Junction Temperature	+150°C
Storage Temperature	-55°C to +150°C

1. Exceeding any one or combination of these limits may cause permanent damage to this device.
2. MACOM does not recommend sustained operation near these survivability limits.
3. The specification is valid only if the photodiode is biased through the TIA chip.

Operating Conditions

Parameter	Absolute Maximum
Supply Voltage[3]	+5.4 V to +6.0 V
Junction Temperature	+150°C
Operating Temperature	-10°C to +85°C
Input Interface	DC Coupled
Output Interface	AC Coupled

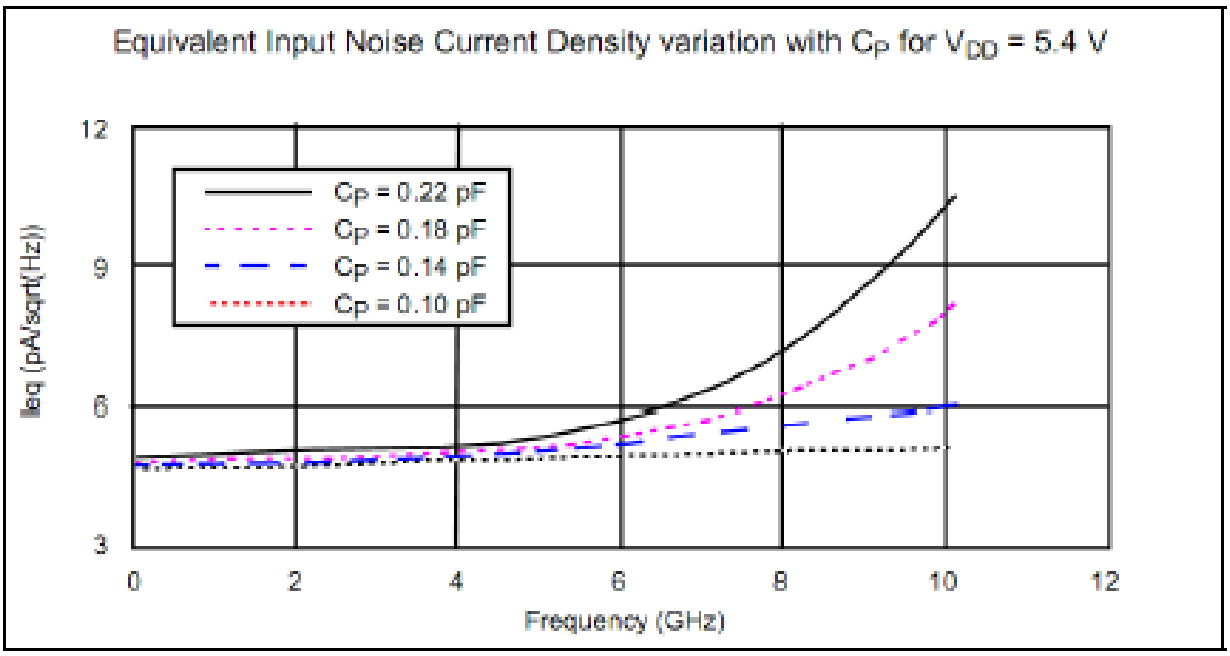
Handling Procedures

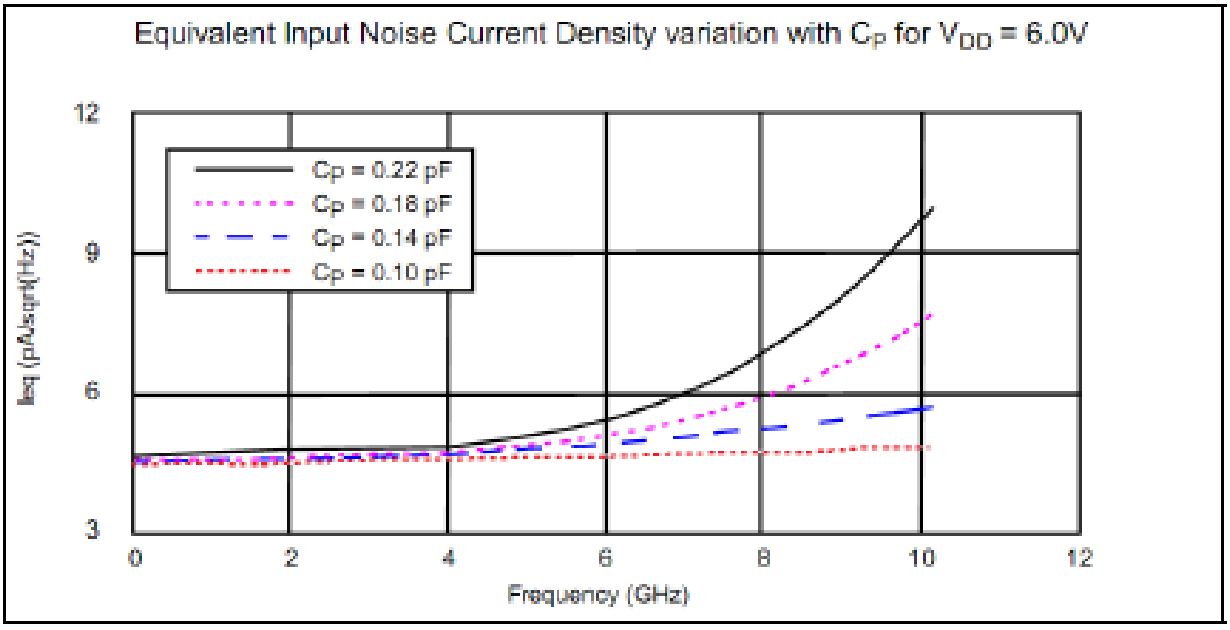
Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Typical Performance Curves:





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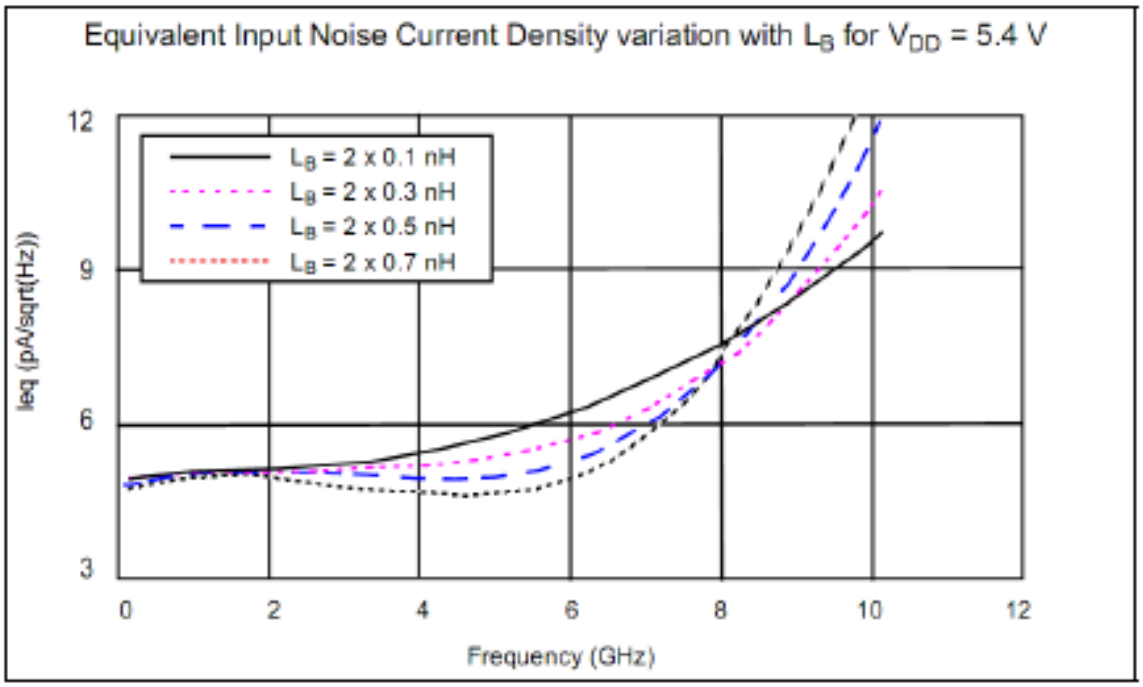

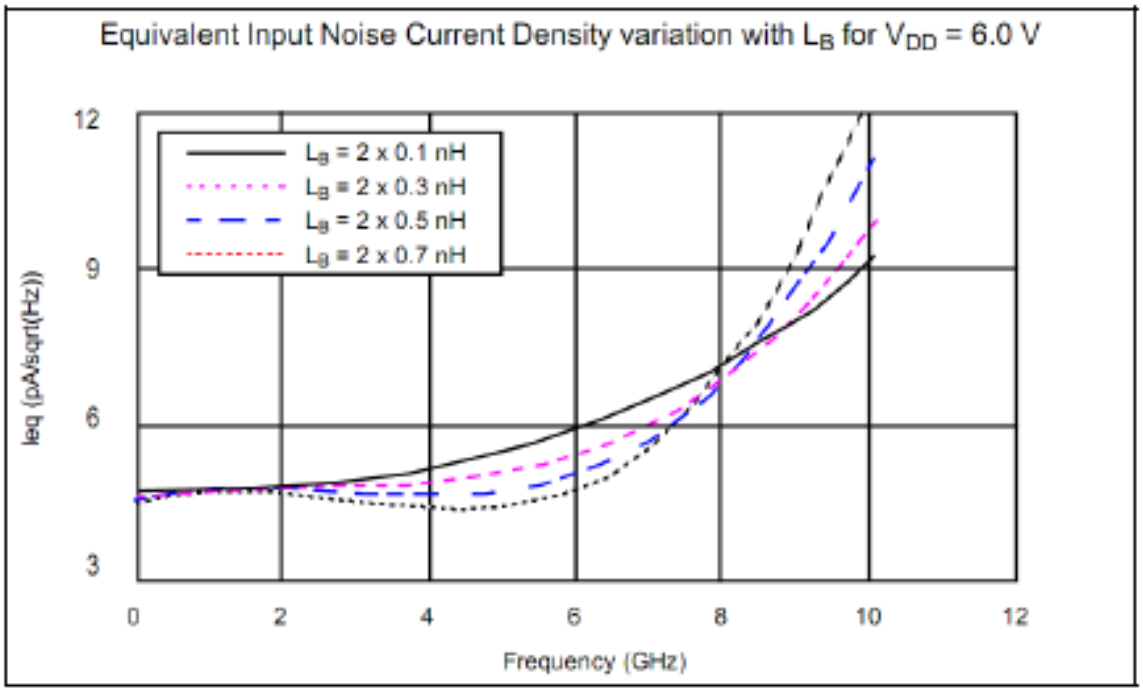

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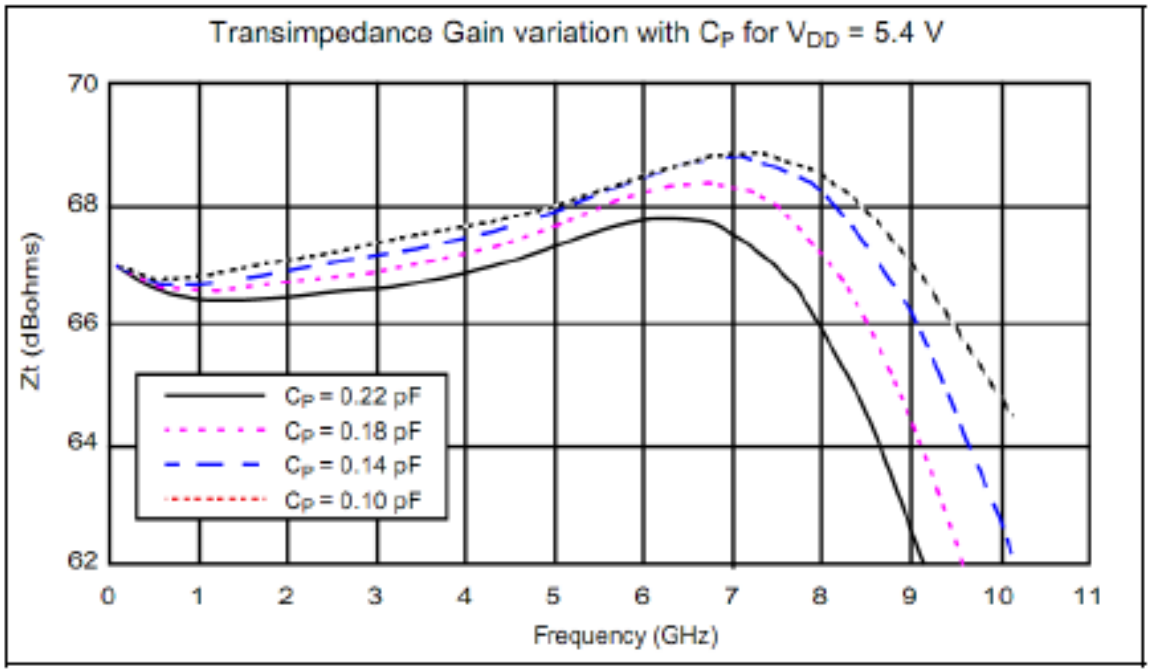

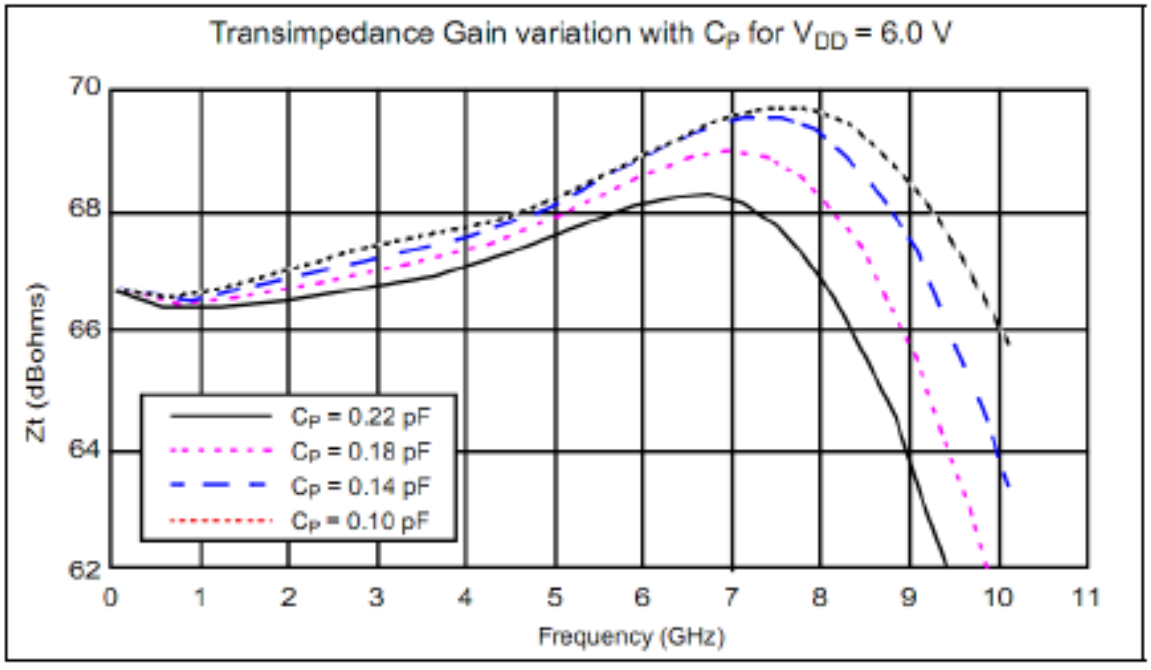

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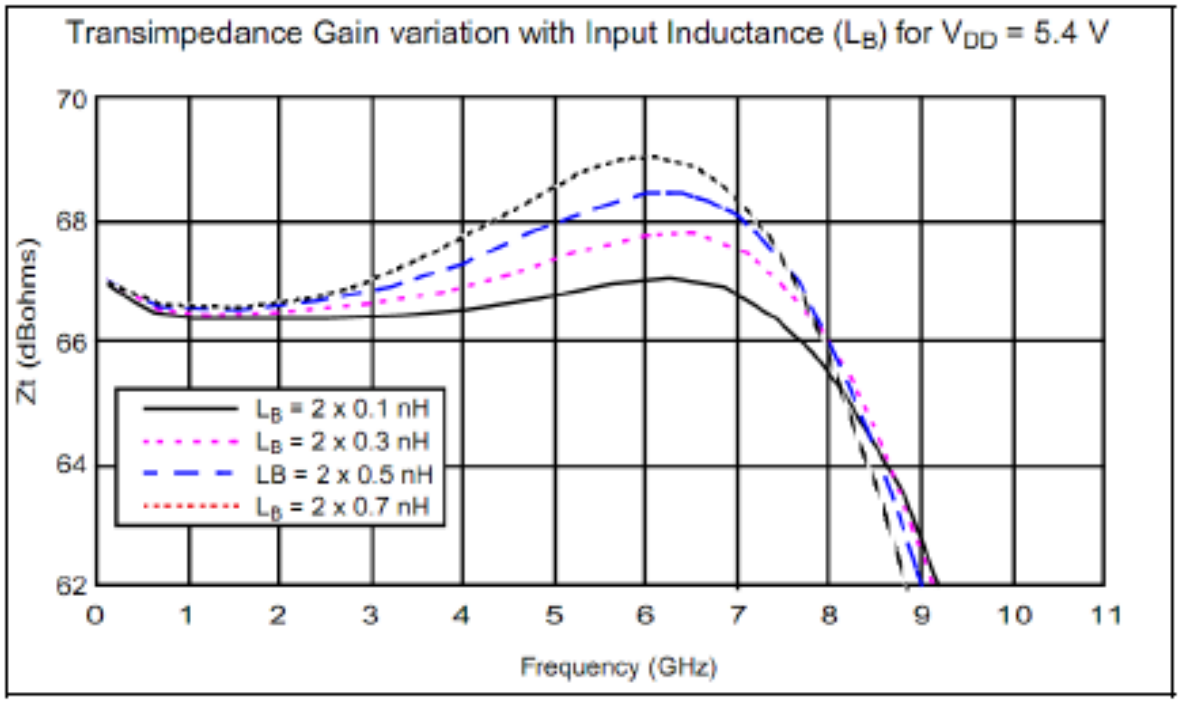
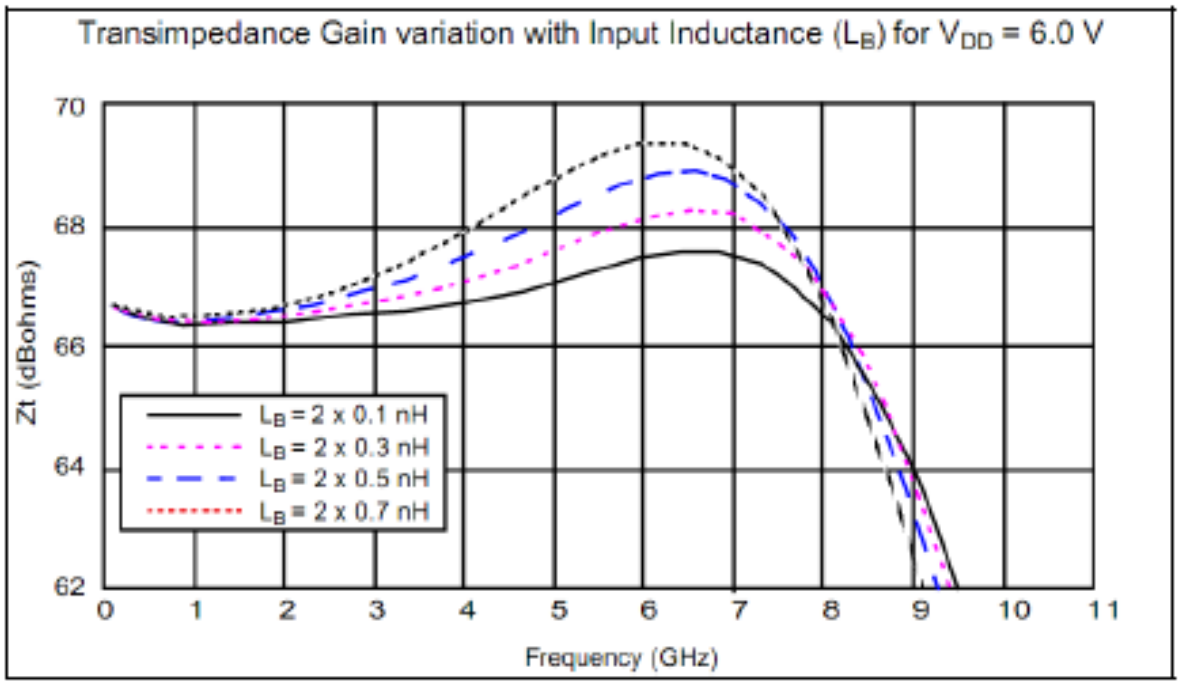
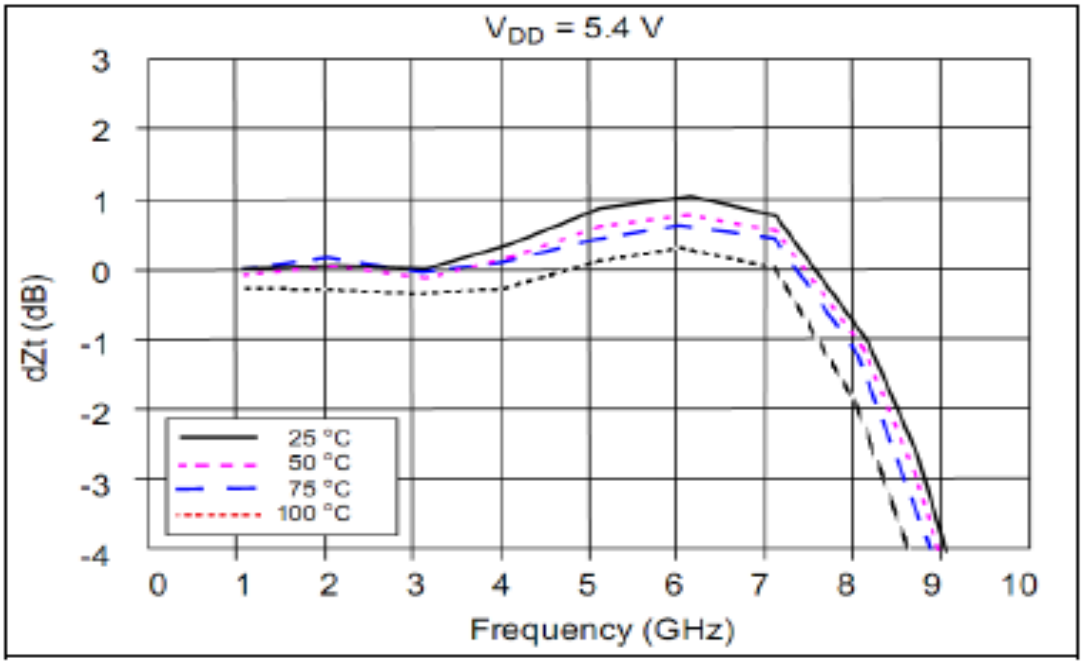
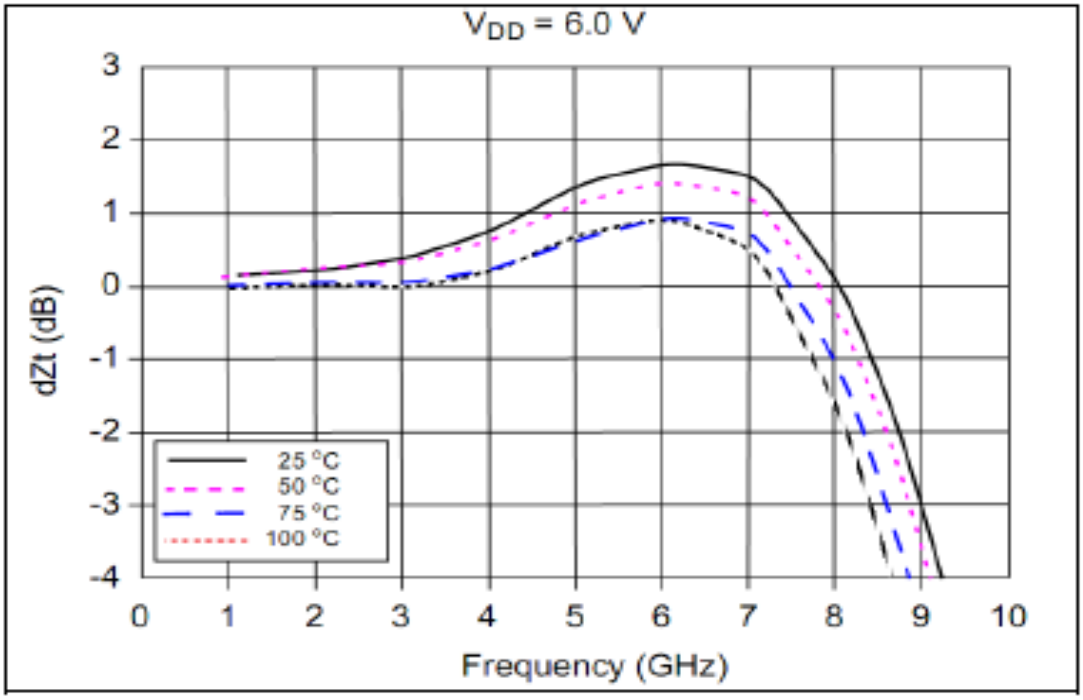




Typical Performance Curves:





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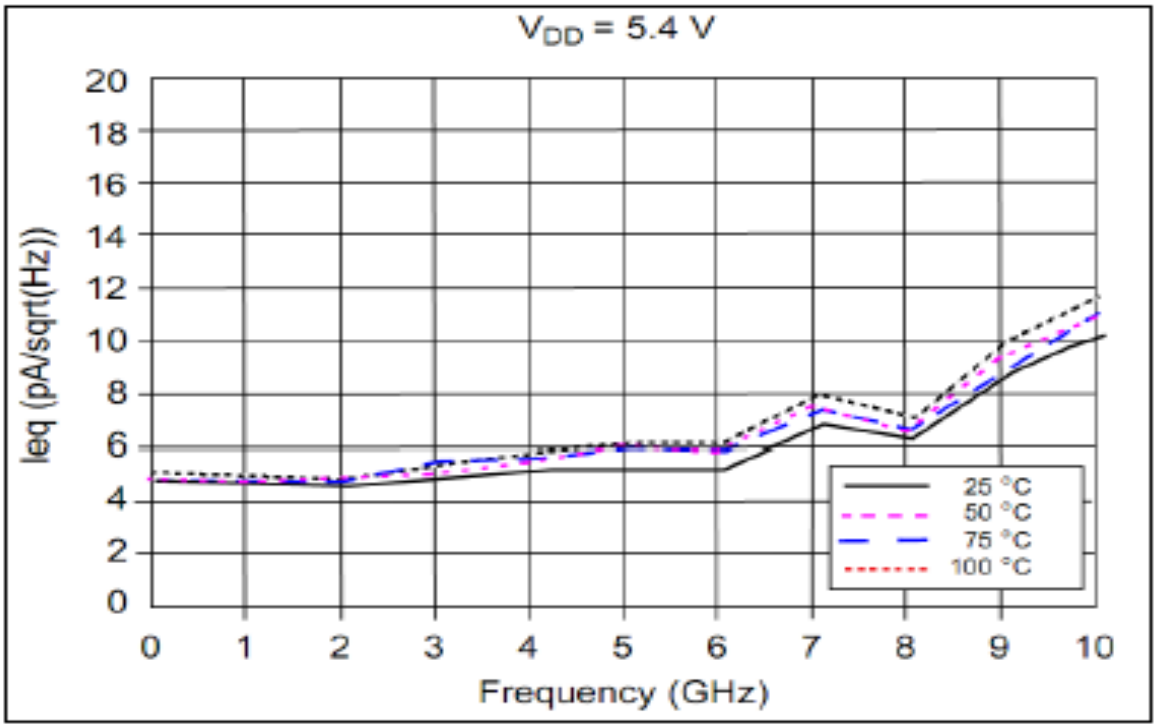
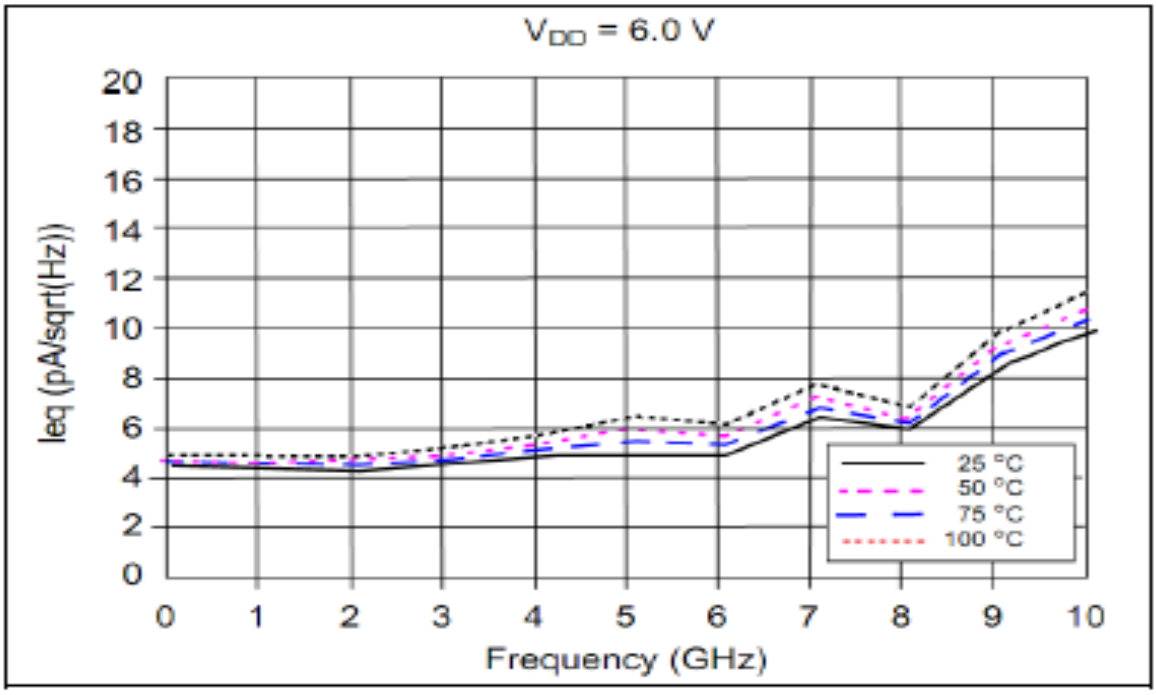
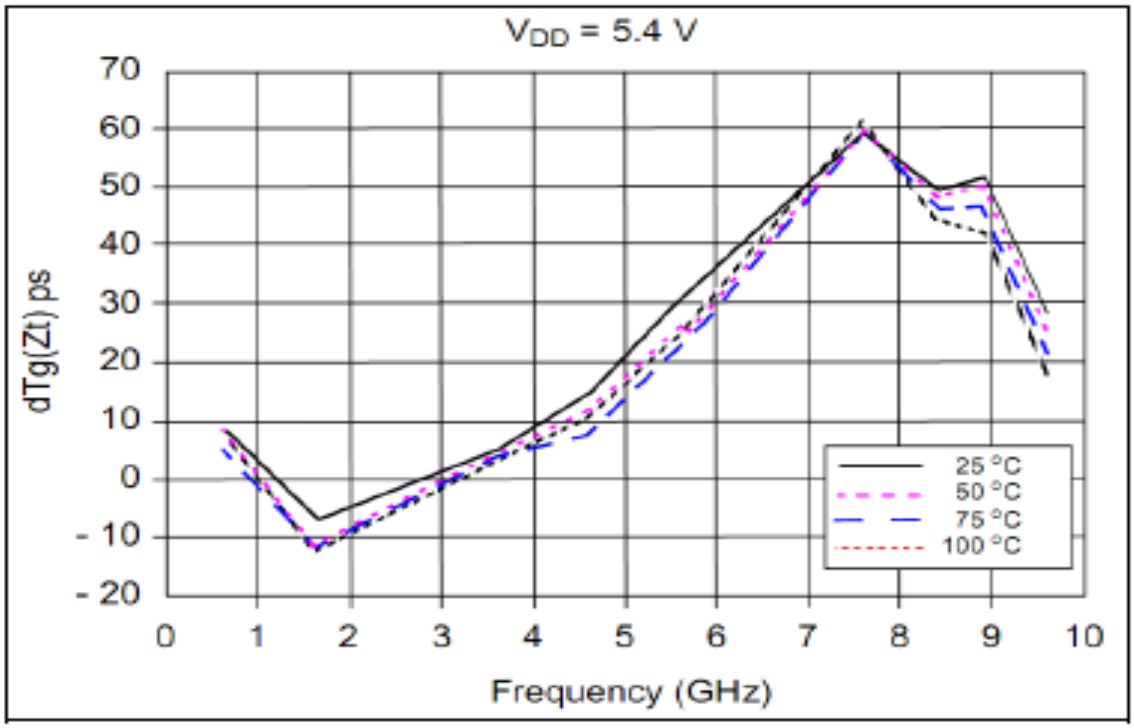
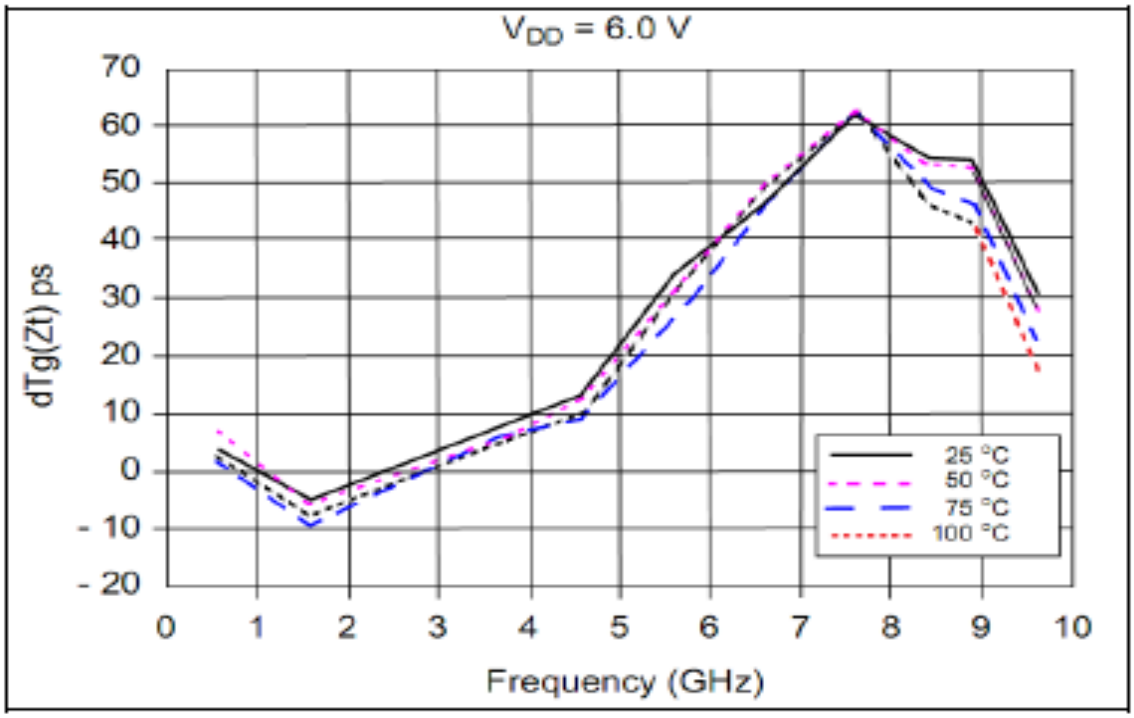




Typical Performance Curves:





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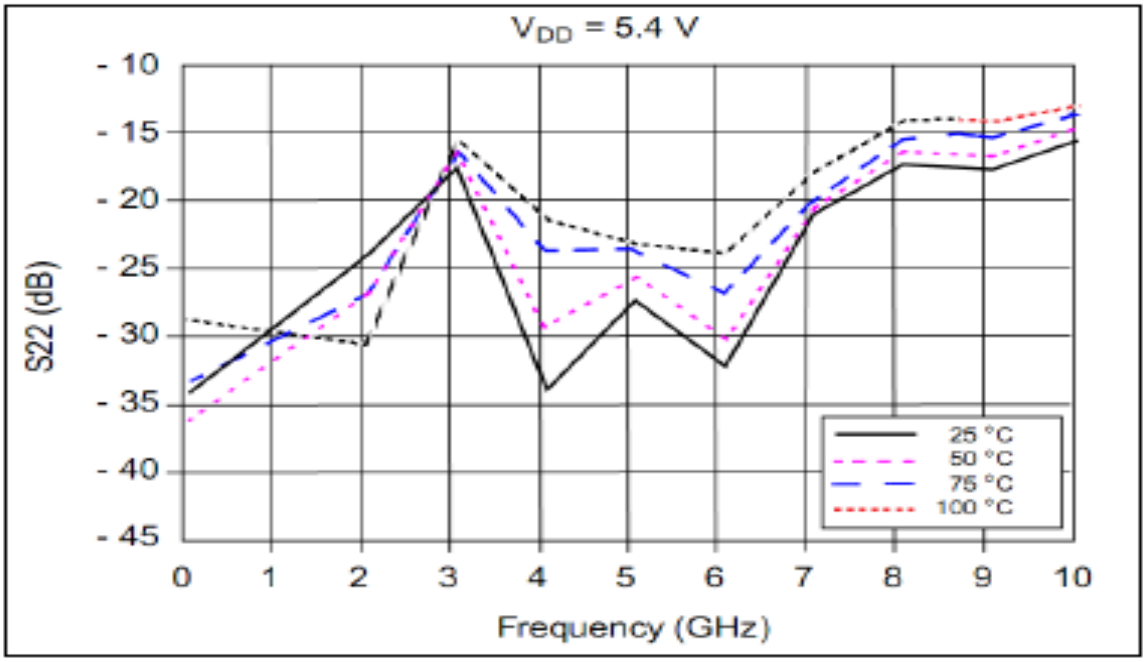
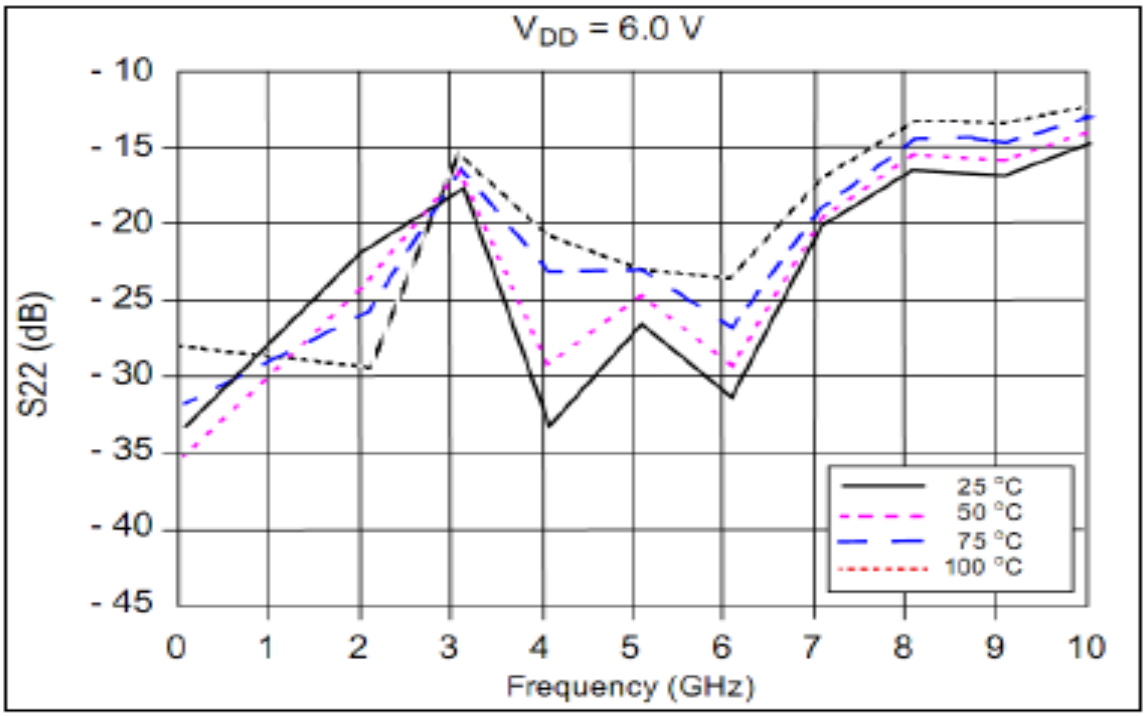




OPERATING AND HANDLING INSTRUCTIONS
The CGY2110UH/C1 is a very high performance GaAs device and care must be taken at all times to avoid damage due to inappropriate handling, mounting and biasing conditions.

Power Supply Sequence :
The following power supply sequence is recommended:

V_{BIAS} : Photodiode bias
V_{DD} : TIA bias

a) Always turn on the photodiode bias Vbias first or simultaneously with VDD. Since the photodiode is direct coupled to the TIA input, powering VDD first can damage the photodiode through forward bias and excess current.
b) Apply the input optical signal.

It is important to apply the DC voltage from ground, then increases them to their desired values.

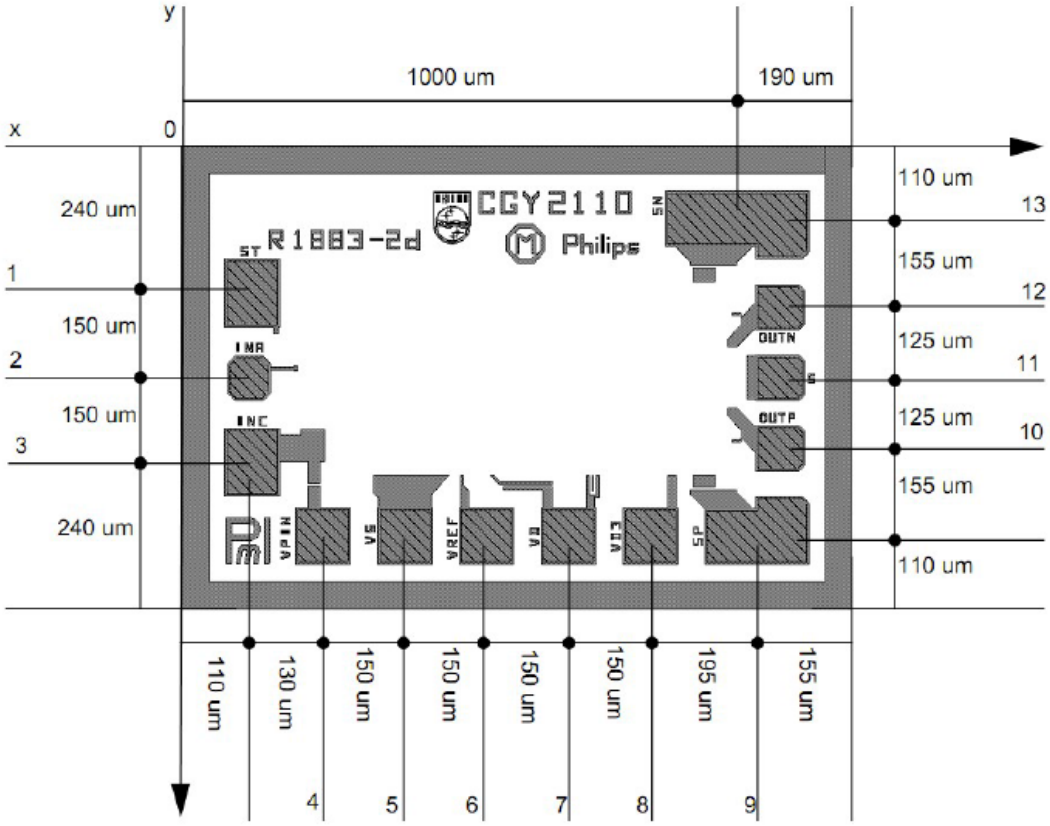
Handling Precautions :
- Use a conductive working desk connected to the ground (or, a conductive table top connected to the ground).
- Require all handling personal to wear a conductive bracelet or wrist-strap connected to the ground.
- Ground all test equipment and all soldering iron tops.
- Store IC's and other devices such as chip capacitors in their conductive carriers until they are soldered.

Pad Position

Pad #	Pad Name	Coordinate		Description
		X	Y	
1	ST	240	110	Do not bond
2	INA	390	110	RF Input, to be connected to photodiode anode
3	INC	540	110	photodiode biasing pad. To be connected to photodiode cathode (optional use)
4	VPIN	670	240	Photodiode DC biasing voltage (optional use)
5	VS	670	390	Bond to ground with lowest possible inductance
6	VREF	670	540	Reference input voltage, must be decoupled to ground using external capacitors
7	VD	670	690	First stage DC supply voltage
8	VD3	670	840	Second stage DC supply voltage
9	SP	670	1035	Bond to ground
10	OUTP	515	1080	RF non-inverted output
11	S	390	1080	Bond to ground
12	OUTN	265	1080	RF inverted output
13	SN	110	1000	Bond to ground

X=0, Y=0 at bottom left corner.
Co-ordinates correspond to the Centre of the Bonding Pad.
See Mechanical Information for more details.

Mechanical Information



Chip Size: 1190 x 780 µm (±15 µm)
VPIN, VS, VREF, VD, VD3: 100 x 100 µm
OUTP, OUTN, S: 90 x 80 µm
ST, INC: 120 x 100 µm
INA: 80 x 80 µm
SP: 190 x 100 µm
SN: 260 x 100 µm
Substrate Thickness: 200 µm