Transimpedance Amplifier, 2.5 Gb/s

CGY2102UH/C2
Rev. V1

Features

- Suitable for 2.5 Gb/s Optical Fiber Links
- Single Supply Voltage: +3.3 V to +5.0 V
- Differential Transimpedance Gain: 70 dBW
- Sensitivity: -27.5 dBm @ BER of 10-10
- Built in AGC Function
- Differential Output
- Peak-to-Peak Input Overload Current: 2.5 mA
- Consumption Current: 45 mA @ +3.3 V
- Tested, Inspected Known Good Die (KGD)
- Samples Available
- Demonstration Boards Available
- Space and MIL-STD also Available
- RoHS* Compliant

Applications

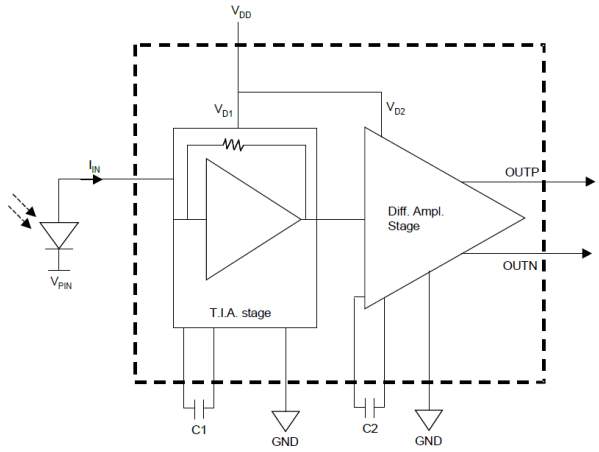
- Digital Optical STM-16 or OC-48 Transmission Systems
- PIN or APD Preamplifier Receivers
- GPON Optical Network Unit (ONU)

Description

The CGY2102UH/C2 is a high performance 2.5 Gb/s transimpedance amplifier (TIA). Typical use is as a low noise preamplifier for lightwave receiver modules in optical fiber networks. The TIA gives an exceptionally good sensitivity and high gain. The device is intended to be used with a PIN or APD photodetector. There is a built in AGC function which limits the peak-to-peak output voltage and protects the device from optical input overload. The CGY2102UH/C2 can be assembled in a small form factor packages, such as TO-46 headers.

The die is manufactured using the 0.18 µm gate length pHEMT technology. The MMIC uses gold bond pads and backside metallization and is fully protected with silicon nitride passivation to obtain the highest level of reliability. This technology has been evaluated for Space applications and is on the European Preferred Parts List of the European Space Agency.

Block Diagram



Ordering Information

Part Number	Package
CGY2102UH/C2	2.5 Gb/s transimpedance amplifier

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

DC Characteristics:

Minimum/Maximum values are defined at V_{DD} = 3.3 V ± 0.3 V, T_A = -40°C to +100°C; Typical data is defined at T_A = 25°C, V_{DD} = 3.3 V ; unless otherwise stated.

Parameter	Units	Min.	Typ.	Max.
Supply Current	mA	—	45	64
DC Input Voltage (IN Pad)	V	—	1.2	1.8
DC Output Voltage Level	V	—	2.5	—
Voltage Offset Between the 2 Outputs	V	-0.7	—	+0.7

Parameter	Units	Min.	Typ.	Max.
Supply Current	mA	—	60	88
DC Input Voltage (IN Pad)	V	—	1.3	1.8
DC Output Voltage Level	V	—	4	—
Voltage Offset Between the 2 Outputs	V	-0.7	—	+0.7

AC Characteristics:

All measured data is at V_{DD} = 3.3 V; T_A = 25°C; RL = 50 Ω. The TIA is measured on-wafer using RF probes. AC characteristics are guaranteed for both OUTP and OUTN ; Unless otherwise stated. C_{PH} = 0.3 pF, L_{PH} = 2.5 nH, R_{PH} = 8 Ω

Parameter	Conditions	Units	Min.	Typ.	Max.
Low Frequency Transimpedance Gain[1] @ 200 MHz, Single Ended	— V_{DD} = 3.3 V ±0.3 V, T_A = -40°C to +100°C V_{DD} = 5.0 V, T_A = +25°C	dBΩ	68.5 68.0 —	70.0 — 73.0	—
Transimpedance Gain Cut-Off Frequency	— V_{DD} = 3.3 V ±0.3 V, T_A = -40°C to +100°C V_{DD} = 5.0 V, T_A = +25°C	GHz	2.5 2.2 —	2.8 — 3.5	—
Low Frequency Cut-Off	AC Coupled at All Outputs (via 100 nF Capacitor)	KHz	—	—	25
Transimpedance Ripple	0.1 MHz - 1.0 GHz 1.0 GHz - 1.8 GHz 1.8 GHz - F_C	dBΩ	-1.0 -1.5 —	—	+1.2 +1.5 +2.0
Output Swing	Single Ended	mVpp	—	325	—
Maximum Peak Input Current	Before Input Overload	mApp	2.5	—	—
Output Reflection Coefficient	0.1 MHz - 2.2 GHz 2.2 GHz - 3.0 GHz	dB	—	—	-12 -8
Total integrated input RMS noise	0.1 GHz - 2.8 GHz	nA	—	207	—
Optical Input Sensitivity	ρ = 0.9 A/W, re = 10 dB, BER = 10^{-10}	dBm	—	-27.5	—
Output Load Termination	OUTN, OUTP	Ω	—	50	—

1. The gain specification is guaranteed down to the lower cut-off frequency. 0.2 GHz is specified as a reference for convenience of measurement.
2. The CGY2102UH is AC coupled at its outputs via an external capacitors, C3 and C4. Hence the low frequency cut-off is determined by the time constant RC, where R is the total output resistance (on-chip output series 50 Ω impedance of the TIA circuit plus the external 50 Ω load) equivalent to 100 Ω.
   Assuming that C3 = C4 = 100 nF, the low frequency cut-off is given by: Fc_low = 1/(2 x pi x R x C3) = 16 KHz.
3. The sensitivity is computed from the total integrated input RMS noise. To obtain a system bit-error rate of 10- 10, the signal-to-noise ratio must be 12.7 or better. The input sensitivity, expressed in average power, is calculated as:

$$\text{Sensitivity} = 10 \times \log\left(\frac{12.7 \times I_{NOISE} \times (r_e + 1)}{2 \times \rho \times (r_e - 1)} \times 1000\right) \text{(dBm)}$$

where ρ and r_e are respectively, the photodiode responsivity in A/W and the extinction ratio. I_{NOISE} is measured in amperes.

Absolute Maximum Ratings[1,2]

Parameter	Absolute Maximum
Supply Voltage	-0.5 V to +8.0 V
Input Average Photo Current @ 3.3 V	4 mA
Junction Temperature	+150°C
Storage Temperature	-55°C to +150°C

1. Exceeding any one or combination of these limits may cause permanent damage to this device.
2. MACOM does not recommend sustained operation near these survivability limits.

Operating Conditions

Parameter	Absolute Maximum
Supply Voltage[3]	+3.0 V to +3.6 V +4.75 V to +5.25 V
Junction Temperature	+150°C
Operating Temperature	-40°C to +100°C
Input Interface	DC Coupled
Output Interface	AC Coupled

3. The TIA IC operates properly in the entire range between 3.0 V and 5.25 V. Nevertheless, the circuit is specified at VDD = 3.3 V ± 0.3 V and VDD = 5.0 V ± 0.25 V.

Handling Procedures

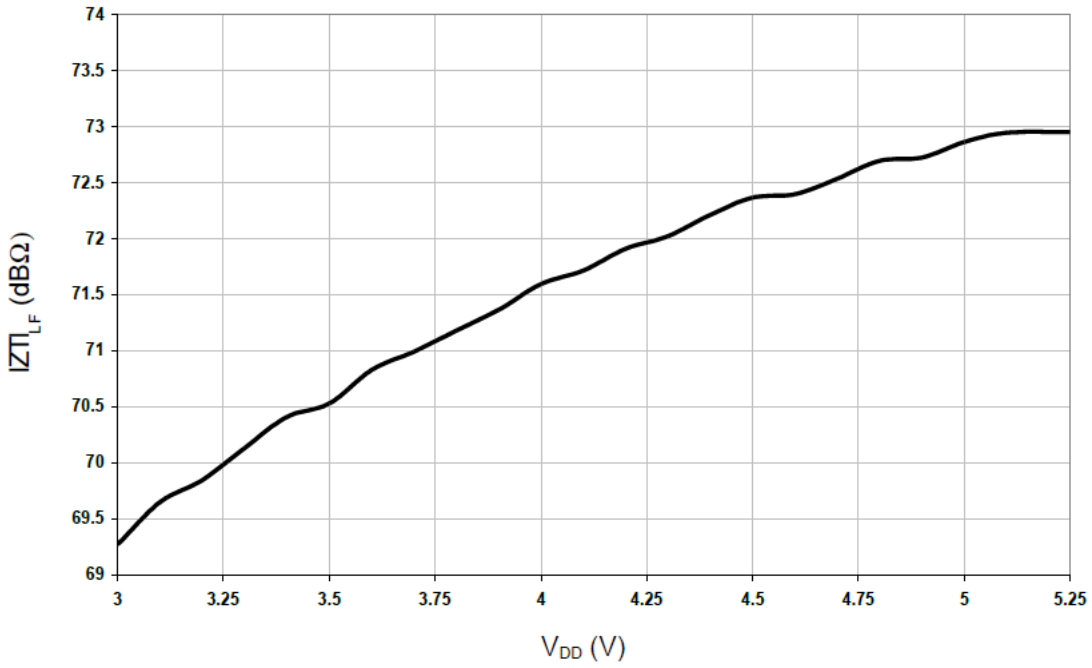
Please observe the following precautions to avoid damage:

Static Sensitivity

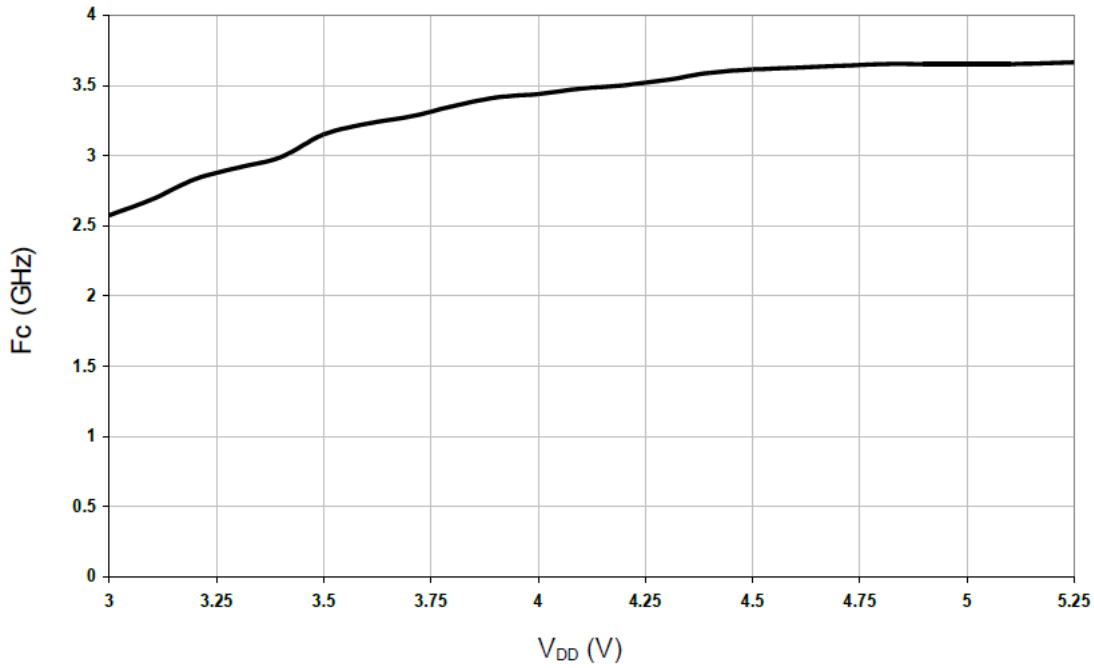
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Typical Performance Curves:

Transimpedance gain vs. V_{DD}

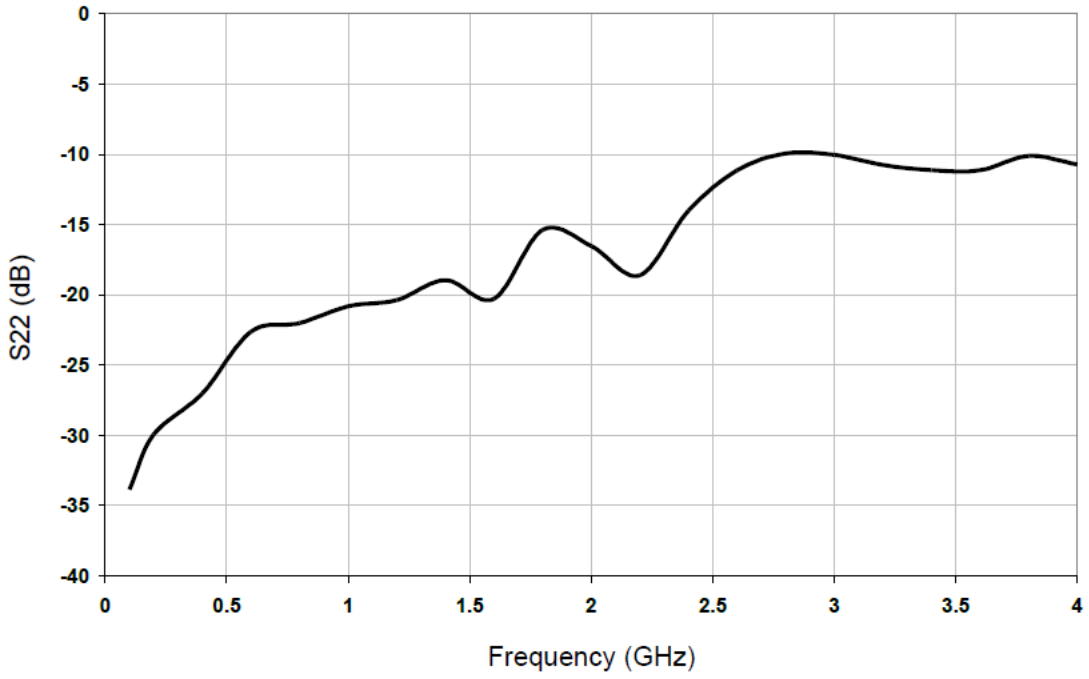


High frequency cut-off vs. V_{DD}

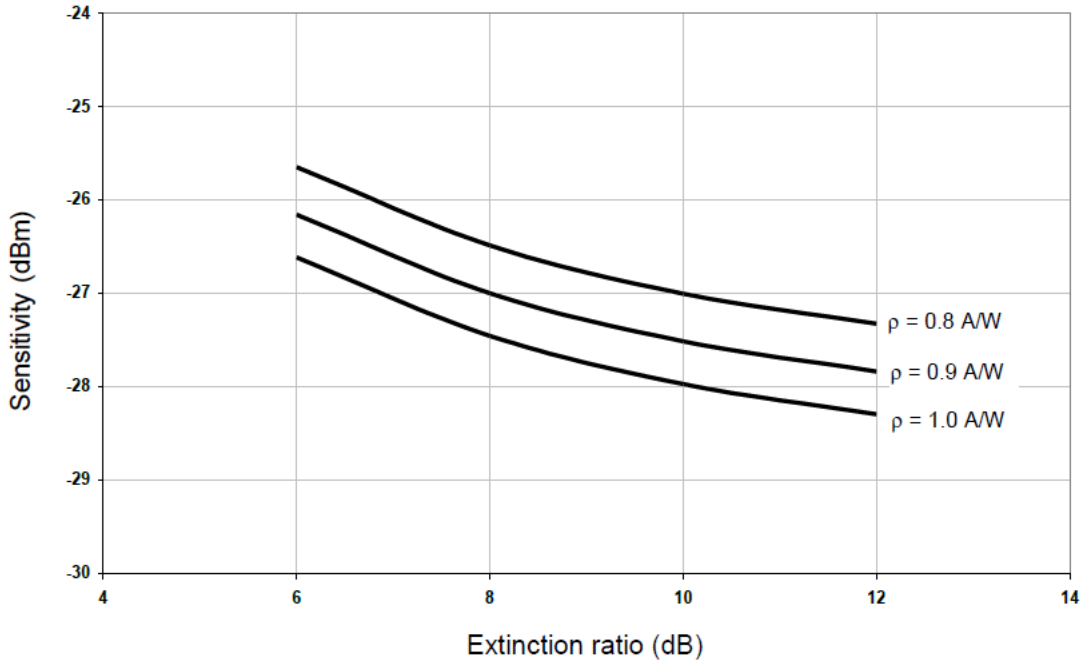


Typical Performance Curves:

Output Reflection Coefficient vs. Frequency

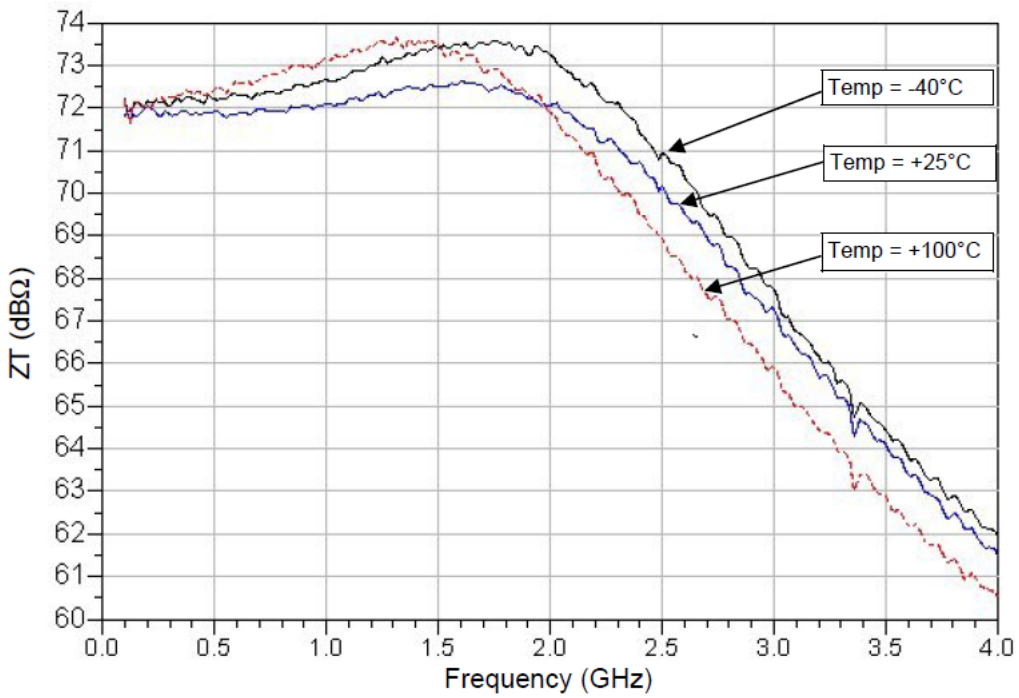


Sensitivity vs. Extinction ratio at various photodiode sensitivity, ρ.



Typical Performance Curves:

Transimpedance gain at various operating temperature (V_{DD} = 3.3 V)



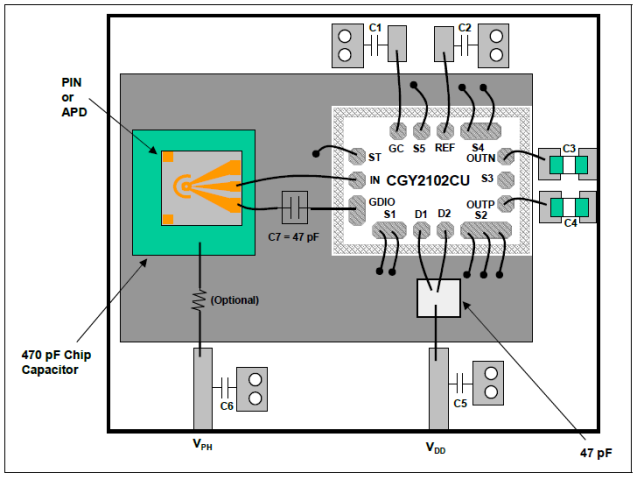
Bonding Diagram & Assembly Information

The performance of the photo-receiver module is very dependent on the photodiode capacitance of the photodiode. The circuit was optimized for a photodiode capacitance CPH lower than 0.3 pF with a low photodiode series resistance (RPH) to give the best noise performance from the receiver module. The CGY2102UH can be used in differential or single ended topology. In the case of single ended configuration, the unused output pad is connected to a 50 Ω load via a DC blocking capacitor (C3, C4).

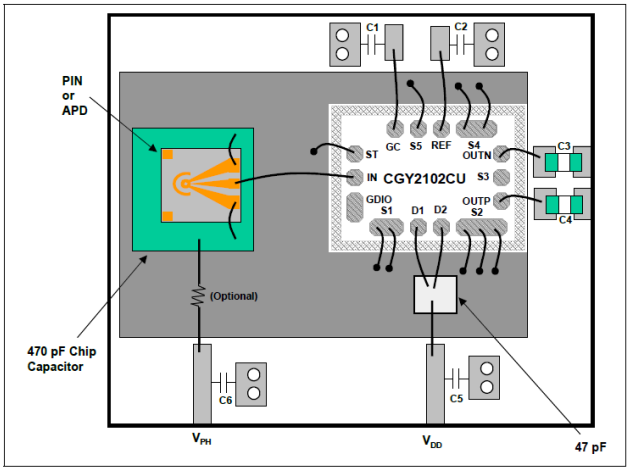
1) Recommended Assembly for RF Performances Guarantee

Two module layout are proposed. The difference occurs only at the input of the receiver:

- In configuration 1, the photodiode cathode is connected to GDIO pad chip via C7 = 47 pF capacitor. This configuration offers slightly more bandwidth.
- The second configuration is more compact at the input.



Configuration 1 : Chip assembly and bonding diagram

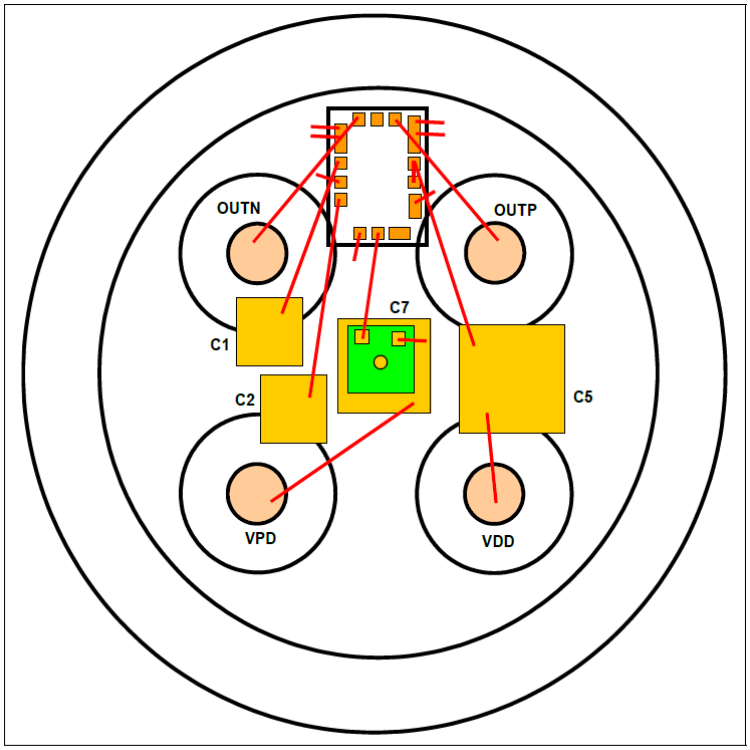


Configuration 2 : Chip assembly and bonding diagram

Recommended Parts List

Pad Name	Description
C1, C2, C5, C6	10 nF
C3, C4	100 nF

2) Suggested Assembly in a 5-pin TO-46
Typical application inside a 5-pin TO-46 is in the figure below. Output RF coupling capacitors, at ports OUTP and OUTN, are implemented outside the TO-46. Therefore, they do not appear in this figure.



Chip assembly and bonding diagram for a 5-Pin TO-46

Recommended Parts List

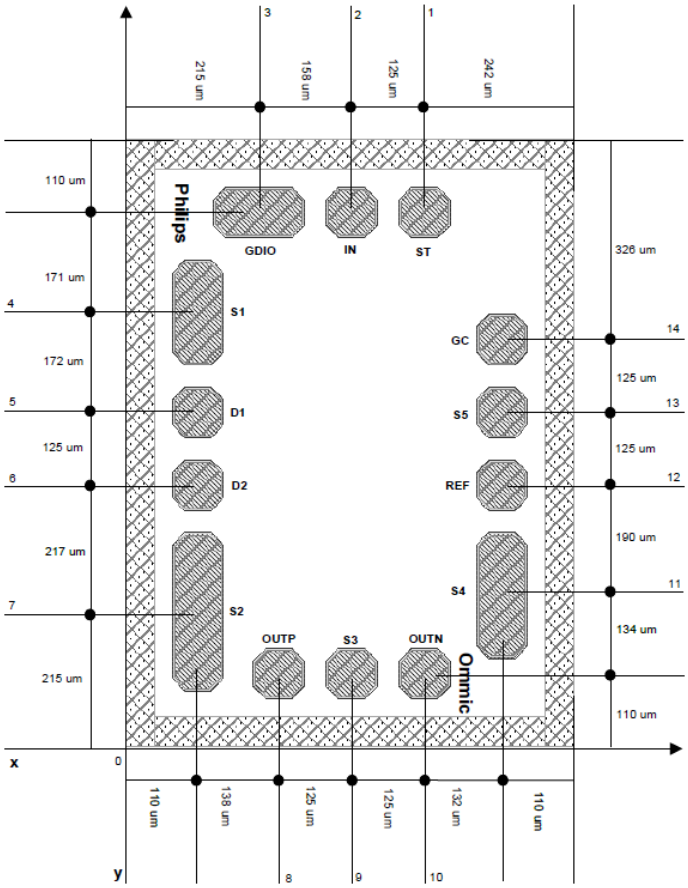
Pad Name	Description
C1, C2,	1.5 nF
C5	10 nF
C7	0.5 nF

Pad Position

Pad #	Pad Name	Coordinate		Description
		X	Y	
1	ST	900	498	bond to ground
2	IN	900	373	RF Input, to be connected to photodiode anode
3	GDIO	900	215	Config 1: connect to photodiode cathode via external capacitor. Config 2: do not bond
4	S1	729	110	bond to ground
5	D1	557	110	First stage DC supply voltage, must be decoupled to ground using an external capacitor
6	D2	432	110	Second stage DC supply voltage, must be decoupled to ground using an external capacitor
7	S2	215	110	bond to ground
8	OUTP	110	248	RF positive non inverting data output
9	S3	110	373	bond to ground
10	OUTN	110	498	RF negative inverting data output
11	S4	244	630	bond to ground
12	REF	434	630	Reference input voltage, must be decoupled to ground using an external capacitor
13	S5	559	630	bond to ground
14	GC	684	630	Gain control pad, must be decoupled to ground using an external capacitor

X=0, Y=0 at bottom left corner.
Co-ordinates correspond to the Centre of the Bonding Pad.
See Mechanical Information for more details.

Mechanical Information



Chip Size: 1010 x 740 µm (±15 µm)
ST, IN, D1, D2, OUTP, S3, OUTN, REF, S5, GC: 90 x 90 µm
GDIO: 157 x 90 µm
S1: 180 x 90 µm
S2: 272 x 90 µm
S4: 216 x 90 µm
Substrate Thickness: 200 µm