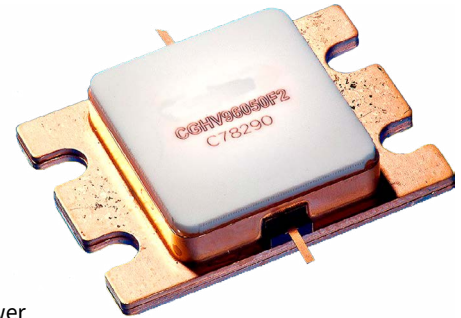


CGHV96050F2

50 W, 7.9 - 9.6 GHz, 50-ohm, Input/Output Matched GaN HEMT



PN: CGHV96050F2
Package Type: 440217

Description

The CGHV96050F2 is a gallium nitride (GaN) High Electron Mobility Transistor (HEMT) on Silicon Carbide (SiC) substrates. This GaN Internally Matched (IM) FET offers excellent power added efficiency in comparison to other technologies. GaN has superior properties compared to silicon or gallium arsenide, including higher breakdown voltage, higher saturated electron drift velocity and higher thermal conductivity. GaN HEMTs also offer greater power density and wider bandwidths compared to GaAs transistors. This IM FET is available in a metal/ceramic flanged package for optimal electrical and thermal performance.

Typical Performance Over 8.4 - 9.6 GHz ($T_c = 25^\circ\text{C}$)

Parameter	8.4 GHz	8.8 GHz	9.0 GHz	9.2 GHz	9.4 GHz	9.6 GHz	Units
Linear Gain	13.8	12.8	12.3	12.3	12.2	11.8	dB
Output Power	85	77	81	82	75	75	W
Power Gain	10.4	9.9	10.1	10.1	8.8	9.8	dB
Power Added Efficiency	57	54	52	54	48	45	%

Note: Measured in CGHV96050F2-AMP (838179) under 100 μs pulse width, 10% duty, P_{IN} 39.0 dBm (7.9 W)

Features

- 8.4 - 9.6 GHz Operation
- 80 W P_{OUT} typical
- 10 dB Power Gain
- 55% Typical PAE
- 50 Ohm Internally Matched
- <0.1 dB Power Droop

Applications

- Marine Radar
- Weather Monitoring
- Air Traffic Control
- Maritime Vessel Traffic Control
- Port Security

Large Signal Models Available for ADS and MWO



Absolute Maximum Ratings (not simultaneous)

Parameter	Symbol	Rating	Units	Conditions
Drain-source Voltage	V_{DSS}	120	V	25°C
Gate-source Voltage	V_{GS}	-10, +2		
Power Dissipation	P_{DISS}	57.6 / 86.4	W	(CW / Pulse)
Storage Temperature	T_{STG}	-65, +150	°C	
Operating Junction Temperature	T_J	225		
Maximum Drain Current	I_{DMAX}	6	A	
Maximum Forward Gate Current	I_{GMAX}	14.4	mA	25°C
Soldering Temperature ¹	T_S	245	°C	
Screw Torque	τ	40	in-oz	
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.40	°C/W	Pulse Width = 100µs, Duty Cycle = 10%, $P_{DISS} = 86.4$ W
Thermal Resistance, Junction to Case		2.12		CW, 85°C, $P_{DISS} = 57.6$ W
Case Operating Temperature ³	T_C	-40, +125	°C	

Notes:

¹ Current limit for long term, reliable operation

² Refer to the Application Note on soldering

³ See also, the Power Dissipation De-rating Curve on Page 9

Electrical Characteristics (Frequency = 9.6 GHz unless otherwise stated; $T_C = 25^\circ\text{C}$)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Conditions
DC Characteristics¹						
Gate Threshold Voltage	$V_{GS(th)}$	-3.8	-3.0	-2.3	V	$V_{DS} = 10$ V, $I_D = 14.4$ mA
Gate Quiescent Voltage	$V_{GS(Q)}$	—		—		$V_{DS} = 40$ V, $I_D = 500$ mA
Saturated Drain Current ²	I_{DS}	11.5	13.0	—	A	$V_{DS} = 6.0$ V, $V_{GS} = 2.0$ V
Drain-Source Breakdown Voltage	V_{BR}	100	—	—	V	$V_{GS} = -8$ V, $I_D = 14.4$ mA
RF Characteristics³						
Small Signal Gain	S21	10.0	11.8	—	dB	$V_{DD} = 40$ V, $I_{DQ} = 500$ mA, $P_{IN} = -20$ dBm
Input Return Loss	S11	—	-5.2	-2.1		$V_{DD} = 40$ V, $I_{DQ} = 500$ mA, $P_{IN} = -20$ dBm, $f = 8.4 - 9.6$ GHz
Output Return Loss	S22	—	-12.3	-9.0		$V_{DD} = 40$ V, $I_{DQ} = 500$ mA, $P_{IN} = -20$ dBm
Power Output ^{3,4}	P_{OUT}	47	70	—	W	$V_{DD} = 40$ V, $I_{DQ} = 500$ mA, $P_{IN} = 39$ dBm
Power Added Efficiency ^{3,4}	PAE	32	45	—	%	
Output Mismatch Stress	VSWR	—	—	5:1	Ψ	No damage at all phase angles, $V_{DD} = 40$ V, $I_{DQ} = 500$ mA

Notes:

¹ Measured on wafer prior to packaging.

² Scaled from PCM data

³ Measured in CGHV96050F2-AMP (AD-09115) under 100µs pulse width, 10% duty

⁴ Fixture loss de-embedded using the following offsets. At 9.6 GHz, input and output = 0.50 dB

CGHV96050F2 Typical Performance

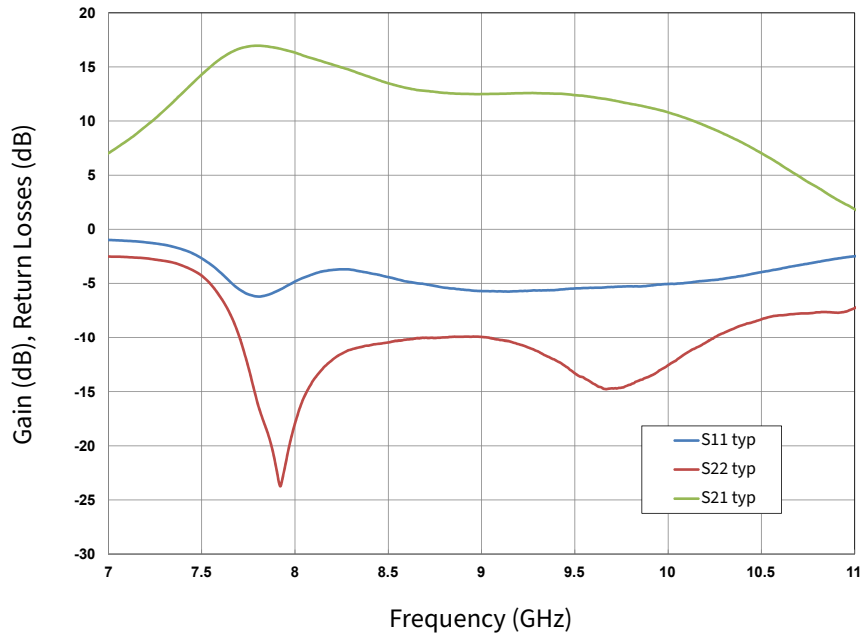


Figure 1. Small Signal Gain and Return Loss vs Frequency of CGHV96050F2 measured in CGHV96050F2-AMP
 $V_{DS} = 40\text{ V}$, $I_{DQ} = 500\text{ mA}$

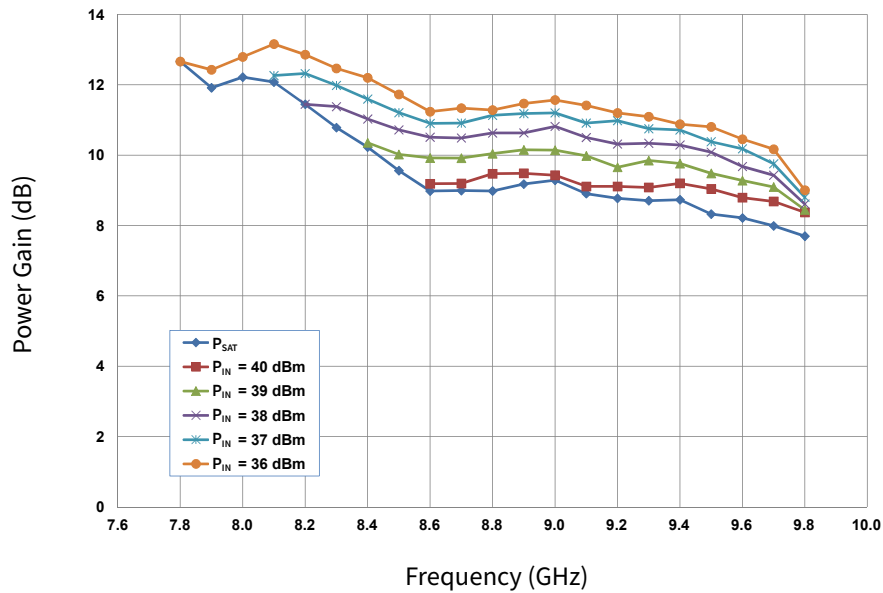


Figure 2. Power Gain vs Frequency and Input Power
 $V_{DD} = 40\text{ V}$, Pulse Width = 100 μ sec, Duty Cycle = 10%

CGHV96050F2 Typical Performance

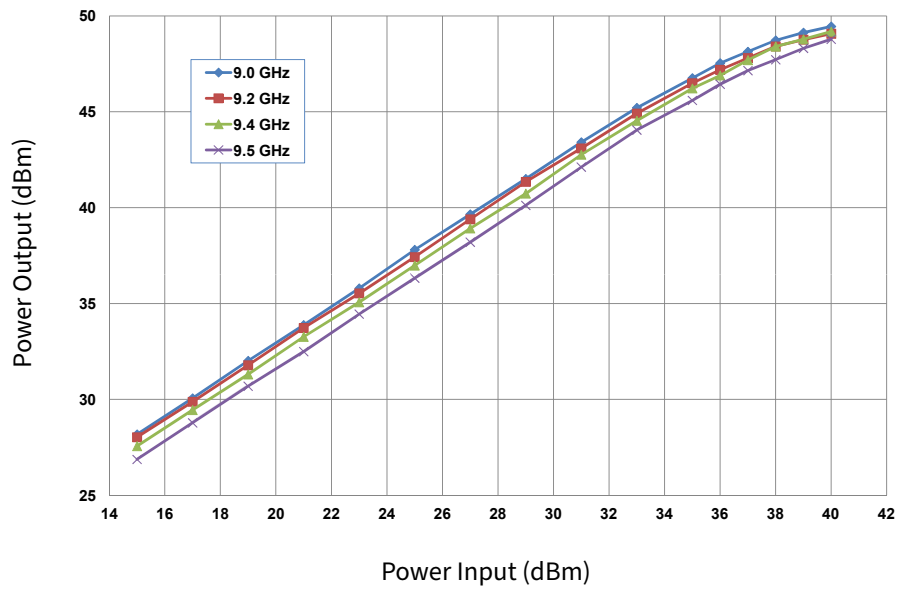


Figure 3. Output Power vs Input Power
 $V_{DD} = 40\text{ V}$, Pulse Width = 100 μsec , Duty Cycle = 10%

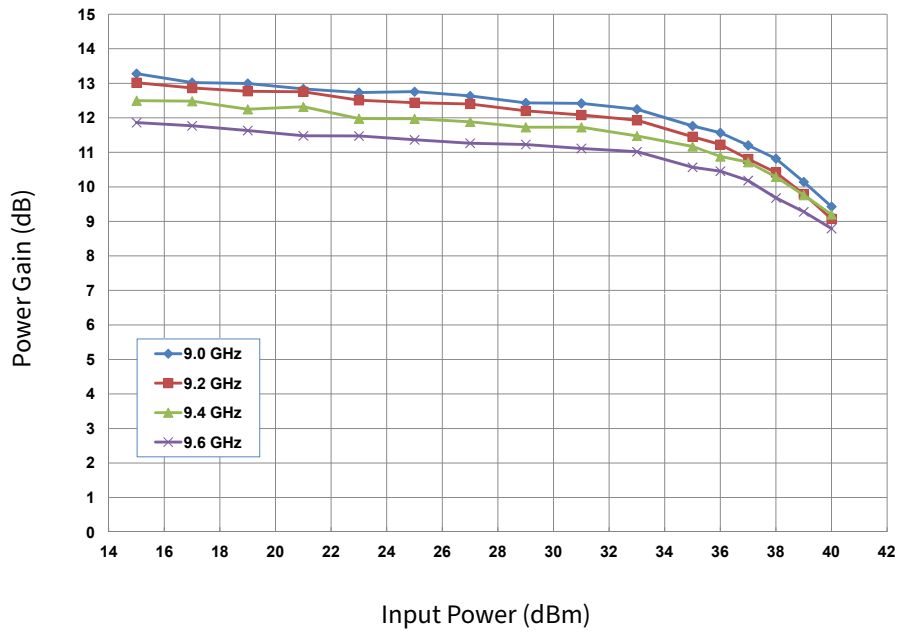


Figure 4. Power Gain vs Frequency and Input Power
 $V_{DD} = 40\text{ V}$, Pulse Width = 100 μsec , Duty Cycle = 10%

CGHV96050F2 Typical Performance

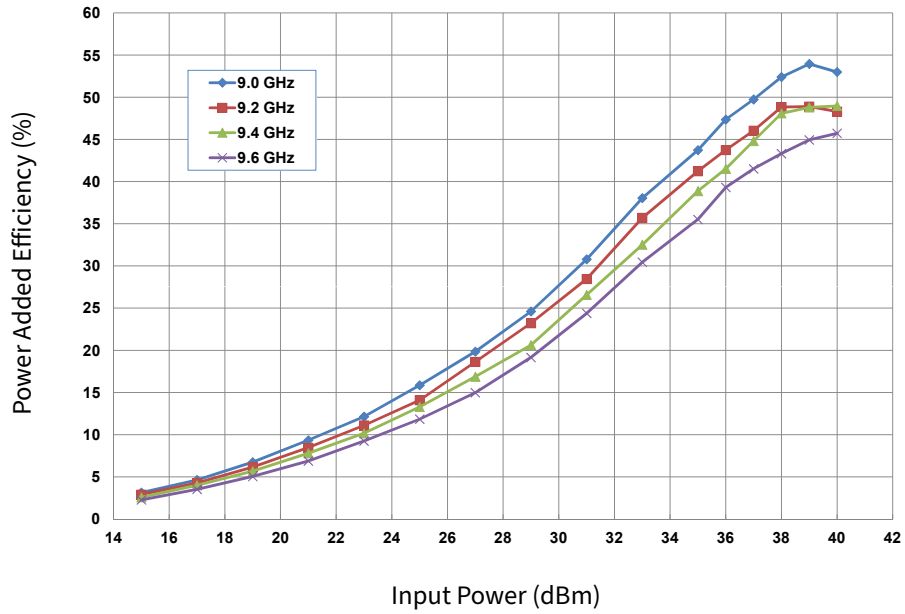


Figure 5. Output Power vs Input Power
 $V_{DD} = 40\text{ V}$, Pulse Width = $100\mu\text{sec}$, Duty Cycle = 10%

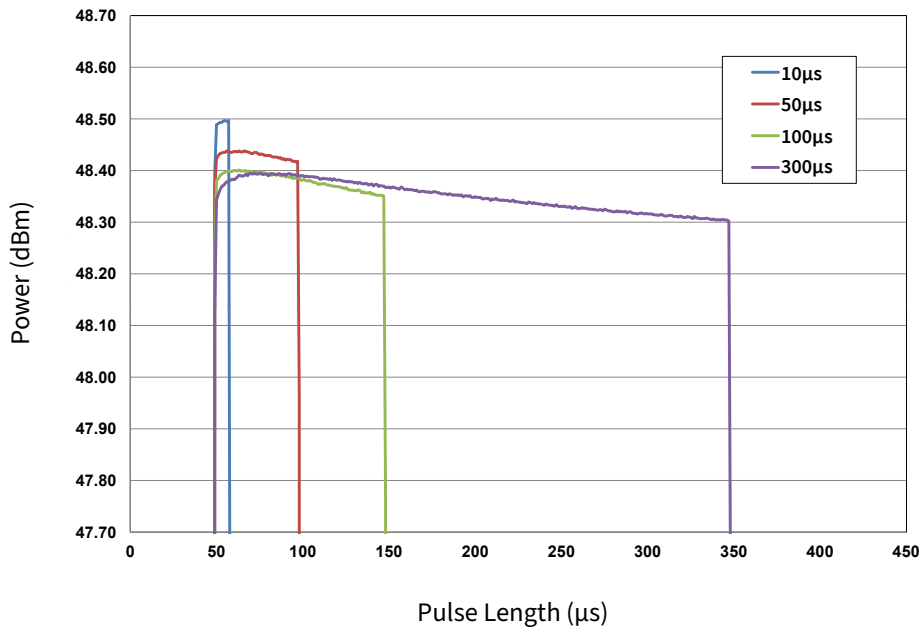


Figure 6. Power Gain vs Frequency and Input Power
 $V_{DD} = 40\text{ V}$, $P_{IN} = 39\text{ dBm}$, Duty Cycle = 10%

CGHV96050F2 Typical Performance

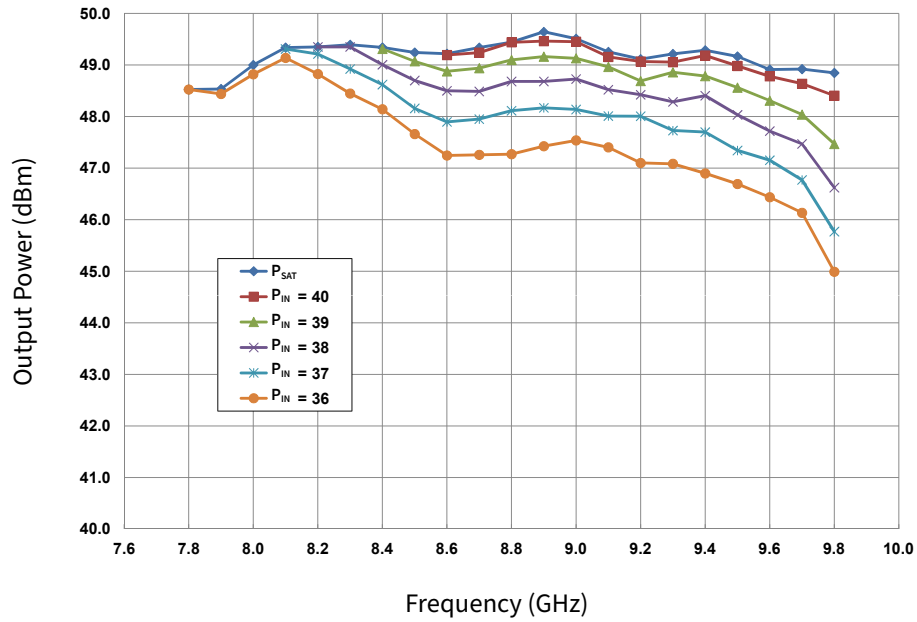


Figure 7. Output Power vs Input Power & Frequency
 $V_{DD} = 40\text{ V}$, Pulse Width = 100 μsec , Duty Cycle = 10%

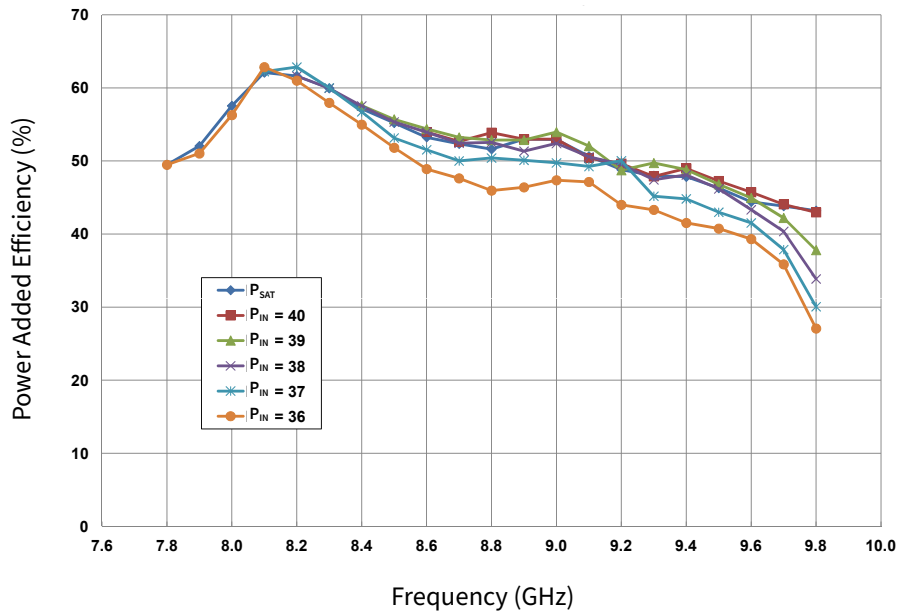
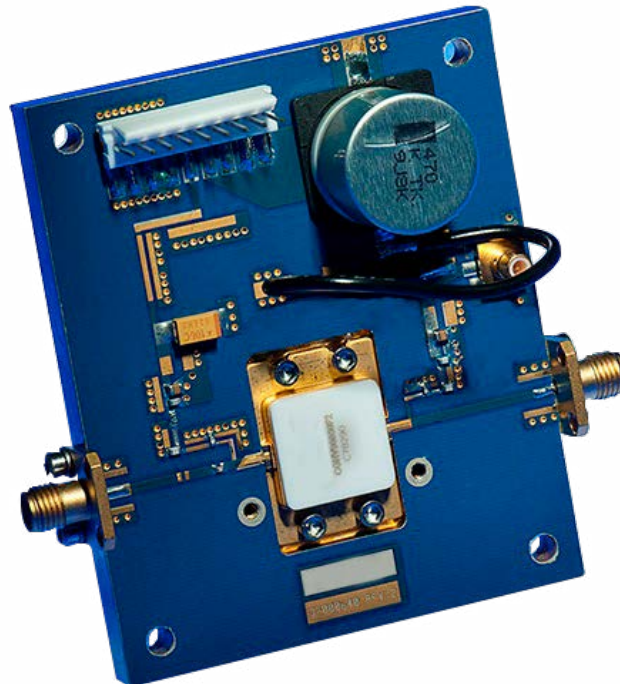


Figure 8. Power Added Efficiency vs Input Power & Frequency
 $V_{DD} = 40\text{ V}$, $P_{IN} = 39\text{ dBm}$, Duty Cycle = 10%

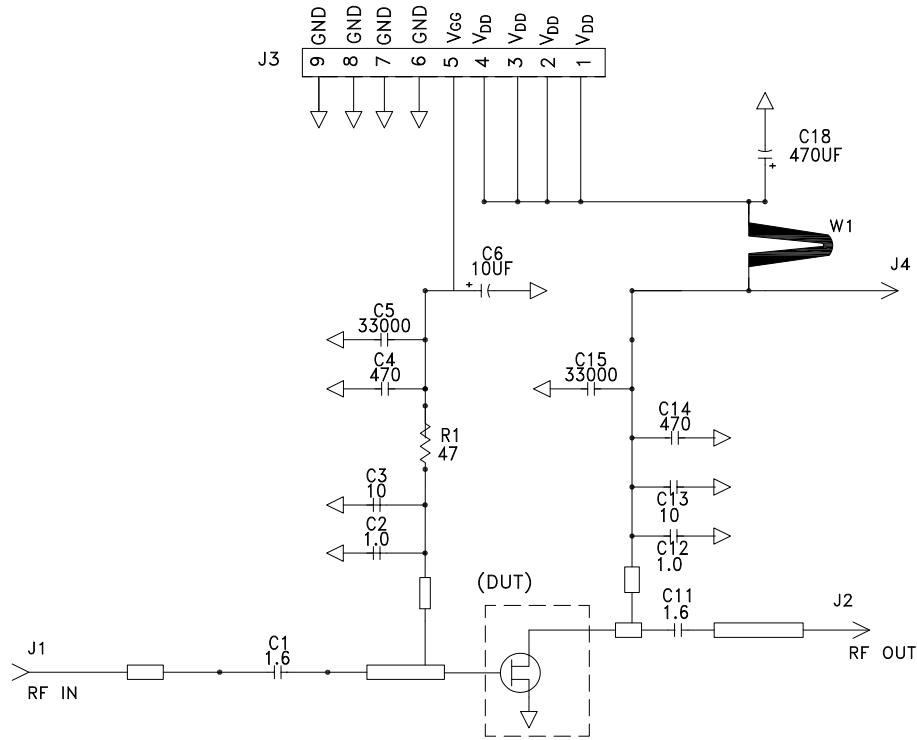
CGHV96050F2-AMP Demonstration Amplifier Circuit Bill of Materials

Designator	Description	Qty
R1	RES, 47 OHM, +/- 1%, 1/16W, 0603	1
C1	CAP, 0.9pF, +/- 0.05pF, 200V, 0402	1
C11	CAP, 1.6pF, +/- 0.1pF, 200V, 0402	1
C2, C12	CAP, 1.0pF, +/- 0.1pF, 200V, 0402	2
C3, C13	CAP, 10.0pF, +/-5%, 250V, 0603,	2
C4, C14	CAP, 470pF, 5%, 100V, 0603, X	2
C5, C15	CAP, 33000pF, 0805, 100V, X7R	2
C6	CAP 10μF 16V TANTALUM	1
C18	CAP, 470μF, 20%, 80V, ELECT, SMD Size K	1
J1, J2	CONN, N, FEM, W/.500 SMA FLNG	2
J3	HEADER RT>PLZ .1CEN LK 9POS	1
J4	CONNECTOR; SMB, Straight, JACK, SMD	1
W1	CABLE, 18 AWG, 4.2"	1
	PCB, RF35, 2.5 X 3.0 X (0.020/0.250)	1
	TRANSISTOR, CGHV96050F2	1
	#2 SPLIT LOCKWASHER SS	4
	2-56 SOC HD SCREW 1/4 SS	4

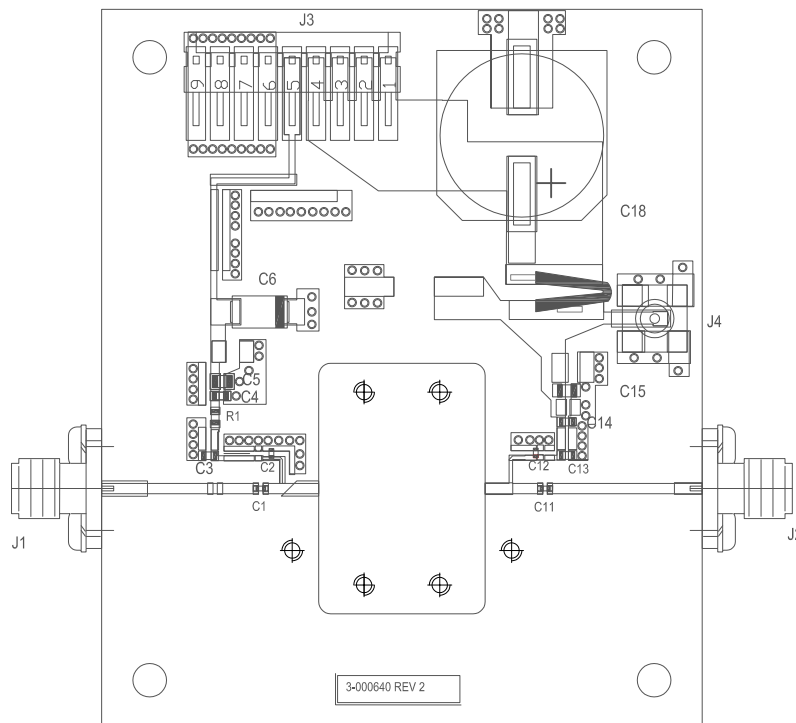
CGHV96050F2-AMP Demonstration Amplifier Circuit



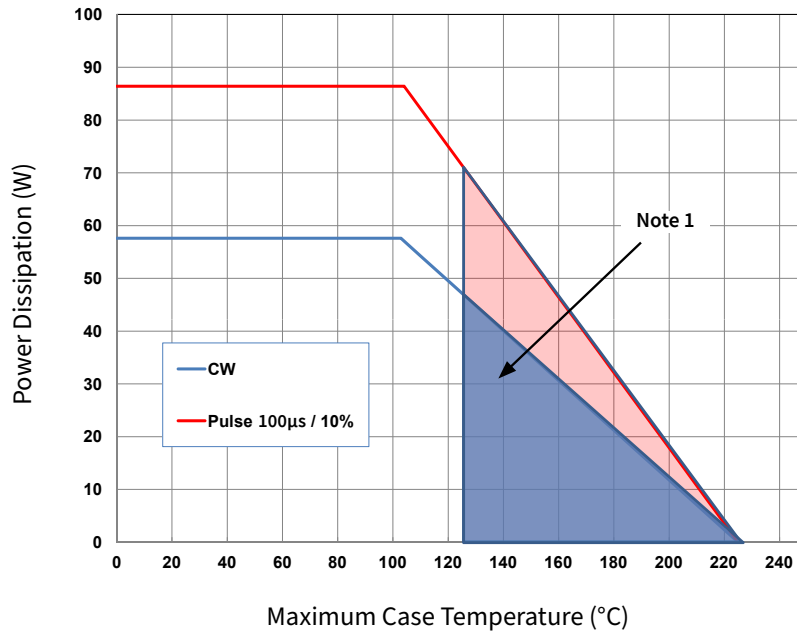
CGHV96050F2-AMP Demonstration Amplifier Circuit Schematic



CGHV96050F2-AMP Demonstration Amplifier Circuit Outline



CGHV96050F2 Power Dissipation De-rating Curve



Note:

¹Area exceeds Maximum Case Temperature (See Page 2)

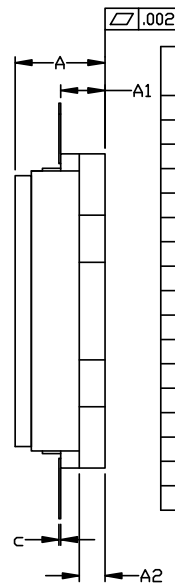
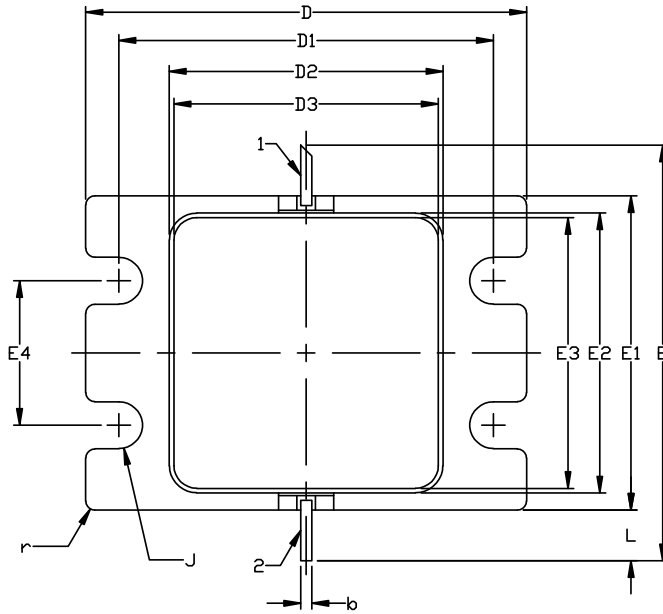
Electrostatic Discharge (ESD) Classifications

Parameter	Symbol	Class	Classification Level	Test Methodology
Human Body Model	HBM	TBD	ANSI/ESDA/JEDEC JS-001 Table 3	JEDEC JESD22 A114-D
Charge Device Model	CDM	TBD	ANSI/ESDA/JEDEC JS-002 Table 3	JEDEC JESD22 C101-C

Product Dimensions CGHV96050F2 (Package Type — 440217)

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. INTERPRET DRAWING IN ACCORDANCE WITH ANSI Y14.5M-2009
2. ADHESIVE FROM LID MAY EXTEND A MAXIMUM OF .020 BEYOND EDGE OF LID
3. LID MAY BE MISALIGNED TO THE BODY OF PACKAGE BY A MAXIMUM OF .008 IN ANY DIRECTION
4. ALL PLATED SURFACES ARE GOLD OVER NICKEL



DIM	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.188	0.198	4.78	5.03	
A1	0.088	0.100	2.24	2.54	2x
A2	0.049	0.061	1.24	1.55	
b	0.022	0.026	0.56	0.66	2x
c	0.002	0.006	0.05	0.15	
D	0.935	0.955	23.75	24.26	
D1	0.797	0.809	20.24	20.55	2x
D2	0.581	0.593	14.76	15.06	
D3	0.563	0.571	14.30	14.50	
E	0.906		23.01		REF
E1	0.679	0.691	17.25	17.55	
E2	0.604	0.616	15.34	15.65	
E3	0.586	0.594	14.88	15.09	
E4	0.309	0.321	7.85	8.15	2x
J	Ø0.097	Ø0.107	Ø2.46	Ø2.72	4x
L	0.090	0.130	2.29	3.30	2x
r	0.02	TYP	0.51	TYP	12x

1. GATE
2. DRAIN

Part Number System

CGHV96050F2

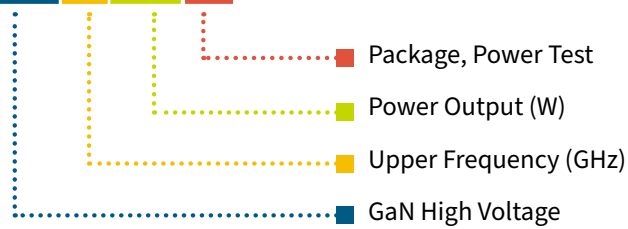


Table 1.

Parameter	Value	Units
Upper Frequency ¹	9.6	GHz
Power Output	50	W
Package	Flange	—

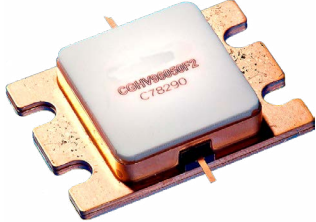
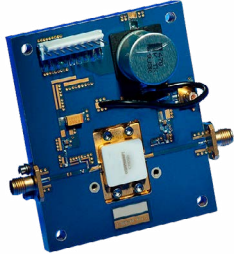
Note:

¹ Alpha characters used in frequency code indicate a value greater than 9.9 GHz. See Table 2 for value.

Table 2.

Character Code	Code Value
A	0
B	1
C	2
D	3
E	4
F	5
G	6
H	7
J	8
K	9
Examples	1A = 10.0 GHz 2H = 27.0 GHz

Product Ordering Information

Order Number	Description	Unit of Measure	Image
CGHV96050F2	GaN HEMT	Each	
CGHV96050F2-AMP	Test board with GaN HEMT Installed	Each	

Notes & Disclaimer

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