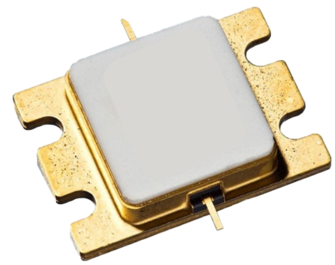
400 W, 50 Ω Input/Output Matched, GaN HEMT
2.9 - 3.5 GHz

CGHV35400F1
Rev. V2

Features

- Saturated Power: 500 W
- Large Signal Gain: 13 dB
- Drain Efficiency: 65%
- Internally Matched: 50 Ω
- High Temperature Operation
- RoHS* Compliant



Package Type: 440226

Applications

- Civil & Military Pulsed Radar Amplifiers

Description

The CGHV35400F1 is a gallium nitride (GaN) high electron mobility transistor (HEMT) designed specifically with high efficiency and high gain for the 2.9 - 3.5 GHz S-Band radar band. The device has been developed with long pulse capability to meet the developing trends in radar architectures. The transistor is matched to 50-ohms on the input and 50 -ohms on the output. The CGHV35400F1 is based on the high power density 50 V, 0.4 µm GaN on silicon carbide (SiC) manufacturing process. The transistor is supplied in a ceramic/ metal flange package of type 440226.

Ordering Information

Part Number	Package
CGHV35400F1	bulk
CGHV35400F1-AMP	test board

Typical Performance: Freq: 2.9 - 3.5 GHz, T_C = +25°C

Parameter	2.9 GHz	3.2 GHz	3.5 GHz	Units
Small Signal Gain[1,2]	15.0	13.6	12.5	dB
Power Gain[1,3]	11.1	10.9	10.4	dB
Output Power[1,3]	57.1	56.9	56.4	dBm
Drain Efficiency[1,3]	69	64	60	%

1. V_{DD} = 50 V, I_{DQ} = 500 mA.
2. Measured @ P_{IN} = -20 dBm.
3. Measured @ P_{IN} = +46 dBm and 2 ms; Duty Cycle = 20%.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

DC Electrical Characteristics @ T_C = +25°C

Characteristics	Symbol	Conditions	Units	Min.	Typ.	Max.
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = 10 V, I_D = 83.6 mA	V	-3.8	-3.0	-2.3
Gate Quiescent Voltage	$V_{GS(Q)}$	V_{DS} = 50 V, I_D = 500 mA	V	—	-2.7	—
Saturated Drain Current[4]	I_{DS}	V_{DS} = 6 V, V_{GS} = 2 V	A	62.7	75.5	—
Drain-Source Breakdown Voltage	V_{BR}	V_{GS} = -8 V, I_D = 83.6 mA	V	125	—	—

4. Scaled from PCM data.

RF Electrical Characteristics[5] @ T_C = +25°C, Freq. = 2.9 - 3.5 GHz, V_{DD} = 50 V, I_{DQ} = 500 mA

Characteristics	Symbol	Conditions	Units	Min.	Typ.	Max.
Small Signal Gain	S21	P_{IN} = -20 dBm	dB	—	13.7	—
Input Return Loss	S11	P_{IN} = -20 dBm	dB	—	7.1	—
Output Return Loss	S22	P_{IN} = -20 dBm	dB	—	5.8	—
Power Gain	G_P	P_{IN} = 46 dBm 2.9 GHz 3.2 GHz 3.5 GHz	dB	10.0	11.2 11.0 10.7	—
Output Power	P_{OUT}	P_{IN} = 46 dBm 2.9 GHz 3.2 GHz 3.5 GHz	dBm	56.0	57.2 57.1 56.7	—
Drain Efficiency	D_E	P_{IN} = 46 dBm 2.9 GHz 3.2 GHz 3.5 GHz	%	54	68 63 62	—
Output Mismatch Stress	VSWR	No damage at all phase angles	Ψ	—	—	3:1

5. Pulse Width = 500 μs, Duty Cycle = 10%.

Thermal Characteristics

Parameter	Symbol	Test Conditions	Units	Rating
Operating Junction Temperature	T_J	Pulse Width = 2 ms, Duty Cycle = 20%, P_{DISS} = 418 W, T_C = 57.2°C	°C	224
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W	0.4

Absolute Maximum Ratings (Not Simultaneous)

Parameter	Symbol	Conditions	Units	Rating
Drain-Source Voltage	V_{DSS}	25°C	V	150
Gate-Source Voltage	V_{GS}	25°C	V	-10 to +2
Maximum Forward Gate Current	I_{GMAX}	25°C	mA	80
Maximum Drain Current	I_{DMAX}	25°C	A	24
Soldering Temperature	T_S	—	°C	245
Operating Junction Temperature	T_J	MTTF > 1e6 Hours	°C	225
Storage Temperature	T_{STG}	—	°C	-65 to +150

Handling Procedures

Please observe the following precautions to avoid damage:

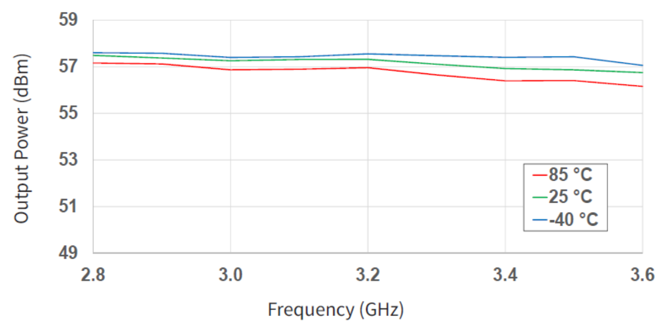
Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 3A and CDM C3 Class devices.

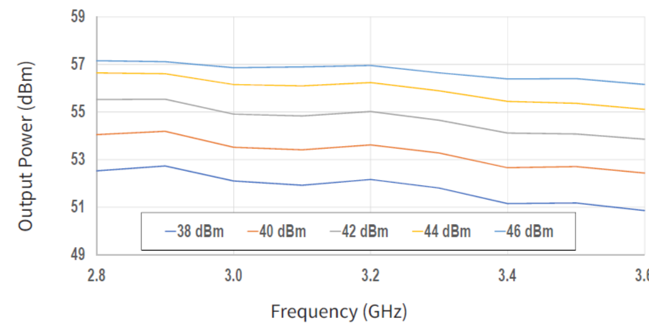
Typical Performance Curves:

V_D = 50 V, I_{DQ} = 500 mA, Pulse Width = 500 µs, Duty Cycle = 10%, P_{IN} = 46 dBm, T_B = +25°C

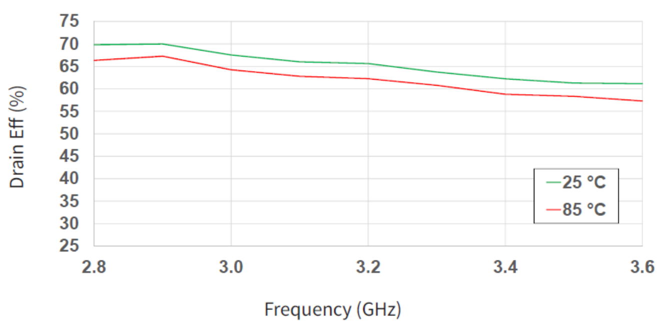
Output Power vs. Frequency over Temperature



Output Power vs. Frequency over Input Power



Drain Efficiency vs. Frequency over Temperature



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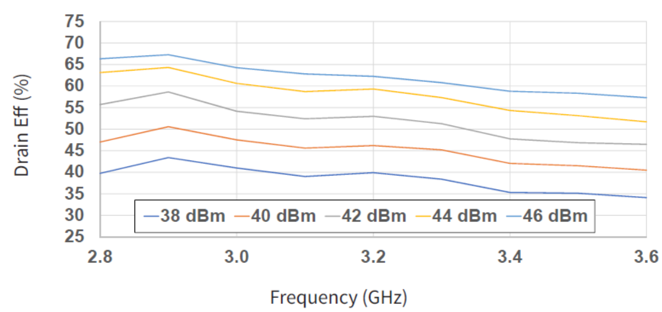
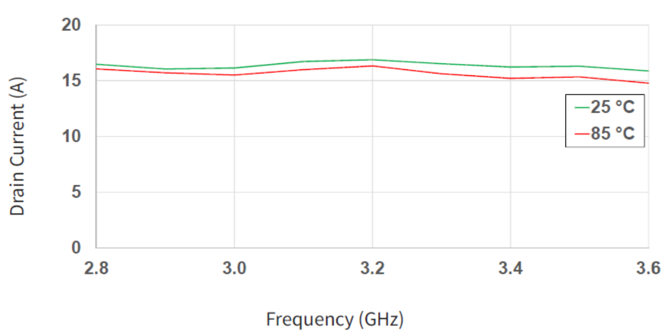


Drain Current vs. Frequency over Temperature



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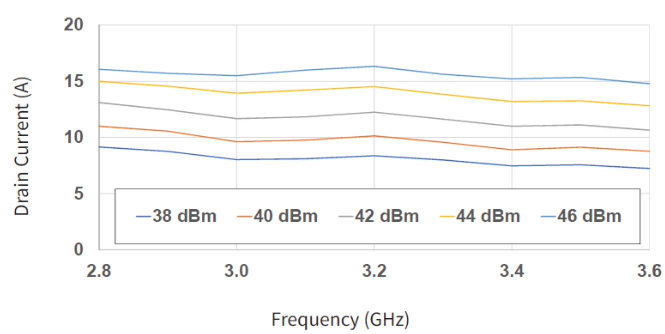

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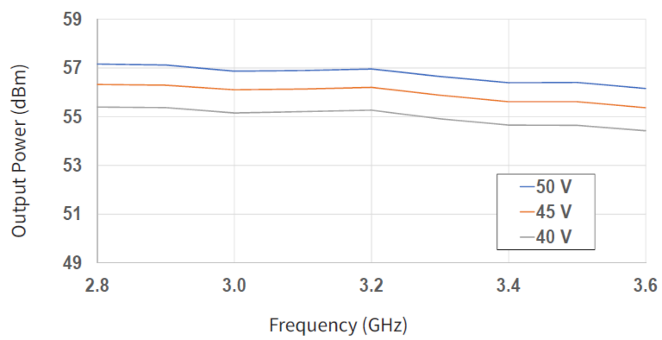
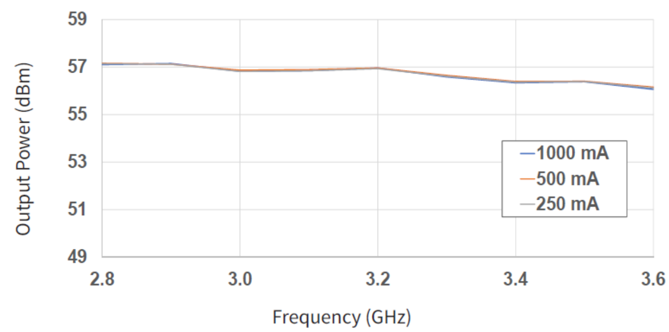
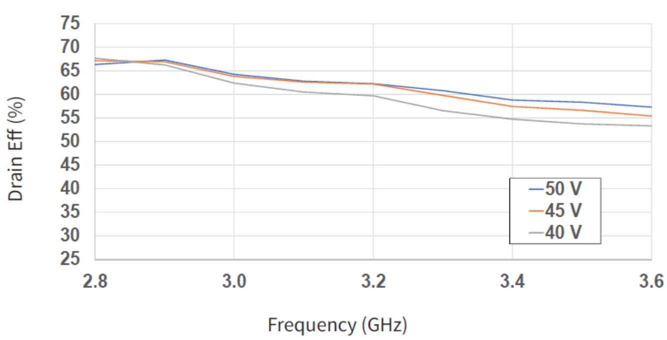
Output Power vs. Frequency over Voltage



Output Power vs. Frequency over I_{DQ}



Drain Efficiency vs. Frequency over Voltage



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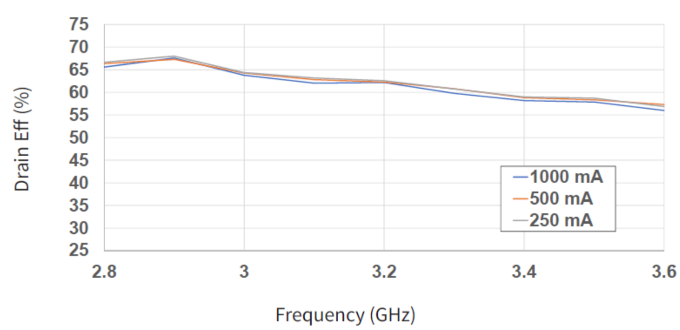
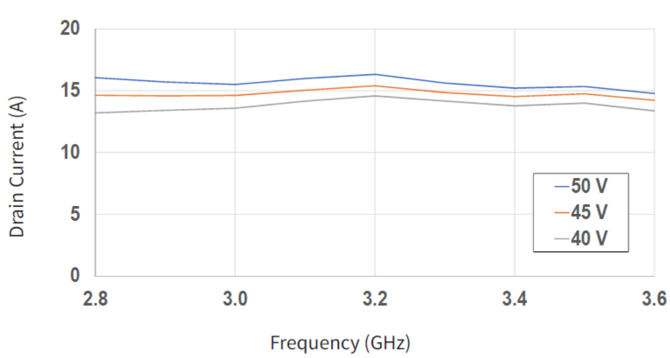


Drain Current vs. Frequency over Voltage



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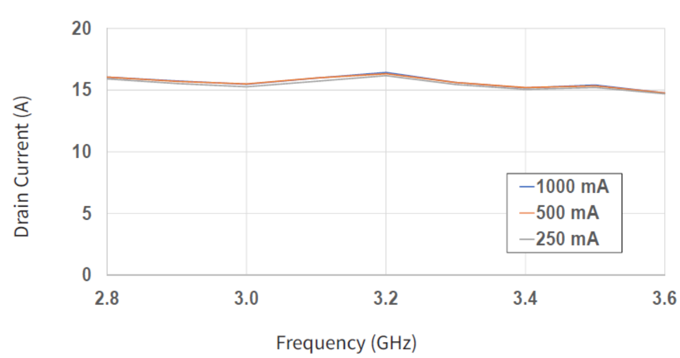

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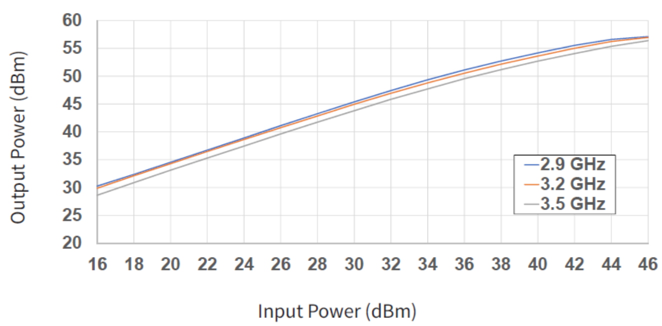
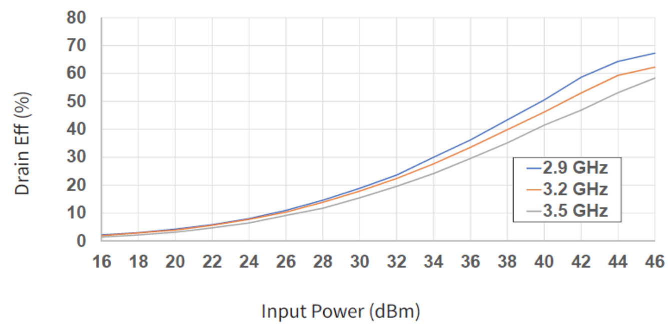
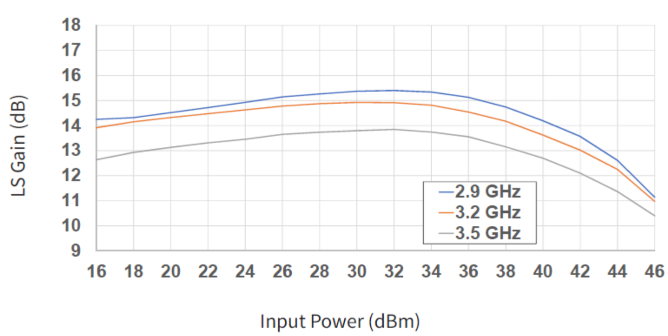


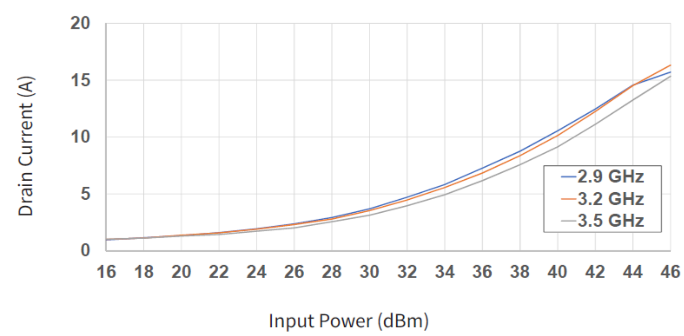
Drain Efficiency vs. Input Power Over Frequency



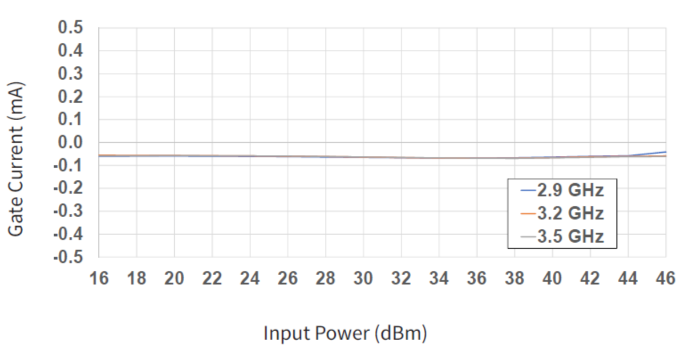
LS Gain vs. Input Power Over Frequency



Drain Current vs. Input Power Over Frequency



Gate Current vs. Input Power Over Frequency



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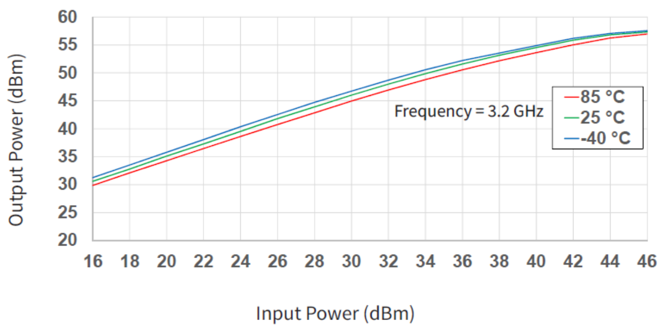
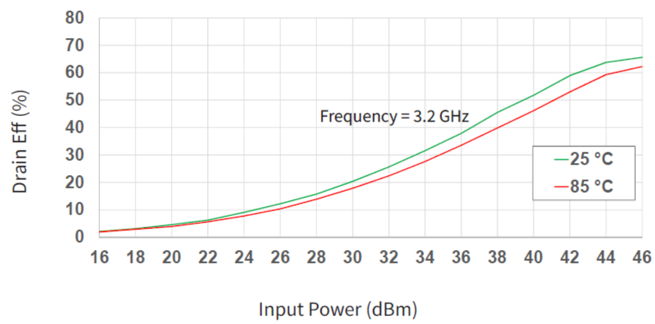
Output Power vs. Input Power Over Temperature



Drain Efficiency vs. Input Power Over Temperature



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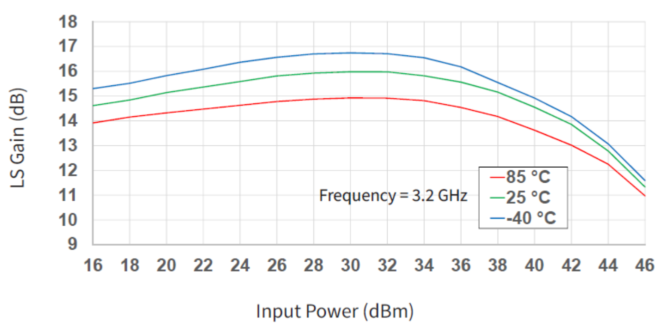

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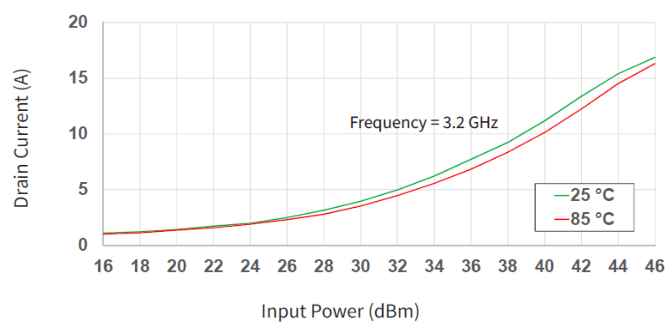

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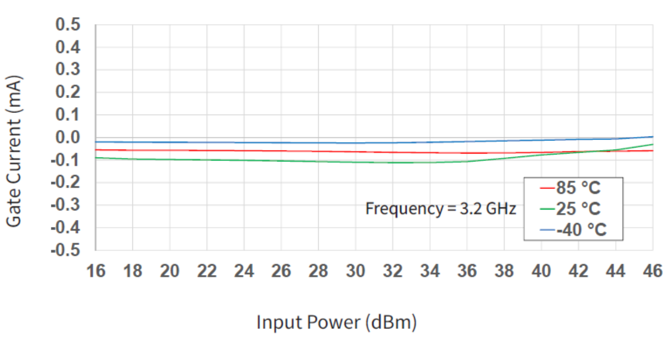

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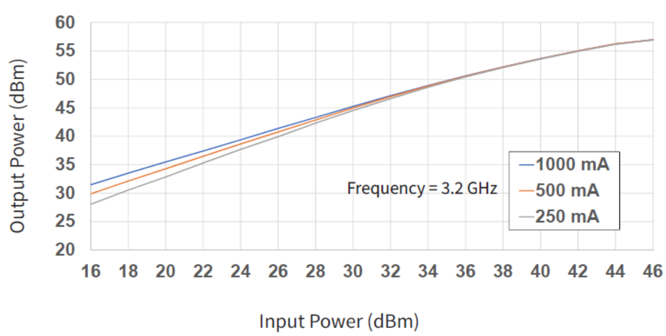
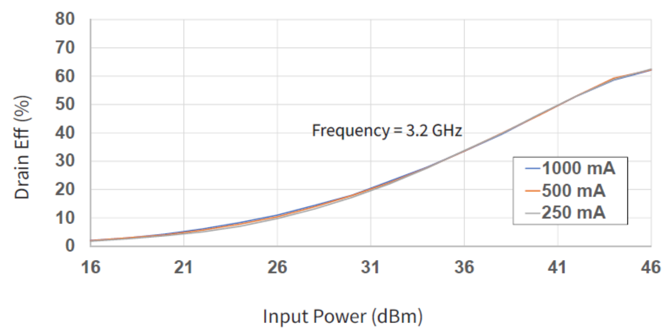
Output Power vs. Input Power Over I_{DQ}



Drain Efficiency vs. Input Power Over I_{DQ}



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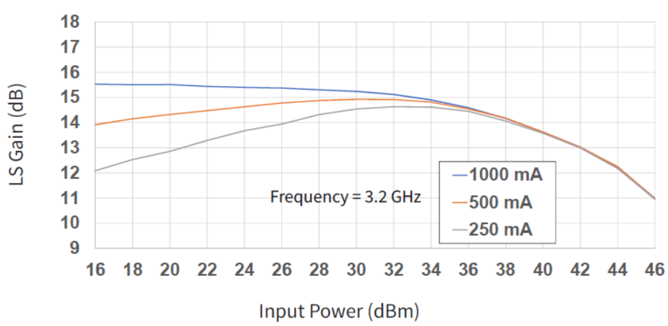

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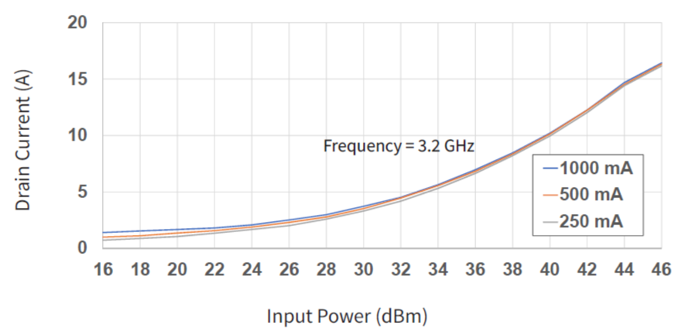

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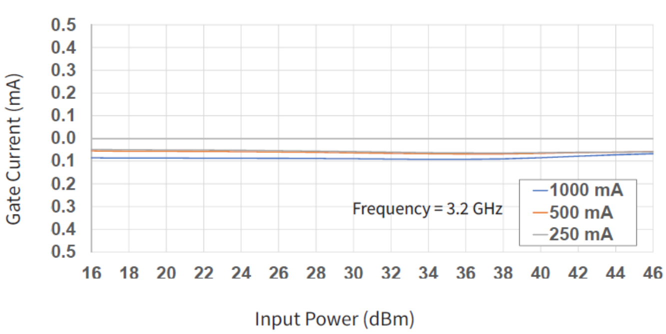

Typical Performance Curves:

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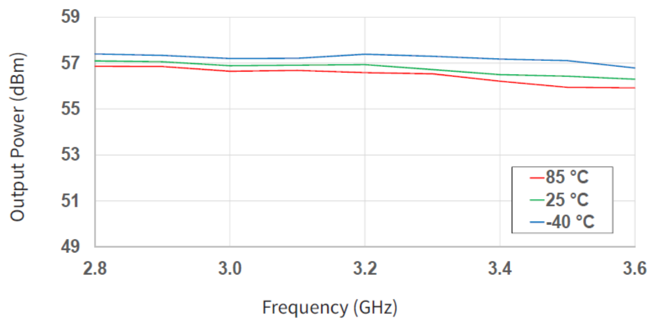
Output Power vs. Frequency over Temperature



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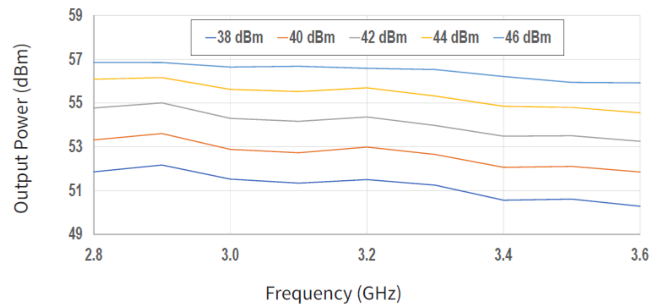
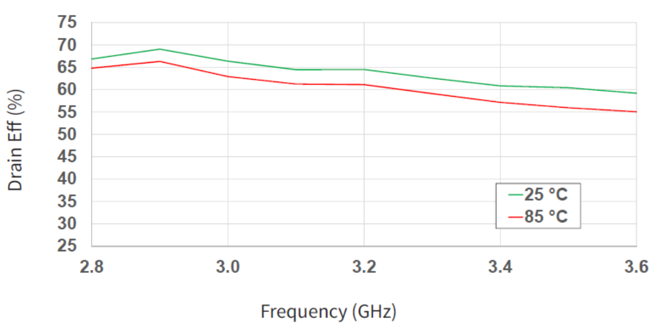


Drain Efficiency vs. Frequency over Temperature



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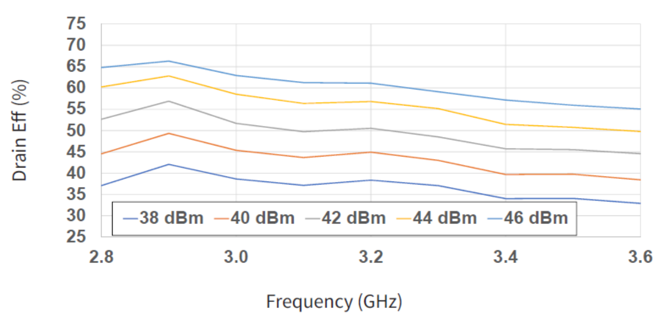

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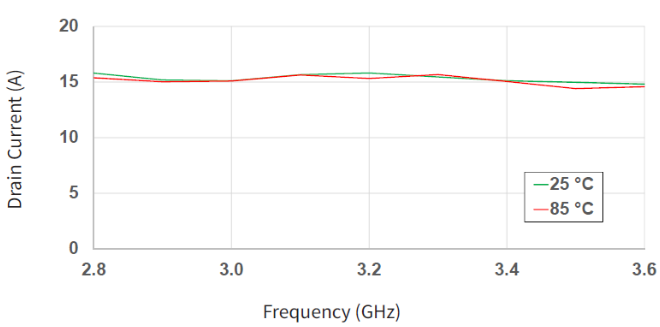

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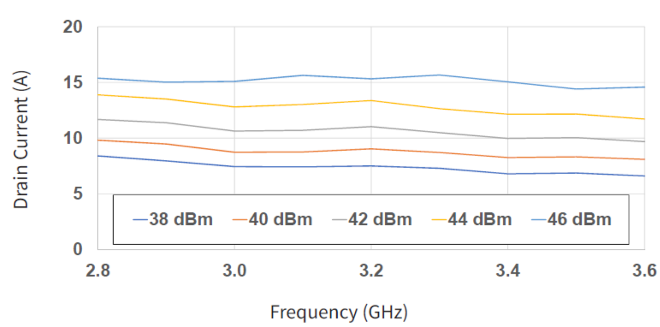

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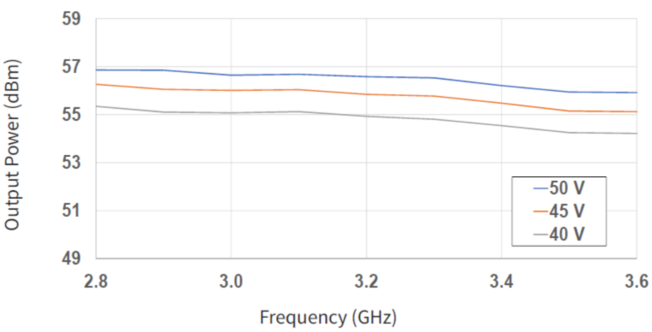
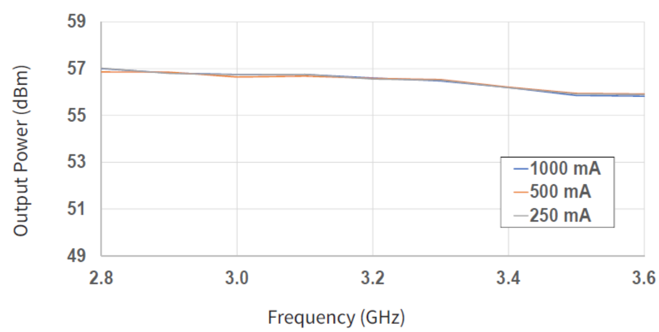
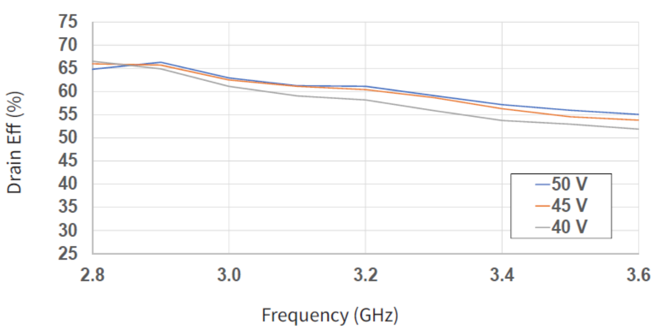
Output Power vs. Frequency over Voltage



Output Power vs. Frequency over I_{DQ}



Drain Efficiency vs. Frequency over Voltage



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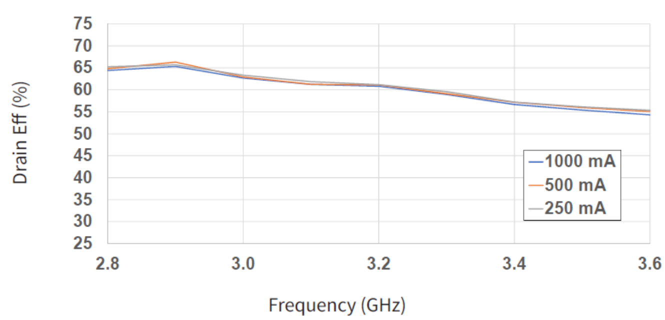
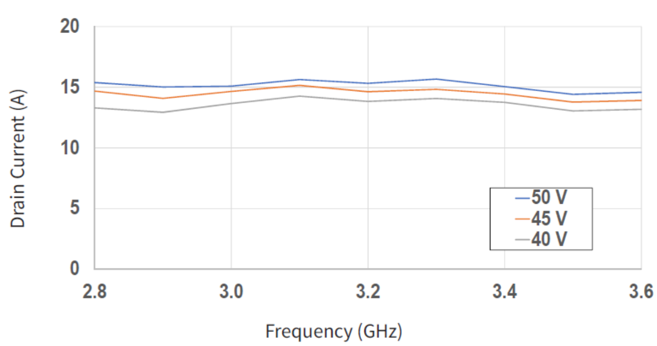
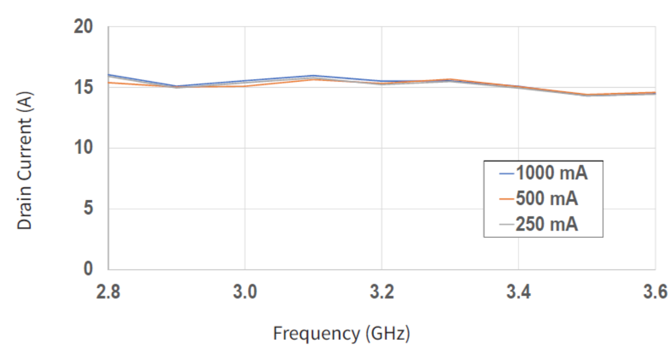


Drain Current vs. Frequency over Voltage



Drain Current vs. Frequency over I_{DQ}



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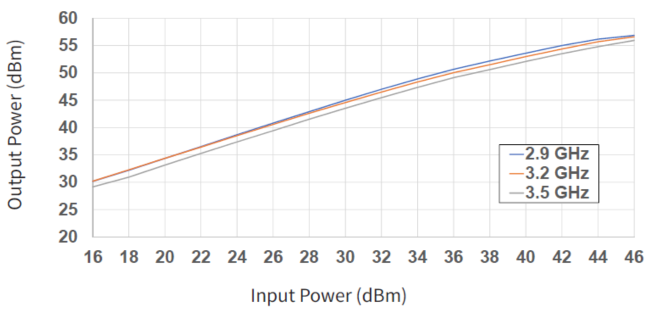
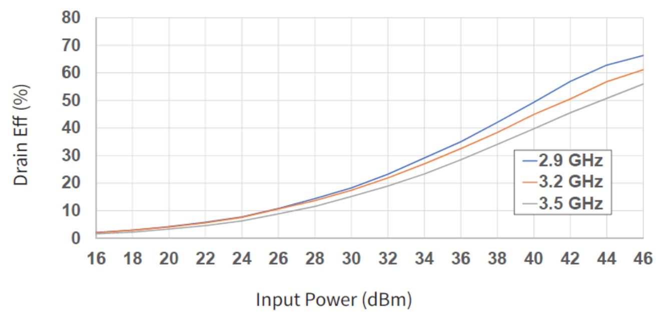
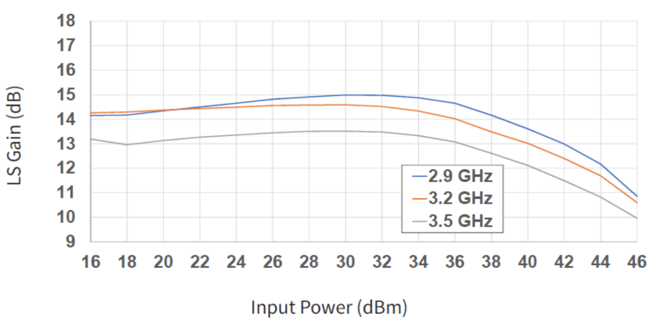
Output Power vs. Input Power over Frequency



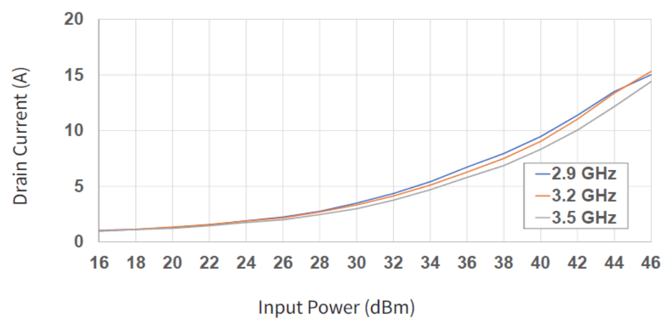
Drain Efficiency vs. Input Power over Frequency



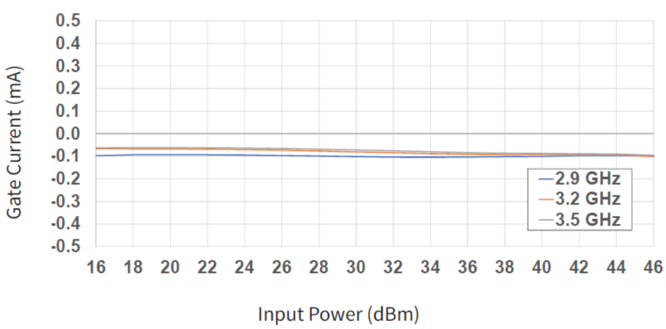
LS Gain vs. Input Power over Frequency



Drain Current vs. Input Power over Frequency



Gate Current vs. Input Power over Frequency



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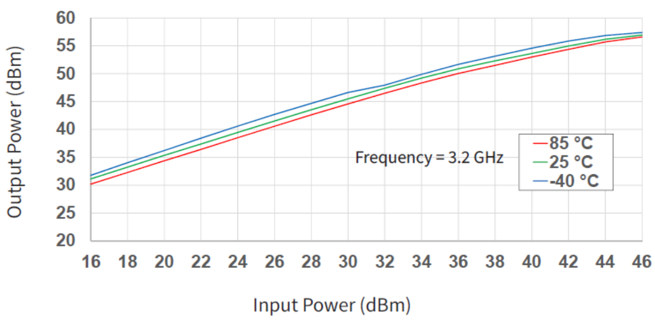
Output Power vs. Input Power over Temperature



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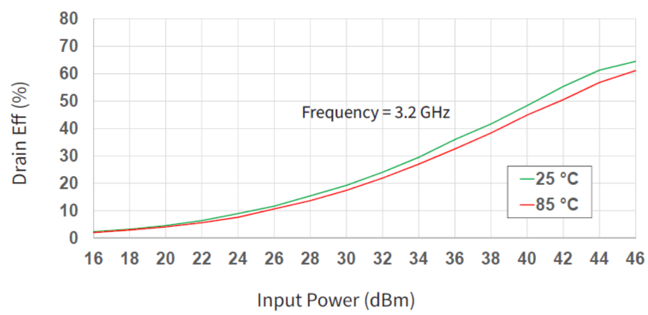

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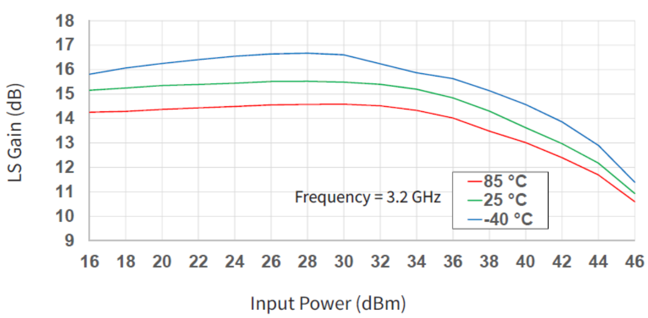

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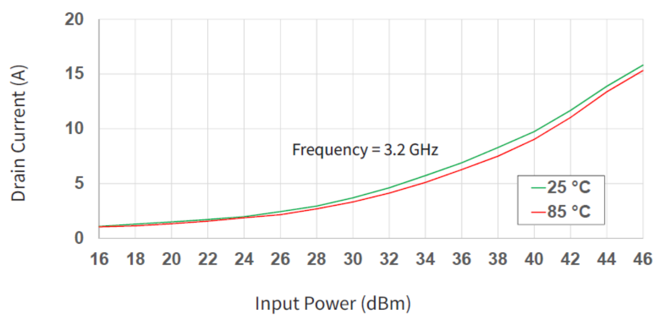

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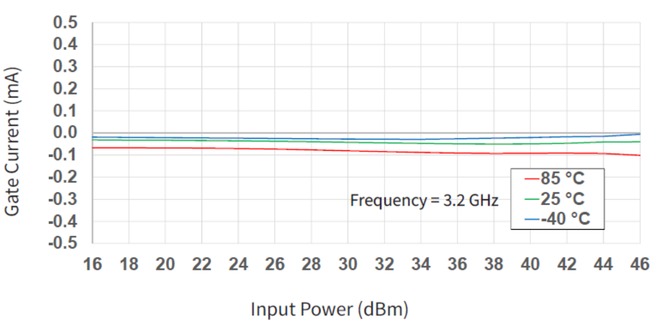

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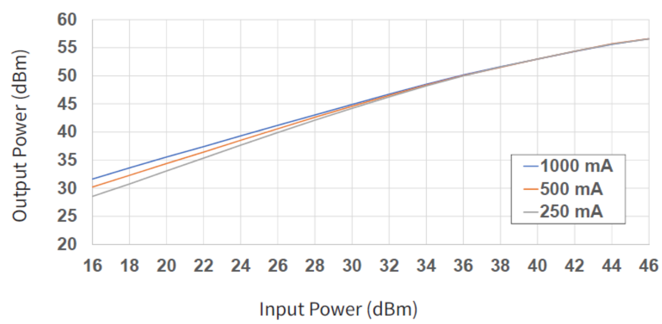

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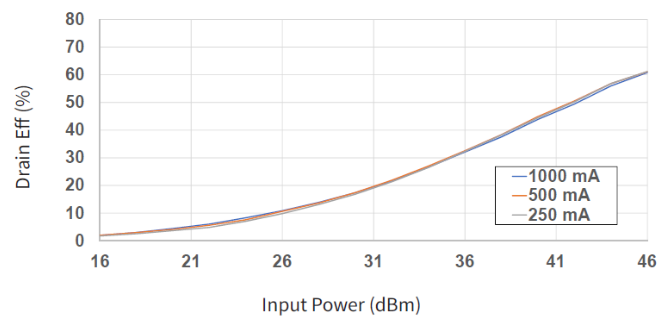

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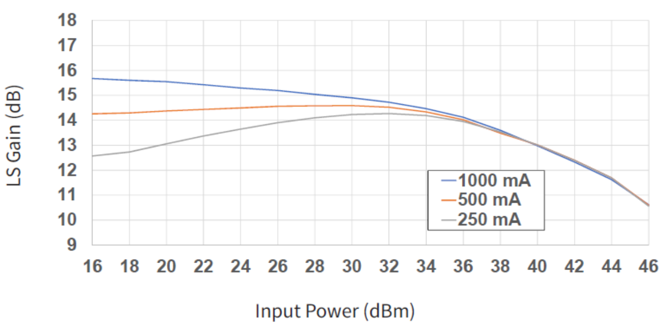
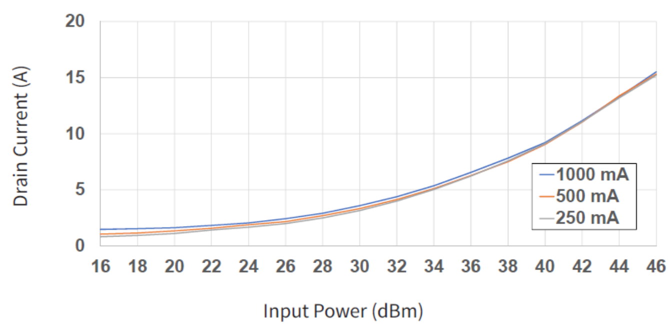
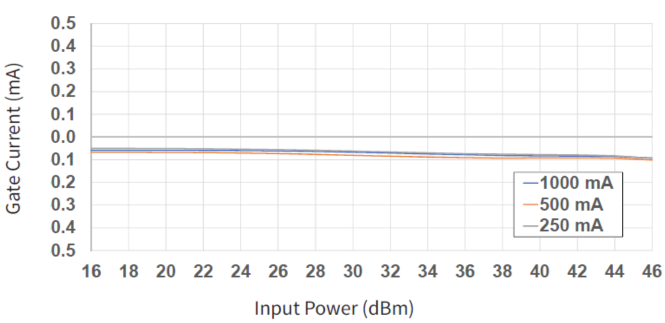


Drain Current vs. Input Power over I_{DQ}



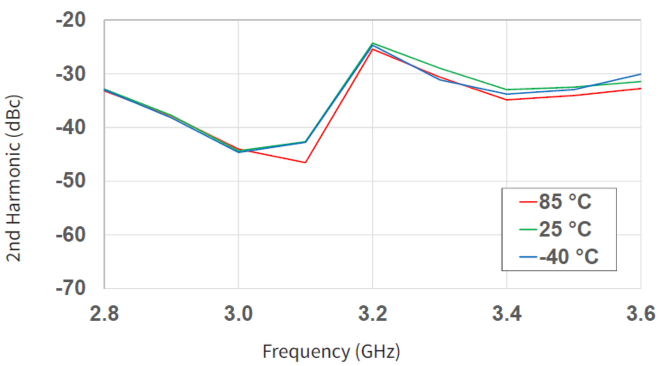
Gate Current vs. Input Power over I_{DQ}



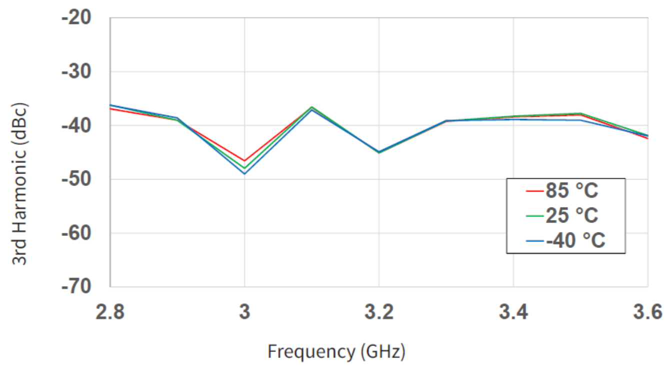
Typical Performance Curves:

V_D = 50 V, I_{DQ} = 500 mA, Pulse Width = 2 ms, Duty Cycle = 20%, P_{IN} = 46 dBm, T_B = +25°C

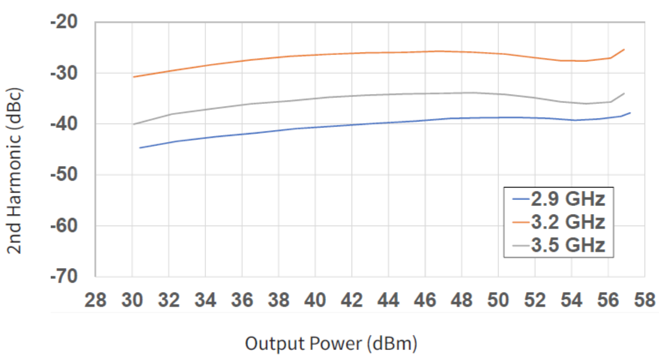
2nd Hamonic vs. Frequency over Temperature



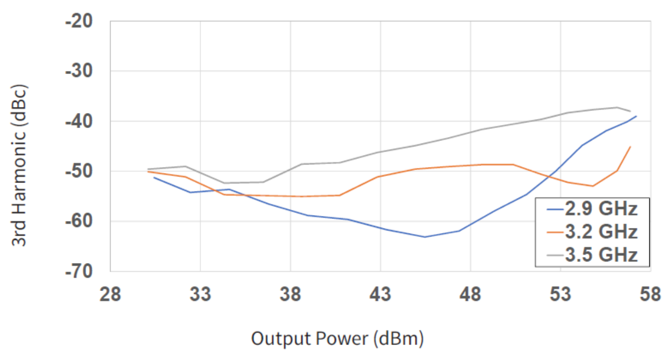
3rd Hamonic vs. Frequency over Temperature



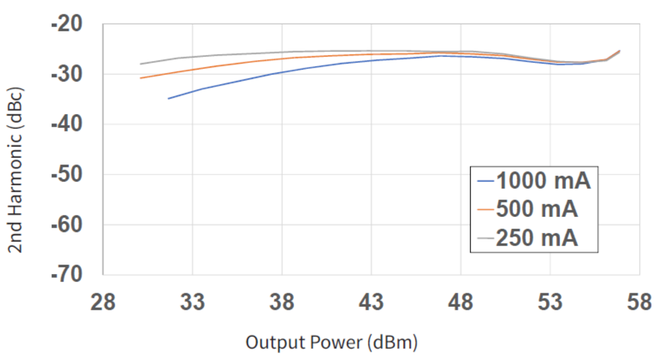
2nd Hamonic vs. Output Power over Frequency



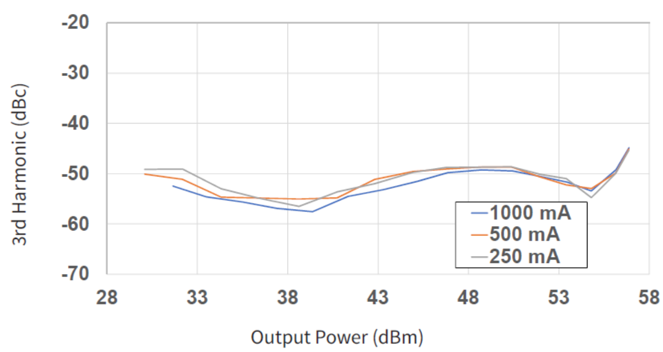
3rd Hamonic vs. Output Power over Frequency



2nd Hamonic vs. Output Power over I_{DQ}



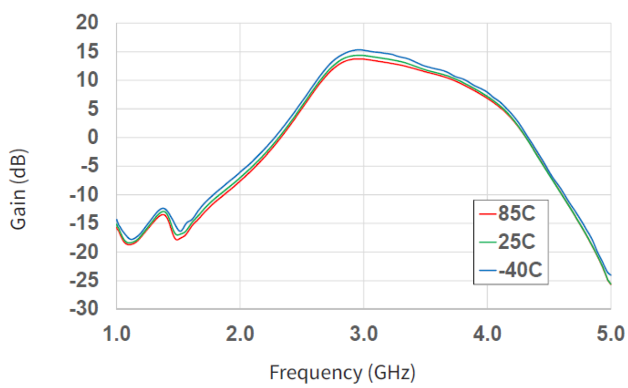
3rd Hamonic vs. Output Power over I_{DQ}



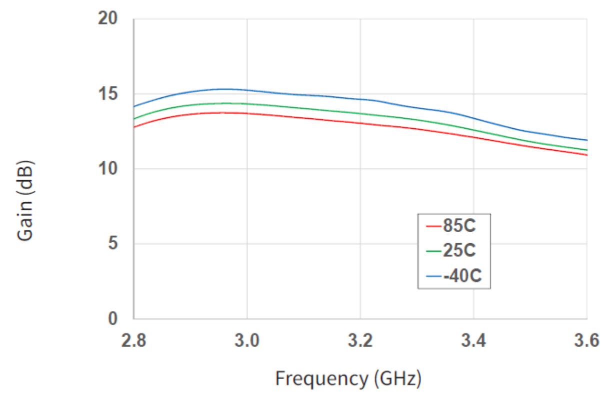
Typical Performance Curves:

V_D = 50 V, I_{DQ} = 500 mA, P_{IN} = -20 dBm, T_B = +25°C

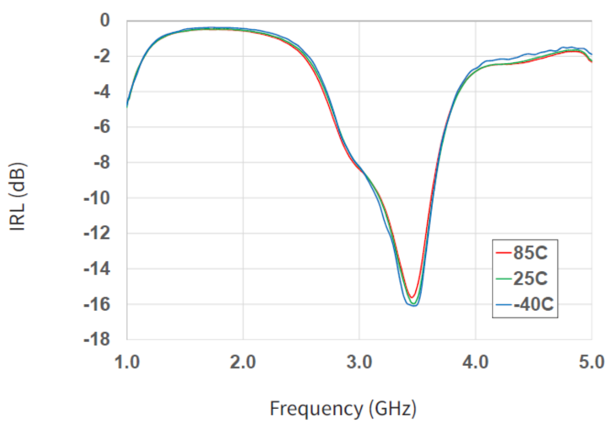
Gain vs. Frequency over Temperature



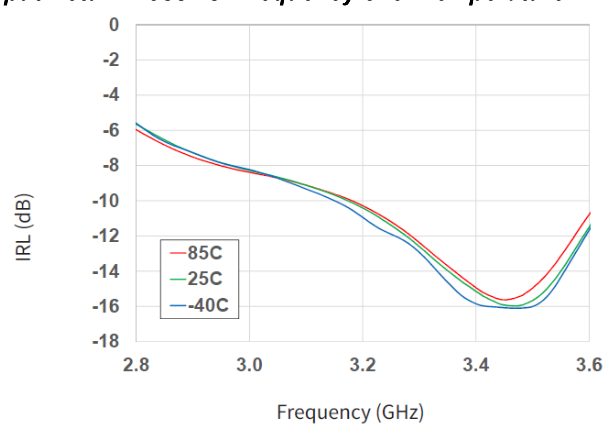
Gain vs. Frequency over Temperature



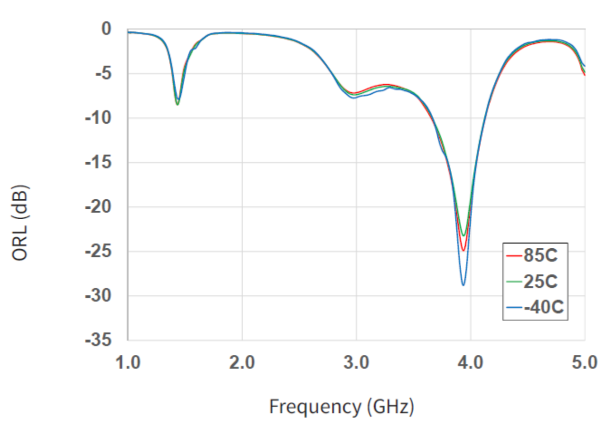
Input Return Loss vs. Frequency over Temperature



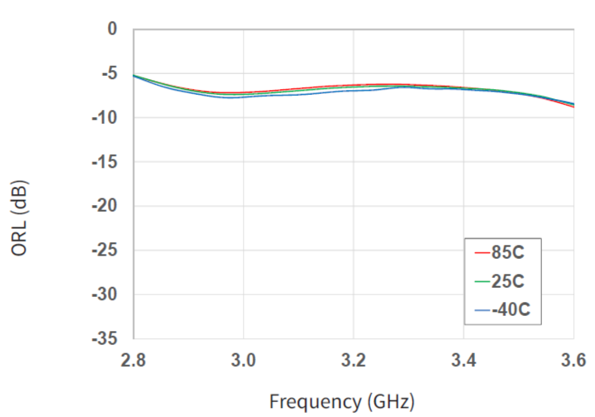
Input Return Loss vs. Frequency over Temperature



Output Return Loss vs. Frequency over Temperature



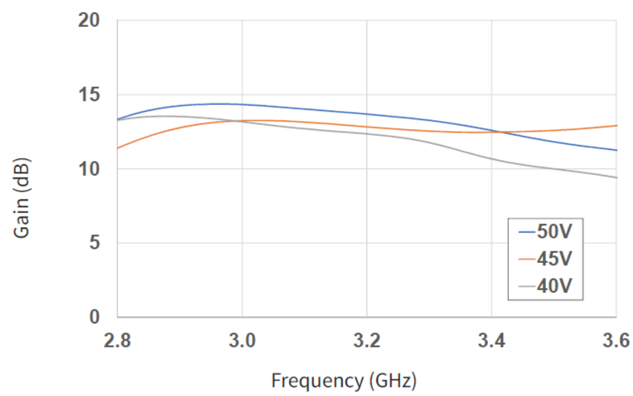
Output Return Loss vs. Frequency over Temperature



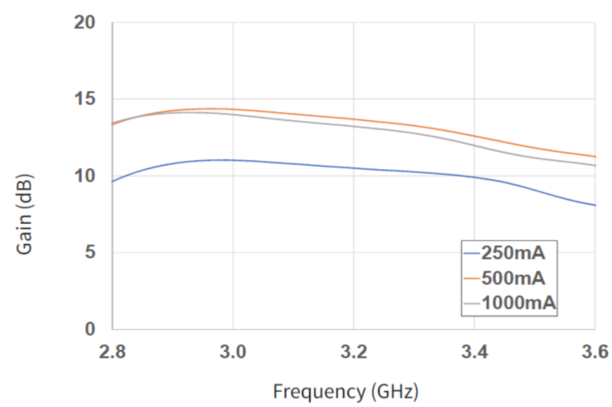
Typical Performance Curves:

V_D = 50 V, I_{DQ} = 500 mA, P_{IN} = -20 dBm, T_B = +25°C

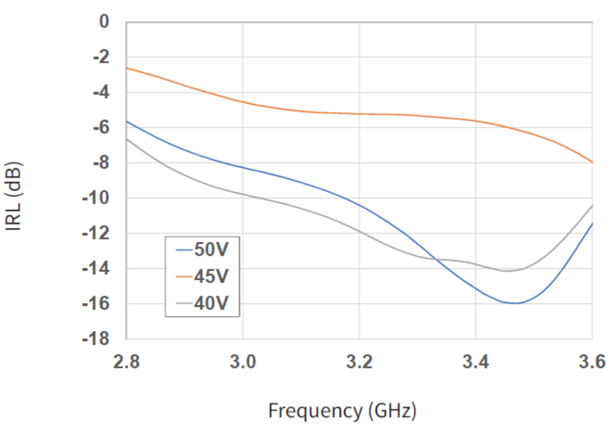
Gain vs. Frequency over Voltage



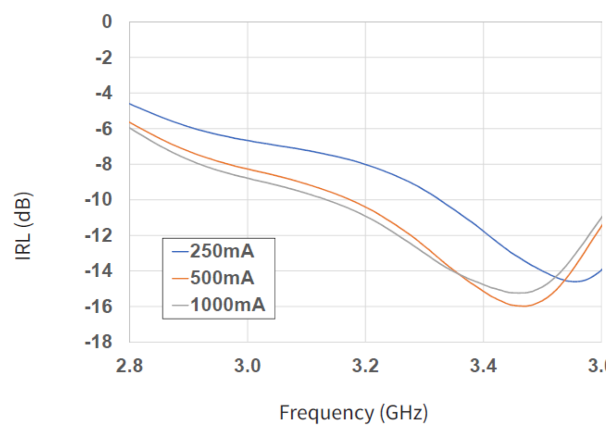
Gain vs. Frequency over I_{DQ}



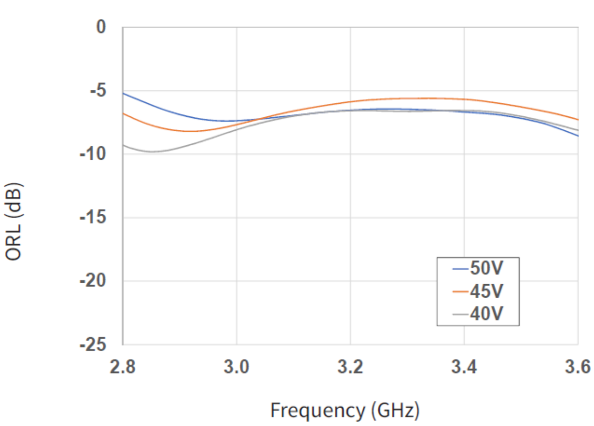
Input Return Loss vs. Frequency over Voltage



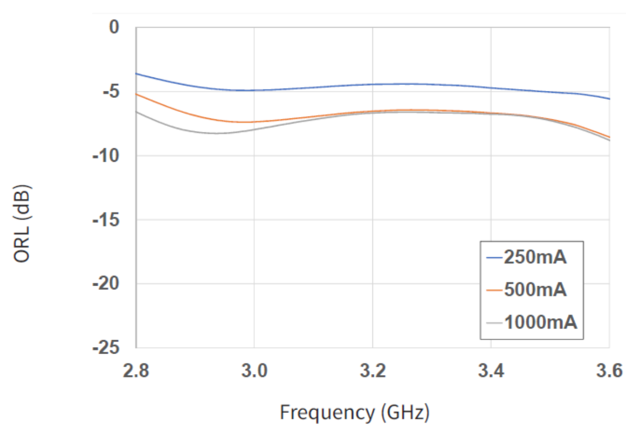
Input Return Loss vs. Frequency over I_{DQ}



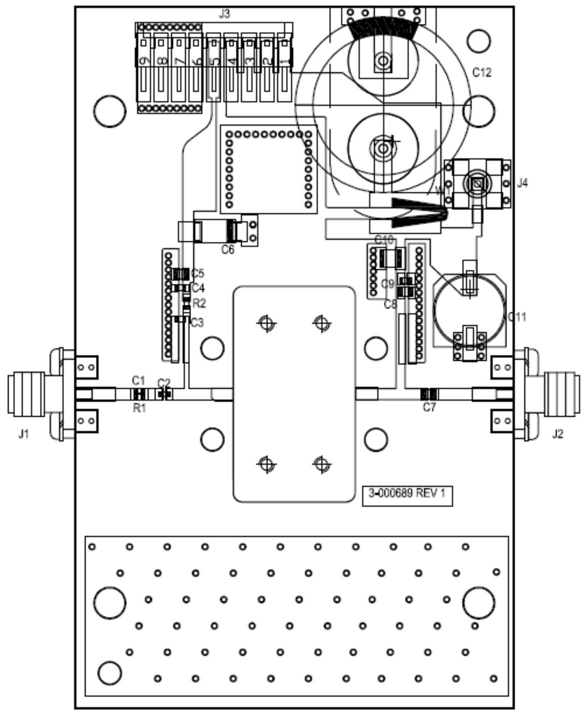
Output Return Loss vs. Frequency over Voltage



Output Return Loss vs. Frequency over I_{DQ}



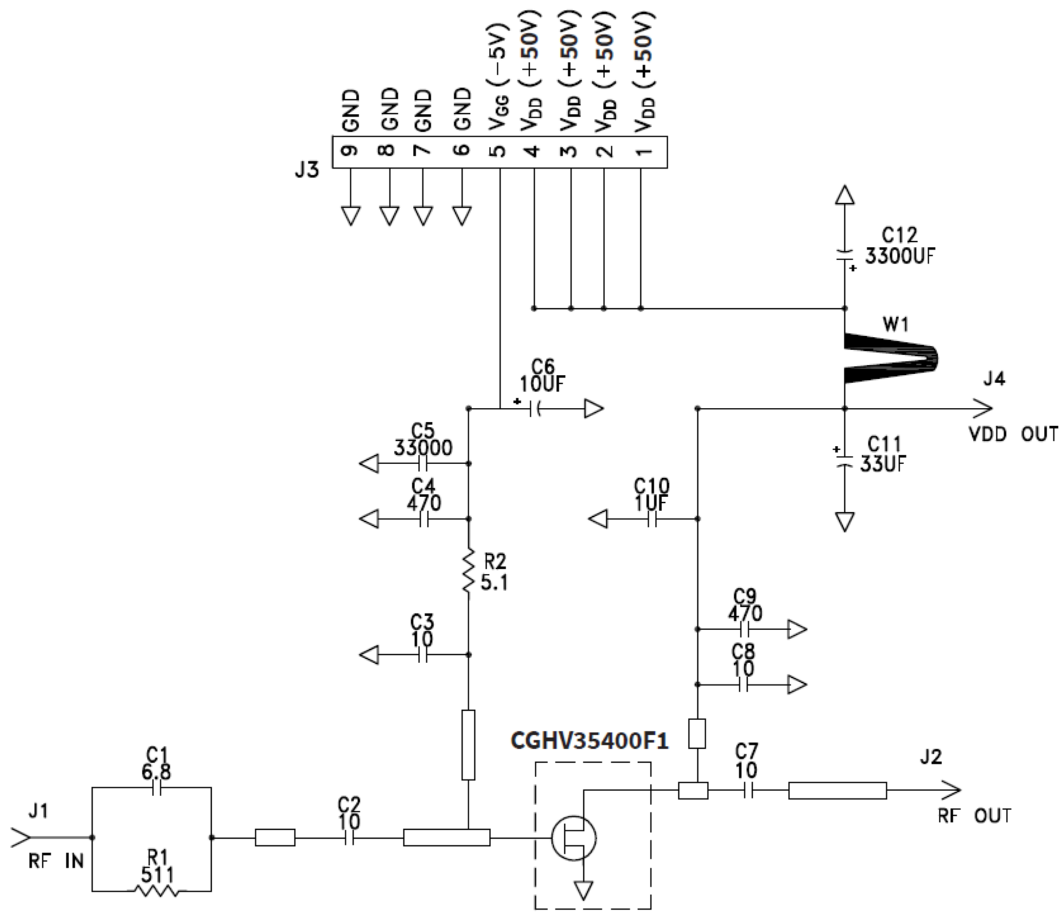
Assembly Drawing



Parts List

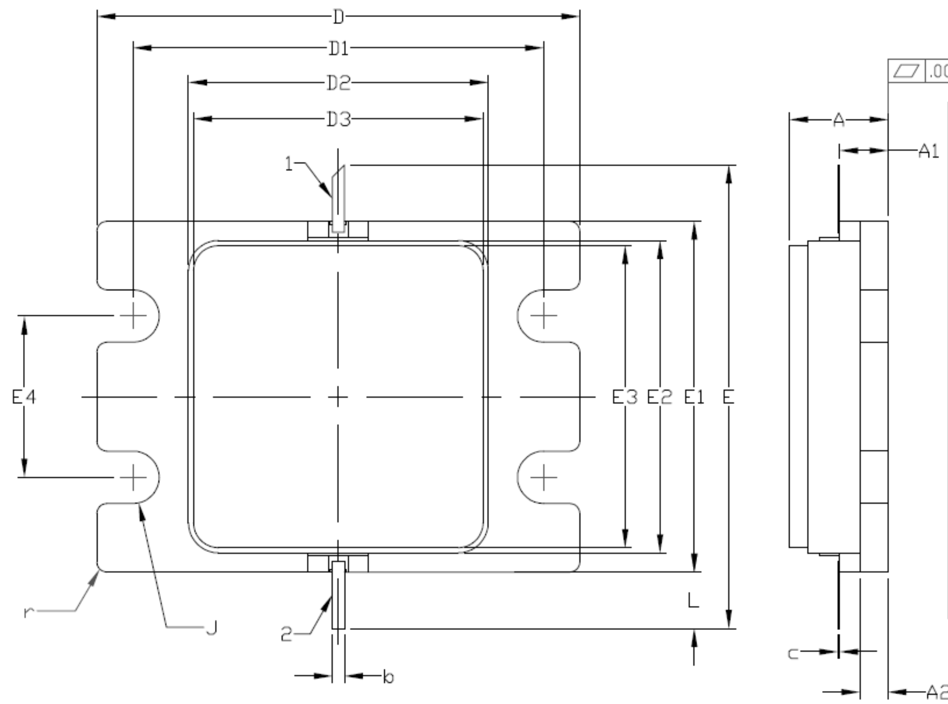
Designator	Description	QTY.
C1	CAP, 6.8 pF, +/-0.25%, 250V, 0603	1
C2, C7, C8	CAP, 10 pF, +/-1%, 250V, 0805	3
C3	CAP, 10 pF, +/-5%, 250V, 0603	1
C4, C9	CAP, 470 pF, 5%, 100V, 0603, X	2
C5	CAP, 33000 pF, 0805, 100V, X7R	1
C6	CAP, 10 µF, 16V, TANTALUM	1
C10	CAP, 1 µF, 100V, 10%, X7R, 1210	1
C11	CAP, 33 µF, 20%, G CASE	1
C12	CAP, 3300 µF, +/-20%, 100V, ELECTROLYTIC	1
J1, J2	CONN, SMA, PANEL MOUNT JACK, FL	2
J3	HEADER, RT>PLZ, 0.1CEN LK 9POS	1
J4	CONNECTOR; SMB, Straight, JACK, SMD	1
R1	RES, 511 Ω, +/- 1%, 1/16W, 0603	1
R2	RES, 5.1 Ω, +/- 1%, 1/16W, 0603	1
W1	CABLE, 18 AWG, 4.2	1
—	PCB, RO4350, 2.5 X 4.0 X 0.030	1
Q1	CGHV35400F1	1

Application Circuit Schematic



Product Dimensions (Package Type 440226)

NOTES: (UNLESS OTHERWISE SPECIFIED)
1. INTERPRET DRAWING IN ACCORDANCE WITH ANSI Y14.5M-2009
2. ADHESIVE FROM LID MAY EXTEND A MAXIMUM OF .020 BEYOND EDGE OF LID
3. LID MAY BE MISALIGNED TO THE BODY OF PACKAGE BY A MAXIMUM OF .008 IN ANY DIRECTION
4. ALL PLATED SURFACES ARE GOLD OVER NICKEL



1. GATE
2. DRAIN

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.185	0.201	4.70	5.11	
A1	0.088	0.100	2.24	2.54	2x
A2	0.049	0.061	1.24	1.55	
b	0.022	0.026	0.56	0.66	2x
c	0.003	0.006	0.08	0.15	
D	0.935	0.955	23.75	24.26	
D1	0.797	0.809	20.24	20.55	2x
D2	0.581	0.593	14.76	15.06	
D3	0.565	0.571	14.35	14.50	
E	0.906		23.01		REF
E1	0.679	0.691	17.25	17.55	
E2	0.604	0.616	15.34	15.65	
E3	0.588	0.594	14.93	15.09	
E4	0.309	0.321	7.85	8.15	2x
J	ø0.097	ø0.107	ø2.46	ø2.72	4x
L	0.090	0.130	2.29	3.30	2x
r	0.02 TYP		0.51 TYP		12x

Pin #	Description
1	Gate / RFIN
2	Drain / RFOUT
3	Source / Flange