

# 2N2221A, L, UA, UB & 2N2222A, L, UA, UB

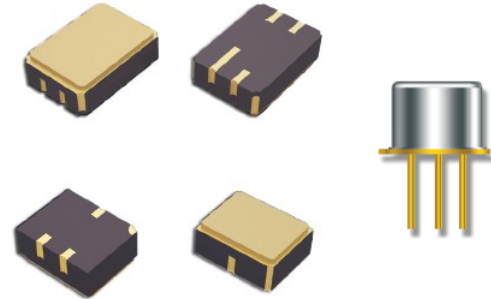


## Radiation Hardened NPN Silicon Switching Transistors

Rev. V1

### Features

- Qualified to MIL-PRF-19500/255
- Levels
  - JANSM-3K Rads (Si) JAN
  - JANSD-10K Rads (Si) JANTX
  - JANSP-30K Rads (Si) JANTXV
  - JANSL-50K Rads (Si) JAN
  - JANSR-100K Rads (Si)
- TO-18 (TO-206AA), Surface mount UA & UB Packages



### Applications

- Switching and Linear Applications
- DC and VHF Amplifier Applications

### Electrical Specifications @ $T_A = 25^\circ\text{C}$

Parameter	Test Conditions	Symbol	Units	Minimum	Maximum	
<b>Off Characteristics:</b>						
Collector - Emitter Breakdown	$I_C = 10 \text{ mAdc}$	$V_{(BR)CEO}$	Vdc	50	—	
Collector - Base Cutoff Current	$V_{CB} = 75 \text{ Vdc}$	$I_{CBO1}$	$\mu\text{Adc}$	—	10	
	$V_{CB} = 60 \text{ Vdc}$	$I_{CBO2}$	nAdc	—	10	
Emitter - Base Cutoff Current	$V_{EB} = 6.0 \text{ Vdc}$	$I_{EBO1}$	$\mu\text{Adc}$	—	10	
	$V_{EB} = 4.0 \text{ Vdc}$	$I_{EBO2}$	nAdc	—	10	
Collector - Emitter Cutoff Current	$V_{CE} = 50 \text{ Vdc}$	$I_{CES}$	nAdc	—	50	
<b>On Characteristics<sup>1</sup>:</b>						
Forward Current Transfer Ratio	2N2221A, L, UA, UB		hFE			
	$I_C = 0.1 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}$			30	—	
	$I_C = 1.0 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}$			35	150	
	$I_C = 10.0 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}$			40	—	
	$I_C = 150.0 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}$			40	120	
	$I_C = 500.0 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}$			20	—	
	2N2222A, L, UA, UB					
	$I_C = 0.1 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}$			50	—	
	$I_C = 1.0 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}$			75	325	
	$I_C = 10.0 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}$			100	11	
Collector - Base Cutoff Current	$I_C = 150 \text{ mAdc}, I_B = 15 \text{ mAdc}$	$V_{CE(sat)}$	Vdc	—	0.3	
	$I_C = 500 \text{ mAdc}, I_B = 50 \text{ mAdc}$				1.0	
Base - Emitter Saturation Voltage	$I_C = 150 \text{ mAdc}, I_B = 15 \text{ mAdc}$	$V_{BE(sat)}$	Vdc	0.6	1.2	
	$I_C = 500 \text{ mAdc}, I_B = 50 \text{ mAdc}$			—	2.0	

1. Pulse Test: Pulse Width = 300 ms, Duty Cycle < 2%.

(Continued next page)

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### Electrical Specifications @ $T_A = 25^\circ\text{C}$

Parameter	Test Conditions	Symbol	Units	Minimum	Maximum
<b>Dynamic Characteristics:</b>					
Small-Signal Short-Circuit Forward Current Transfer Ratio	$I_C = 1 \text{ mAdc}$ , $V_{CE} = 10 \text{ Vdc}$ , $f = 1 \text{ kHz}$ 2N2221A, L, UA, UB 2N2222A, L, UA, UB	hfe		30 50	—
Magnitude of Small-Signal Short-Circuit, Forward Current Transfer Ratio	$I_C = 20 \text{ mAdc}$ , $V_{CE} = 20 \text{ Vdc}$ , $f = 100 \text{ MHz}$	hfe		2.5	—
Output Capacitance	$V_{CB} = 10 \text{ Vdc}$ , $I_E = 0$ , $100 \text{ kHz} \leq f \leq 1 \text{ MHz}$ $V_{CB} = 0.5 \text{ Vdc}$ , $I_E = 0$ , $100 \text{ kHz} \leq f \leq 1 \text{ MHz}$	$C_{OBO}$ $C_{1BO}$	pF	—	8 25
<b>Switching Characteristics:</b>					
Turn-On Time	(See figure 17 of MIL-PRF-19500/255)	$T_{ON}$	ns	—	35
Turn-Off Time	(See Figure 18 of MIL-PRF-19500/255)	$T_{OFF}$	ns	—	300

### Absolute Maximum Ratings @ $T_C = 25^\circ\text{C}$

Parameter	Absolute Maximum
Collector - Emitter Voltage ( $V_{CEO}$ )	50 Vdc
Collector - Base Voltage ( $V_{CBO}$ )	75 Vdc
Emitter - Base Voltage ( $V_{EBO}$ )	6.0 Vdc
Collector Current ( $I_C$ )	800 mAdc
Total Power Dissipation ( $P_T$ ) $T_A = +25^\circ\text{C}$	0.5 W
Thermal Resistance ( $R_{\theta JC}$ ) Junction to Ambient	325 $^\circ\text{C/W}$
Operating Temperature	-65 $^\circ\text{C}$ to +200 $^\circ\text{C}$
Storage Temperature	-65 $^\circ\text{C}$ to +200 $^\circ\text{C}$

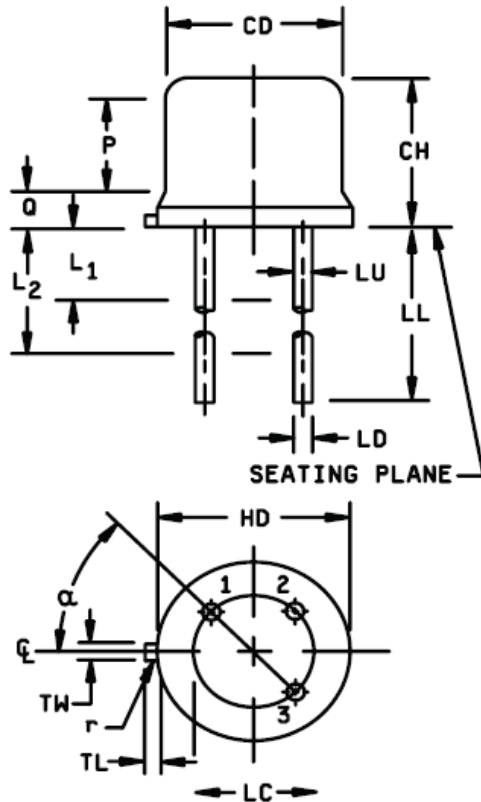
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### Outline Drawing (TO-18):



Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min.	Max.	Min.	Max.	
CD	0.178	0.195	4.52	1.95	—
CH	0.170	0.210	4.32	5.33	—
HD	0.209	0.230	5.31	5.84	—
LC	0.100 Typ.		2.54 Typ		6
LD	0.016	0.021	0.41	0.53	7, 8
LL	0.500	0.750	12.70	19.05	7, 8, 13
LU	0.016	0.019	0.41	0.48	7, 8
L1	—	0.050	—	1.27	7, 8
L2	0.250	—	6.35	—	7, 8
P	0.100	—	2.54	—	—
Q	—	0.030	—	0.76	5
TL	0.028	0.048	0.71	1.22	3, 4
TW	0.036	0.046	0.91	1.17	3
r	—	0.010	—	0.25	10
a	45° Typ.				6
1, 2, 9, 11, 12, 13					

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Beyond r (radius) maximum, TL shall be held for a minimum length of .011 inch (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
6. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within 0.007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC.
7. Dimension LU applies between L1 and L2. Dimension LD applies between L2 and LL minimum. Diameter is uncontrolled in L1 and beyond LL minimum.
8. All three leads.
9. The collector shall be internally connected to the case.
10. Dimension r (radius) applies to both inside corners of tab.
11. In accordance with ASME Y14.5M, diameters are equivalent to  $\Phi x$  symbology.
12. Lead 1 = emitter, lead 2 = base, lead 3 = collector.
13. For L suffix devices, dimension LL = 1.5 inches (38.10 mm) min. and 1.75 inches (44.45 mm) max.

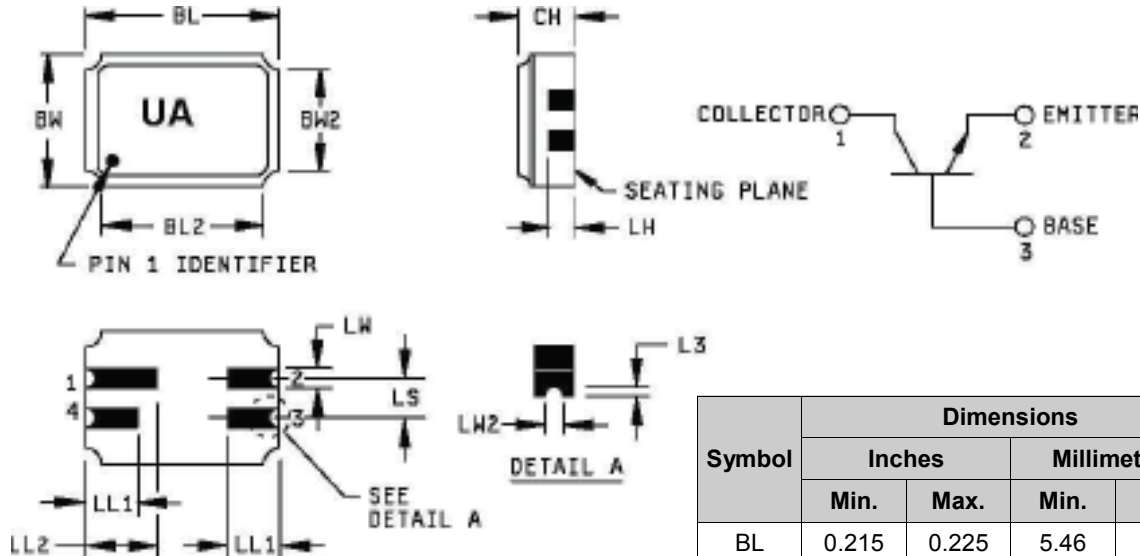
# 2N2221A, L, UA, UB & 2N2222A, L, UA, UB



## Radiation Hardened NPN Silicon Switching Transistors

Rev. V1

### Outline Drawing (UA Surface Mount):



Pin #	1	2	3	4
Transistor	Collector	Emitter	Base	N/C

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min.	Max.	Min.	Max.	
BL	0.215	0.225	5.46	5.71	—
BL2	—	0.225	—	5.71	—
BW	0.145	0.155	3.68	3.93	—
BW2	0.155		3.93		—
CH	0.061	0.075	1.55	1.90	3
L3	0.003	0.007	0.08	0.18	5
LH	0.029	0.042	0.74	1.07	—
LL1	0.032	0.048	0.81	1.22	—
LL2	0.072	0.088	1.83	2.23	—
LS	0.045	0.055	1.14	1.39	—
LW	0.022	0.028	0.56	0.71	—
LW2	0.006	0.022	0.15	0.56	5

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Dimension CH controls the overall package thickness. When a window lid is used, dimension CH must increase by a minimum of .010 inch (0.254 mm) and a maximum of .040 inch (1.020 mm).
4. The corner shape (square, notch, radius) may vary at the manufacturer's option, from that shown on the drawing.
5. Dimensions LW2 minimum and L3 minimum and the appropriate castellation length define an unobstructed three-dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on the bottom two layers, optional on the top ceramic layer.) Dimension LW2 maximum and L3 maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dipping.
6. The co-planarity deviation of all terminal contact points, as defined by the device seating plane, shall not exceed .006 inch (0.15 mm) for solder dipped leadless chip carriers.
7. In accordance with ASME Y14.5M, diameters are equivalent to  $\Phi x$  symbology.

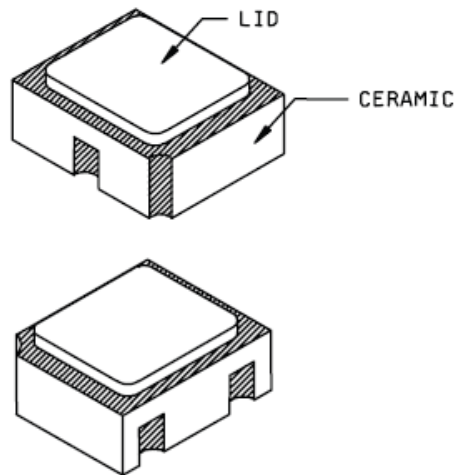
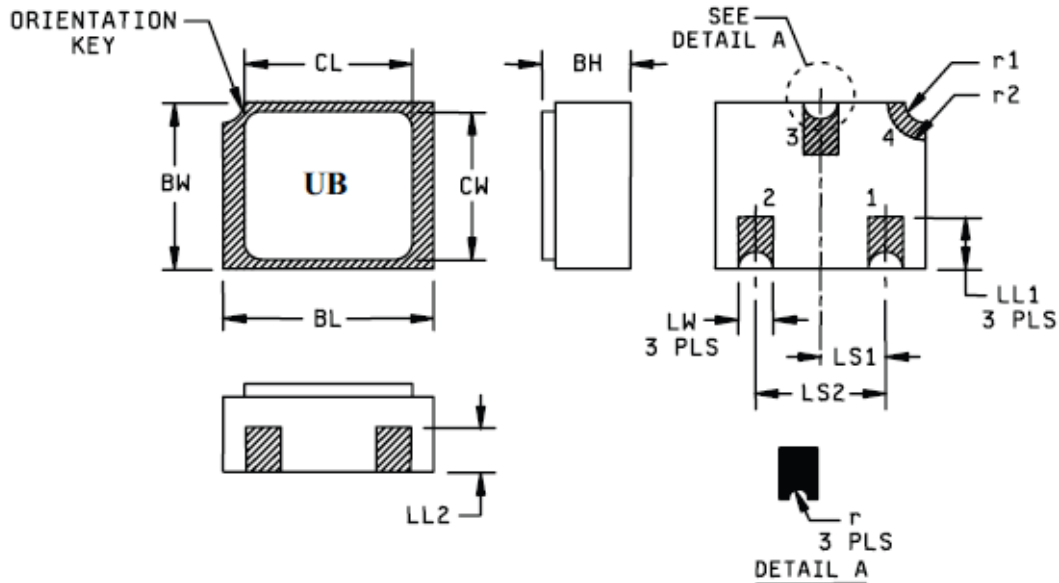
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### Outline Drawing (UB Surface Mount):



Symbol	Dimensions			
	Inches		Millimeters	
	Min.	Max.	Min.	Max.
BH	0.046	0.056	1.17	1.42
BL	0.115	0.128	2.92	3.25
BW	0.085	0.108	2.16	2.74
CL	—	0.128		3.25
CW		0.108		2.74
LL1	0.022	0.038	0.56	0.96
LL2	0.017	0.035	0.43	0.89
LS1	0.036	0.040	0.91	1.02
LS2	0.071	0.079	1.81	2.01
LW	0.016	0.024	0.41	0.61
r	—	0.008	—	0.203
r1	—	0.012	—	0.305
r2	—	0.022	—	0.559

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Hatched areas on package denote metalized areas.
4. Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Pad 4 = Shielding connected to the lid.
5. In accordance with ASME Y14.5M, diameters are equivalent to  $\Phi x$  symbology.

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