M21544, M21554, M21564

3G/HD/SD-SDI Long Reach Adaptive Cable Equalizer with Integrated Jitter Cleaner

The M21544/54/64 are multi-rate, highly integrated, adaptive cable equalizers for SDI and DVB-ASI video as well as digital audio applications. It provides adaptive, low noise, high gain equalization for 75 Ω coaxial cable at SDI data rates from 125 Mbps to 2.97 Gbps. The device is capable of compensating for losses accumulated across cable length up to 200 m when operating at 2.97 Gbps.

The M21544/54/64 feature an integrated jitter cleaner, which automatically removes the jitter generated at HD-SDI and 3G-SDI at the output of the equalizer, eliminating the need for standalone reclockers at the input and reducing system cost, complexity and power consumption. The jitter cleaner may be powered down and bypassed in applications where it is not required to allow for optimized power consumption for each application.

The M21544/54 also feature dual differential outputs, eliminating the need for additional circuitry and simplifying system design. Both outputs feature programmable swing as well as de-emphasis for enabling the signal to be transmitted across 40" of FR4 trace. The second, optional output may be disabled for additional power savings. The M21564 offers a single output solution with a smaller footprint and maximum power savings.

The device operates using a single 2.5 V supply voltage and has extremely low power consumption with the equalizer and jitter cleaner dissipating only 145 mW when one output driver is enabled. It may be used in either hardware mode, or controlled through a standard four-wire serial digital interface. Furthermore, it features advanced diagnostic capabilities such as cable length indication, loss of signal detection, and offers power management functions such as power down upon loss of signal.

The M21544/54/64 are offered in a green and RoHS compliant small footprint QFN package.

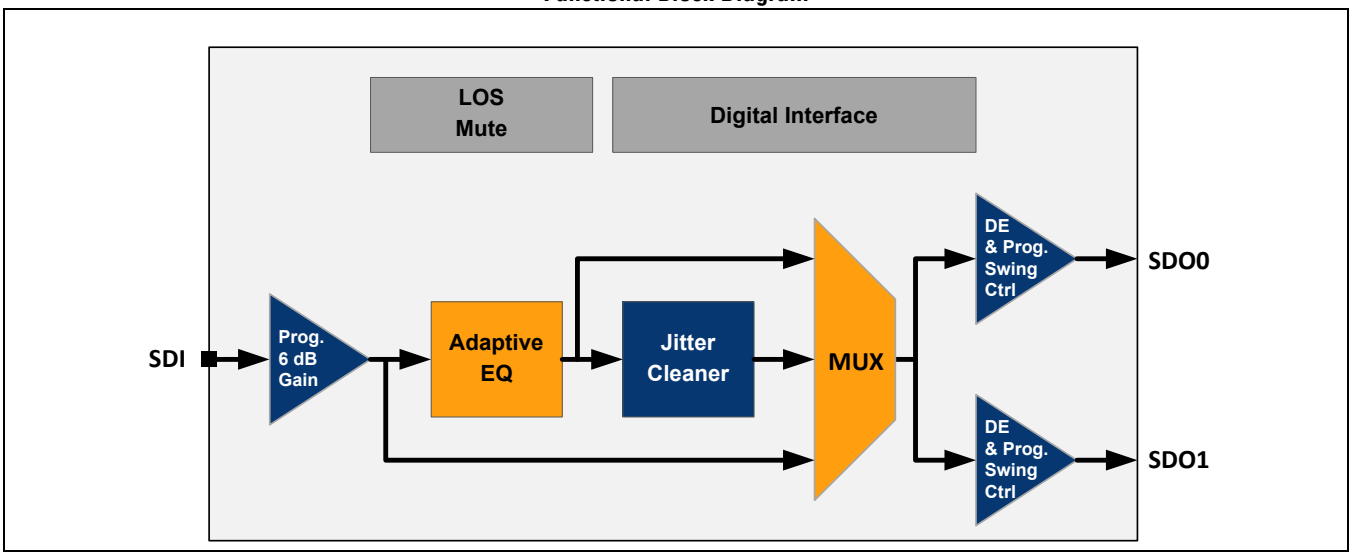
Features

- SMPTE 424M, SMPTE 292M, SMPTE 344M, SMPTE 259M, and DVB-ASI compliant
- Robust adaptive cable equalization for up to 200 meters of Belden 1694A at 2.97 Gbps, up to 200 meters of Belden 1694A at 1.485 Gbps, and up to 400 meters of Belden 1694A at 270 Mbps
- Integrated jitter cleaner for 3G/HD-SDI use with automatic rate detection
- Individually controllable dual differential output drivers with programmable 8 dB of de-emphasis
- Optional 6 dB flatband gain at input
- Cable length indication
- SD, HD and 3G Data Rate Detection
- Optional four-wire serial digital interface
- Very low power consumption: 145 mW (single output), 160 mW (dual output)
- Power down and mute features
- Extended operating temperature range: -40 °C to +85 °C

Applications

- Broadcast video routing and production switchers
- Broadcast video distribution amplifiers
- Broadcast video cameras and monitors

Functional Block Diagram



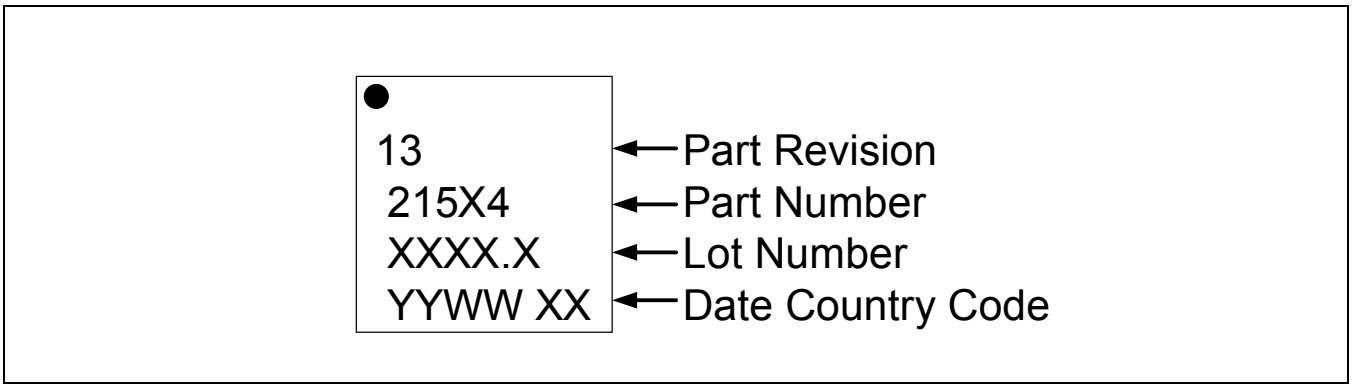
Ordering Information

Part Number	Package	Operating Data Rate	Operating Temperature
M21544G-13*	24-pin QFN (RoHS compliant)	125–2970 Mbps	–40 °C to 85 °C
M21554G-13*	32-pin QFN (RoHS compliant)	125–2970 Mbps	–40 °C to 85 °C
M21564G-13*	16-pin QFN (RoHS compliant)	125–2970 Mbps	–40 °C to 85 °C
* The letter 'G' designator after the part number indicates a RoHS-compliant package. Refer to www.mindspeed.com for additional information.			

Revision History

Revision	Level	Date	Description
E	Release	June 2013	Updated ordering information and marking diagram Updated electrical specifications including maximum power consumption and Jitter Performance Chapter 1.0 Added Figure 2-1 and Figure 2-2. Revised xCS pin description for all three devices in Section 3.0. Updated M21544 pins 17, 18 descriptions.
D	Advance	November	Updated Ordering information from -11P to -12P Added Marking Diagram Updated typical power consumption Table 1-3 Updated typical electrical specifications Table 1-4 Updated M21554 Pinout, Figure 3-3 Updated M21554 Pin Specifications, Table 3-2 Added 6 dB attenuation in the functional description Section 4.1.3 Updated Digital Interface functional description Section 4.5 Updated 4-Wire specifications Table 4-6
C	Advance	September 2012	Added Figure 2-1 and Figure 2-2. Revised xCS pin description for all three devices in Section 3.0. Pins 17, 18 revised for M21554.
B	Advance	May 2012	Added electrical specifications, pinout diagram, pin descriptions, package drawings, functional description and register settings.
A	Advance	June 2011	Advance Release.

M21544/54/64 Marking Diagram



1.0 Electrical Characteristics

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
AV_{DD}	Analog power supply voltage	-0.5	2.75	V
$V_{IN,PCML}$	DC input voltage (PCML)	V_{SS} - 0.5	AV_{DD} + 0.5	V
$V_{IN,CMOS}$	DC input voltage (CMOS)	V_{SS} - 0.6	DV_{DD} + 0.5	V
T_{STORE}	Storage temperature	-65	150	°C
T_{JUNC}	Junction temperature	—	125	°C
$V_{ESD,HBM}$	Electrostatic discharge voltage (HBM)	-3000	3000	V
$V_{ESD,CDM}$	Electrostatic discharge voltage (CDM)	-500	500	V
$V_{ESD,}$mm	Electrostatic discharge voltage (mm)	-150	150	V

NOTES:

1. Exposure of the device beyond the minimum/maximum limits may cause permanent damage.
2. HBM and CDM per JEDEC Class 2 (JESD22-A114-B).
3. Limits listed in the above table are stress limits only and do not imply functional operation within these limits.

Table 1-2. Recommended Operating Conditions

Symbol	Parameter		Minimum	Typical	Maximum	Unit
V_{CC}	Analog power supply voltage		2.37	2.5	2.63	V
T_{CASE}	Operating case temperature		-40	—	85	°C
θ_{JC}	Junction to case thermal resistance	M21544/64	—	—	13.8	°C/W
		M21554	—	—	11.5	°C/W

NOTES:

1. Thermal resistance value is calculated using a 5% increase on the supply voltage and includes all temperature variations.

Table 1-3. Power Consumption Specifications (1 of 2)

Symbol	Parameter		Typical	Maximum	Unit
I_{CC} Core Current Consumption	Intermediate output swing (Default)	Two outputs enabled	62	75	mA
		One output enabled	56	68	mA
	Maximum output swing	Two outputs enabled	64	78	mA
		One output enabled	57	70	mA

Table 1-3. Power Consumption Specifications (2 of 2)

Symbol	Parameter		Typical	Maximum	Unit
P_{TOTAL}	Intermediate swing (Default)	Two outputs enabled	155	197	mW
		One output enabled	140	179	mW

NOTES:

1. Maximum current and maximum power consumption numbers are calculated using a 5% increase on the supply voltage, with jitter cleaner and include all temperature and process variations.

Table 1-4. PCML Input/Output Electrical Characteristics (1 of 2)

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
DR	NRZ data rate		125	—	2970	Mbps
V_{IN}	Differential input swing		720	800	880	mV_{PP}
R_{IN}	Input termination resistance		—	2.3	—	kΩ
C_{IN}	Input Capacitance		—	0.4	—	pF
S_{11}	Input Return Loss from 5 MHz to 1.5 GHz		—	—	-15	dB
S_{11}	Input Return Loss from 1.5 GHz to 3 GHz		—	—	-10	dB
V_{OUT}	Differential output swing	1	250 390 540	365 555 740	480 720 940	mV_{PPD}
V_{OCM}	Output Common Mode Voltage	1	0.8	—	1.2	V
t_R/t_F	Output rise/fall time (20% - 80%)	2	—	90	130	ps
DE	Highest output de-emphasis setting	3	0	—	8	dB
Jitter Performance						
t_{JIT}	Total jitter added at 2.97 Gbps for the following Belden 1694A cable length 0 - 200 m	4, 5, 6	—	 100	 170	mUI
	Total jitter added at 1.485 Gbps for the following Belden 1694A cable length 0 - 200 m	4, 5, 6	—	 50	 100	mUI
	Total jitter added at 270 Mbps for the following Belden 1694A cable length 0 - 400 m	4, 5, 6	—	—	 300	mUI
Jitter Cleaner						
DR	Input data rate retimed, SMPTE 292M		—	1483, 1485	—	Mbps
DR	Input data rate retimed, SMPTE424M		—	2967, 2970	—	Mbps
F_{LBW}	Loop bandwidth for SMPTE 292M		—	2	—	MHz
F_{LBW}	Loop bandwidth for SMPTE 424M		—	4	—	MHz

Table 1-4. PCML Input/Output Electrical Characteristics (2 of 2)

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
$t_{LOCK, ASYNCH}$	Lock time, asynchronous		—	—	15	ms
$t_{LOCK, SYNCH}$	Lock time, synchronous		—	—	1	µs

NOTES:

1. Programmable with 200 mV increments.
2. Measured using a clock pattern with 50% duty cycle and consisting of 10 Consecutive Identical Digits (10 CID)
3. Programmable in 2 dB steps.
4. Measured according to SMPTE RP184 and SMPTE RP192.
5. Jitter cleaner is used for HD and 3G data rates only, bypassed and powered down for SD data rates.
6. Measured to BER 1E-09 using PRBS10 test pattern, using default output swing

Table 1-5. Control/Interface Logic Input/Output Characteristics

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
V_{OH}	Digital output logic high	1	0.85 x V_{CC}	V_{CC}	—	V
V_{OL}	Digital output logic low	2	—	0	0.15 x V_{CC}	V
V_{IH}	Digital input logic high		0.75 x V_{CC}	—	V_{CC}	V
V_{IL}	Digital input logic low		0	—	0.25 x V_{CC}	V
V_{IF}	Digital input logic float		0.35 x V_{CC}	—	0.65 x V_{CC}	V

NOTES:

1. I_{OH} = -4 mA.
2. I_{OL} = 4 mA.

2.0 Typical Performance Characteristics

Unless otherwise noted, typical performance applies for V_{CC} = 2.5 V, 25 °C ambient temperature, 800 mV_{PP} differential input data swing, PRBS 2^{10} – 1 data pattern at 2.97 Gbps.

Figure 2-1. Eye Diagram @2.97 Gbps, Unequalized Signal, After 200 m Belden 1694A Cable

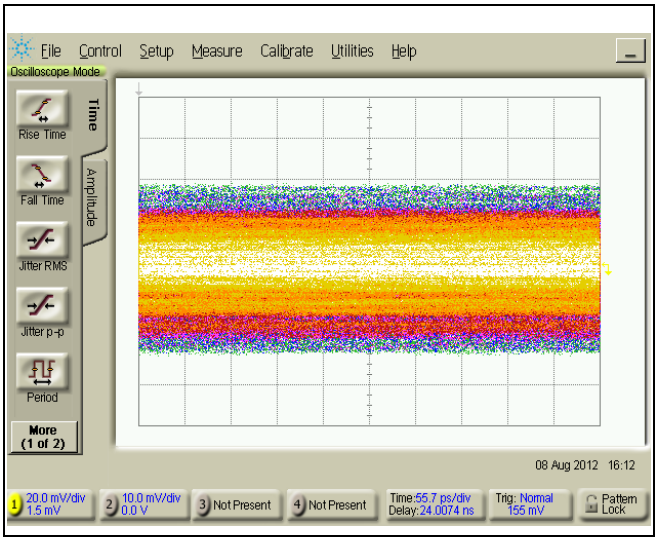
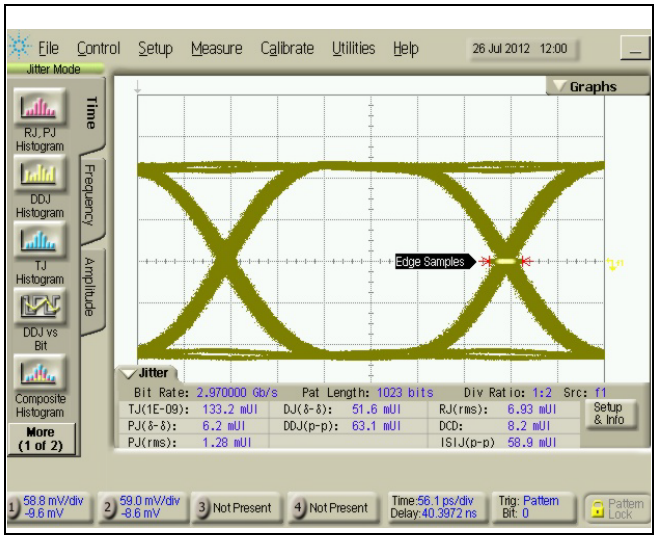


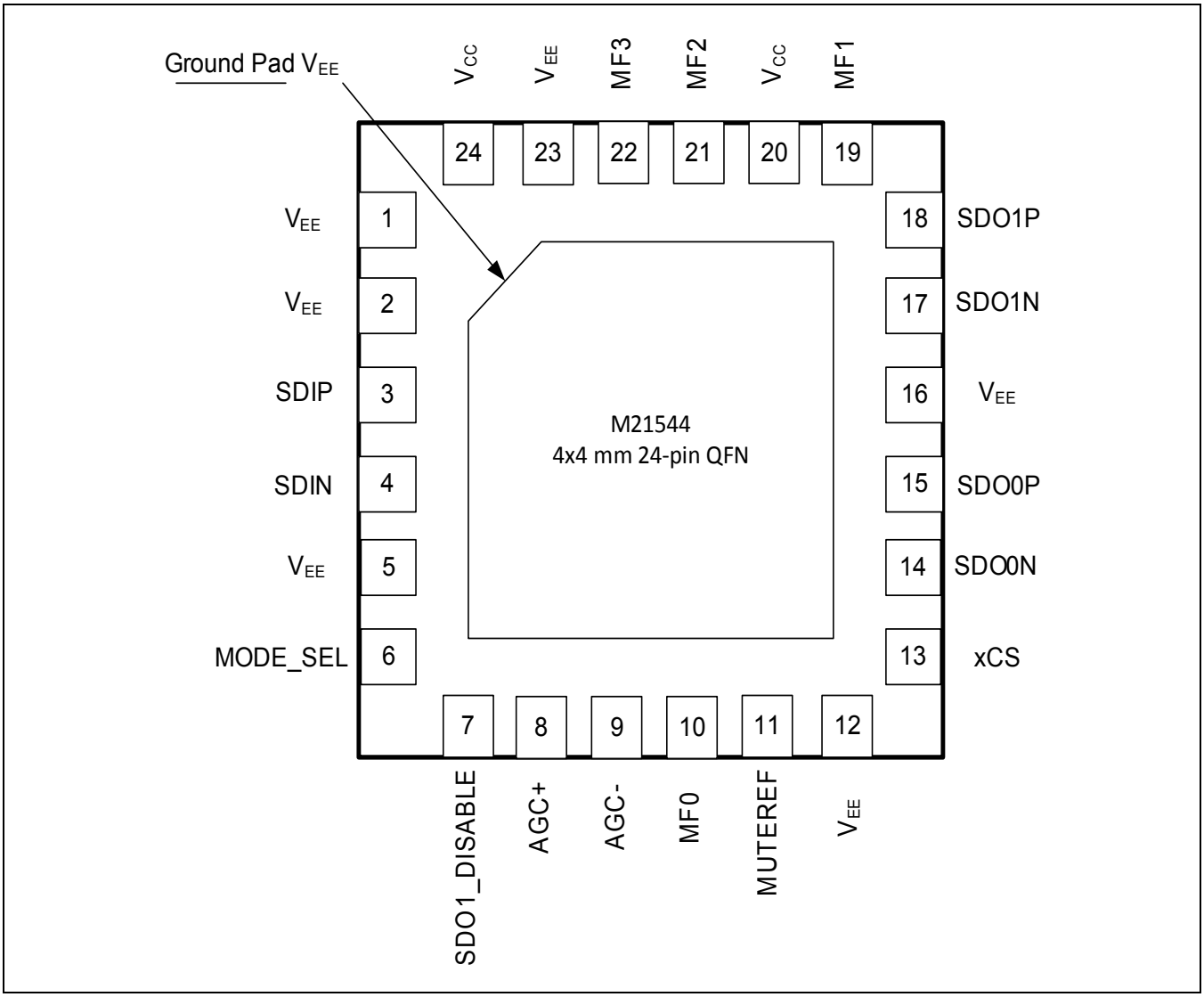
Figure 2-2. Eye Diagram @2.97 Gbps, Equalized Signal, After 200 m Belden 1694A Cable (Jitter Cleaner Enabled)



3.0 Pinout Diagram, Pin Descriptions, and Package Outline Drawing

3.1 M21544 Pinout

Figure 3-1. M21544 Pinout Diagram (Bottom View of the Package)



3.2 M21544 Pin Description

Table 3-1. M21544 Pin Descriptions (1 of 2)

Pin Name	Pin Number(s)	Type	Description
V_{EE}	1,2,5,12,16,23, Ground Pad	Ground	Negative power supply (ground)
V_{CC}	20,24	Power	Positive power supply (2.5 V)
SDIP/SDIN	3,4	I, SDI	Serial data input
SDO0P/SDO0N	15,14	O, LVDS	Serial data output 0
SDO1P/SDO1N	18,17	O, LVDS	Serial data output 1
MODE_SEL	6	I, LVCMOS	Mode Select 1: **Software Mode Enabled** (4-wire digital interface) 0: **Hardware Mode Enabled** Internal pull down
SDO1_DISABLE	7	I, LVCMOS	SDO1 disable pin 1: SDO1 disable 0: SDO1 enable Internal pull up. Hardware pin state overrides register setting configurations
AGC+/-	8,9	I/O, Analog	Equalizer loop filter capacitor (33 nF)
MF0	10	I, tri-state LVCMOS	**Hardware Mode** (MODE_SEL =0) BYPASS 1: Bypass entirely the equalizer and jitter cleaner Z: Bypass only the jitter cleaner 0: Normal operation **Software Mode** (MODE_SEL =1) xSD: Signal Detect Complement 1: No input signal is present or the cable length is above the MUTEREF threshold 0: Input signal is present and cable length is below the MUTEREF threshold
MUTEREF	11	I, Analog	Mute reference input. Defines the cable length threshold at which the signal detect will be asserted. By connecting xSD to MUTE, it controls the maximum cable length after which the part will mute. This pin can be left floating or can be grounded for maximum equalization.
xCS	13	I, LVCMOS	**Hardware Mode** (MODE_SEL =0) Must be set LOW for normal operation. **Software Mode** (MODE_SEL =1) Chip Select Complement, Internal pullup.
MF1	19	I, LVCMOS	**Hardware Mode** (MODE_SEL =0) Automatic sleep control. Sleep mode has precedence over MUTE and BYPASS. 1: Automatic power down when no input is present 0: Normal mode, the equalizer is always active **Software Mode** (MODE_SEL =1) 4-wire: Signal Out Internal pull up

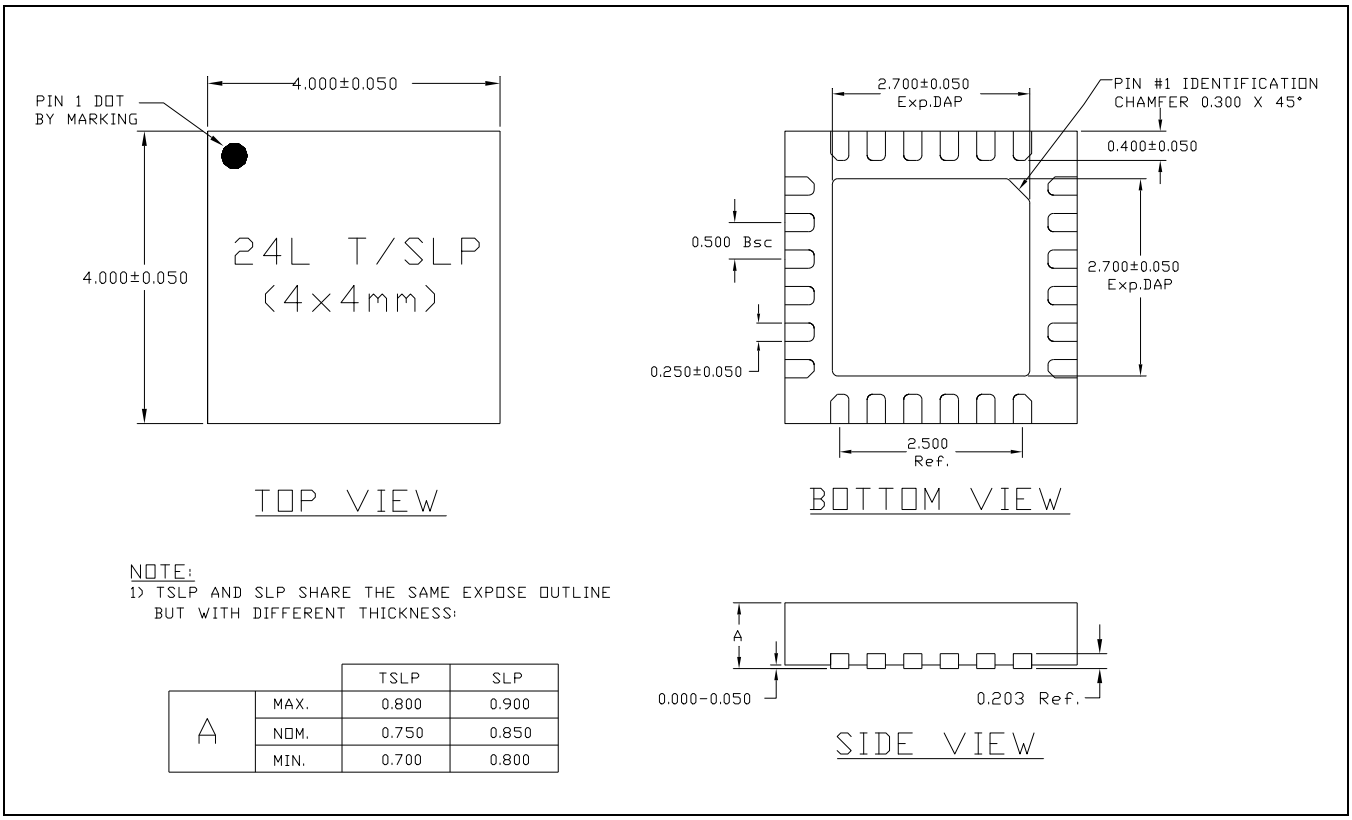
Table 3-1. M21544 Pin Descriptions (2 of 2)

Pin Name	Pin Number(s)	Type	Description
MF2	21	I, LVCMOS	**Hardware Mode** (MODE_SEL =0) Output mute. MUTE has precedence over BYPASS. 1: Outputs are muted 0: Normal operation **Software Mode** (MODE_SEL =1) 4-wire: SCLK Internal pull down
MF3	22	I, LVCMOS	**Hardware Mode** (MODE_SEL =0) xSD: Signal Detect 1: No input signal is present or the cable length is above the MUTEREF threshold 0: Input signal is present and cable length is below the MUTEREF threshold **Software Mode** (MODE_SEL =1) 4-wire: Signal In Internal pull down

3.3 M21544 Package Information

The M21544 is packaged in a 4 mm footprint, 24-pin QFN.

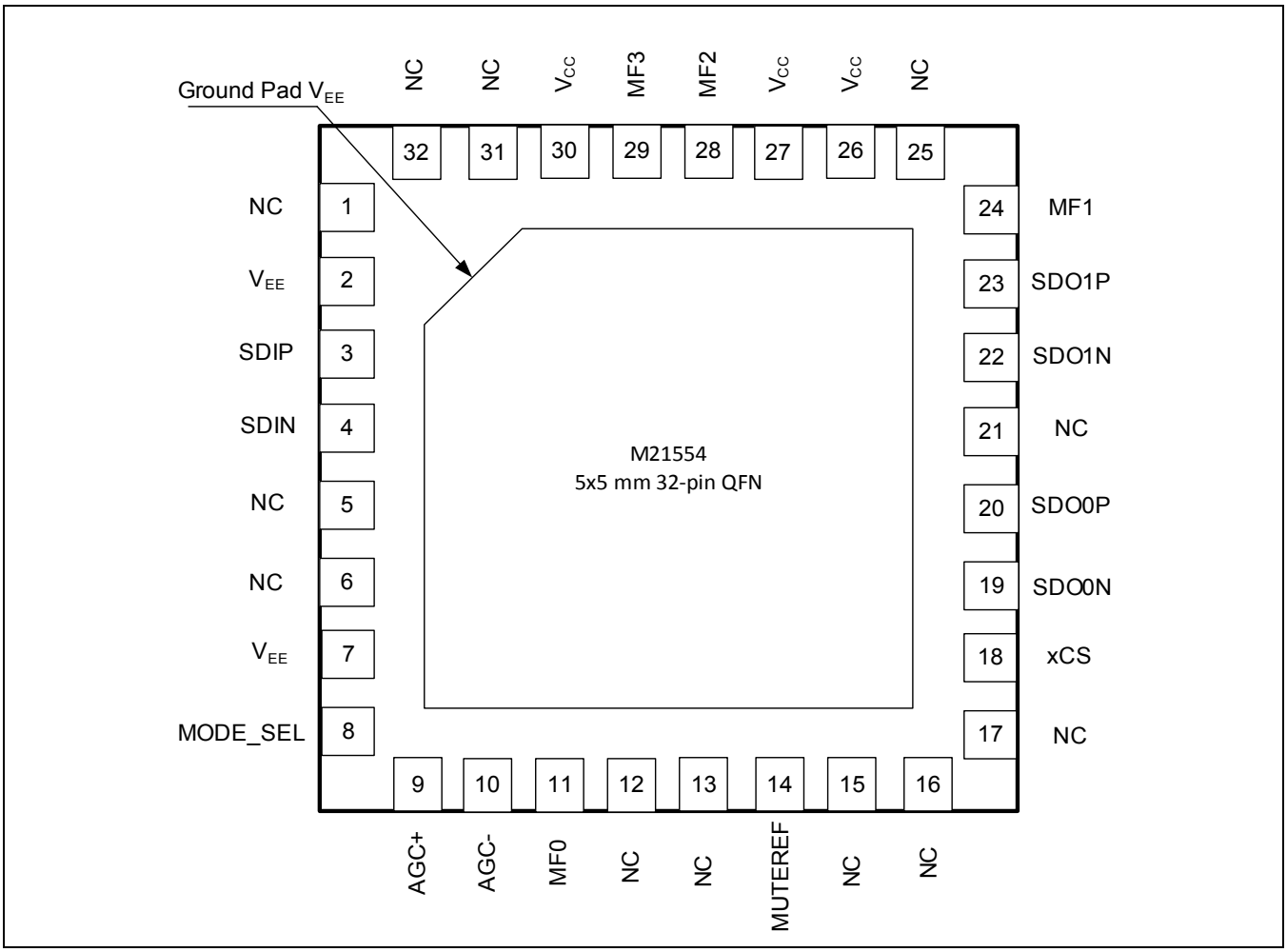
Figure 3-2. M21544 Packaging Drawing



		TSLP	SLP
A	MAX.	0.800	0.900
	NOM.	0.750	0.850
	MIN.	0.700	0.800

3.4 M21554 Pinout

Figure 3-3. M21554 Pinout Diagram (Bottom View of the Package)



3.5 M21554 Pin Description

Table 3-2. M21554 Pin Descriptions (1 of 2)

Pin Name	Pin Number(s)	Type	Description
V_{EE}	2,7, Ground Pad	Ground	Negative power supply (ground)
V_{CC}	26,27,30	Power	Positive power supply (2.5 V)
SDIP/SDIN	3,4	I, SDI	Serial data input
SDO0P/SDO0N	20,19	O, LVDS	Serial data output 0
SDO1P/SDO1N	23,22	O, LVDS	Serial data output 1
MODE_SEL	8	I, LVCMOS	Mode Select 1: **Software Mode Enabled** (4-wire digital interface) 0: **Hardware Mode Enabled** Internal pull down
AGC+/-	9,10	I/O, Analog	Equalizer loop filter capacitor (33 nF)
MF0	11	I, tri-state LVCMOS	**Hardware Mode** (MODE_SEL =0) BYPASS 1: Bypass entirely the equalizer and jitter cleaner Z: Bypass only the jitter cleaner 0: Normal operation **Software Mode** (MODE_SEL =1) xSD: Signal Detect Complement 1: No input signal is present or the cable length is above the MUTEREF threshold 0: Input signal is present and cable length is below the MUTEREF threshold
MUTEREF	14	I, Analog	Mute reference input. Defines the cable length threshold at which signal detect will be asserted. By connecting xSD to MUTE, it controls the maximum cable length after which the part will mute. This pin can be left floating or can be grounded for maximum equalization.
xCS	18	I, LVCMOS	**Hardware Mode** (MODE_SEL =0) Must be set LOW for normal operation. **Software Mode** (MODE_SEL =1) Chip Select Complement, Internal pullup.
MF1	24	I, LVCMOS	**Hardware Mode** (MODE_SEL =0) Automatic sleep control. Sleep mode has precedence over MUTE and BYPASS. 1: Automatic power down when no input is present 0: Normal mode, the equalizer is always active **Software Mode** (MODE_SEL =1) 4-wire: Signal Out Internal pull up

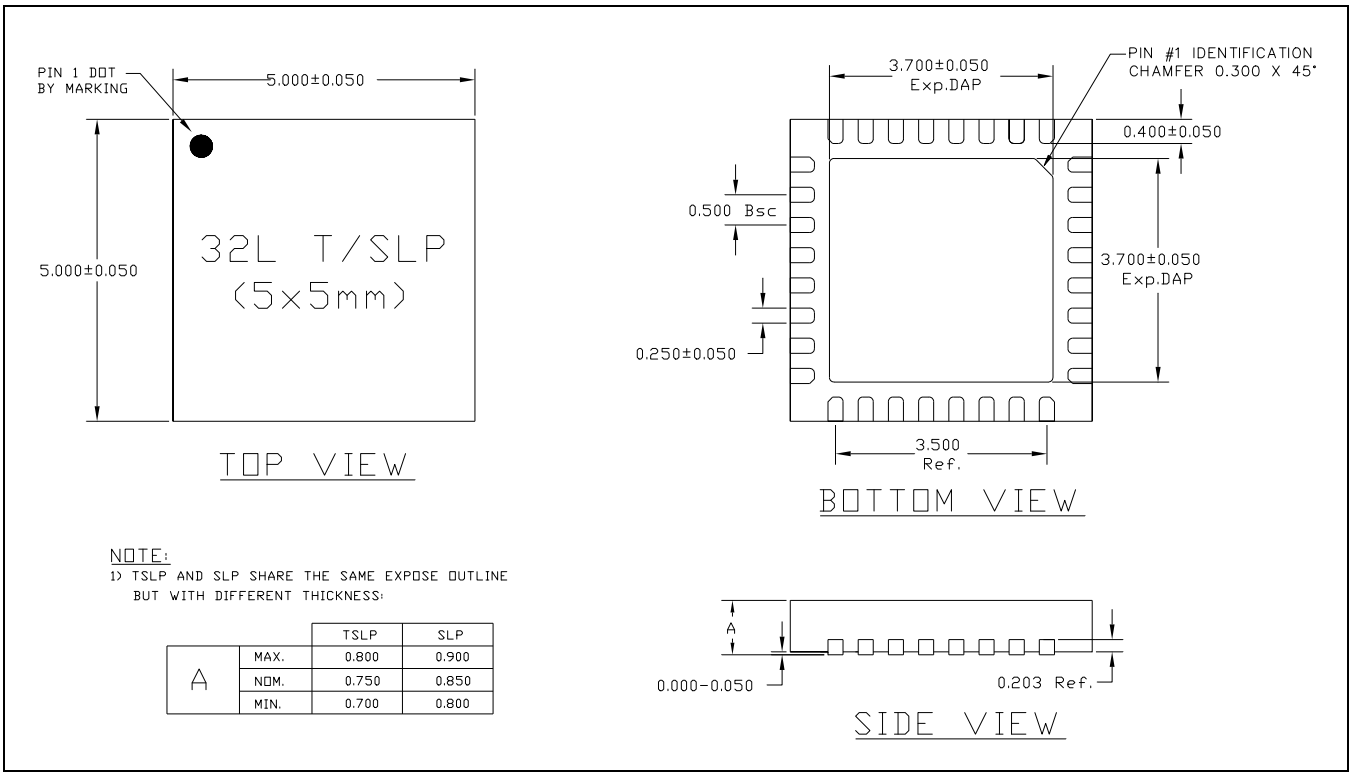
Table 3-2. M21554 Pin Descriptions (2 of 2)

Pin Name	Pin Number(s)	Type	Description
MF2	28	I, LVCMOS	**Hardware Mode** (MODE_SEL =0) Output mute. MUTE has precedence over BYPASS. 1: Outputs are muted 0: Normal operation **Software Mode** (MODE_SEL =1) 4-wire: SCLK Internal pull down
MF3	29	I, LVCMOS	**Hardware Mode** (MODE_SEL =0) xSD: Signal Detect 1: No input signal is present or the cable length is above the MUTEREF threshold 0: Input signal is present and cable length is below the MUTEREF threshold **Software Mode** (MODE_SEL =1) 4-wire: Signal In Internal pull down
NC	1,5,6,12,13, 15,16,17,21, 25,31,32		No Connect

3.6 M21554 Package Information

The M21554 is packaged in a 5 mm footprint, 32-pin QFN.

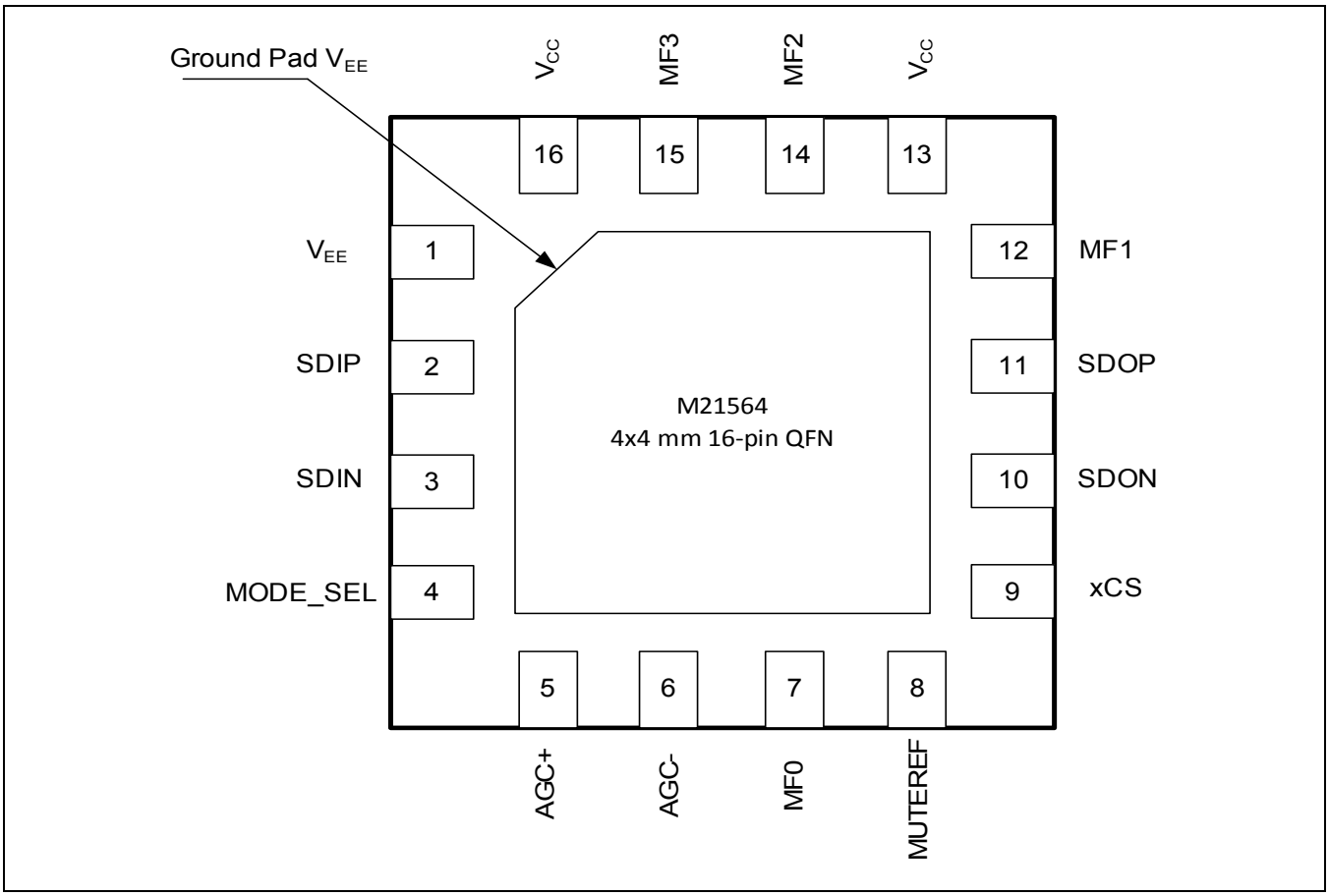
Figure 3-4. M21554 Packaging Drawing



		TSLP	SLP
A	MAX.	0.800	0.900
	NOM.	0.750	0.850
	MIN.	0.700	0.800

3.7 M21564 Pinout

Figure 3-5. M21564 Pinout Diagram (Bottom View of the Package)



3.8 M21564 Pin Description

Table 3-3. M21564 Pin Descriptions (1 of 2)

Pin Name	Pin Number(s)	Type	Description
V_{EE}	1, Ground Pad	Ground	Negative power supply (ground)
V_{CC}	13,16	Power	Positive power supply (2.5 V)
SDIP/SDIN	2,3	I, SDI	Serial data input
SDOP/SDON	11,10	O, LVDS	Serial data output 0
MODE_SEL	4	I, LVCMOS	Mode Select 1: **Software Mode Enabled** (4-wire digital interface) 0: **Hardware Mode Enabled** Internal pull down
AGC+/-	5,6	I/O, Analog	Equalizer loop filter capacitor (33 nF)
MF0	7	I, tri-state LVCMOS	**Hardware Mode** (MODE_SEL =0) BYPASS 1: Bypass entirely the equalizer and jitter cleaner Z: Bypass only the jitter cleaner 0: Normal operation **Software Mode** (MODE_SEL =1) Signal Detect 1: No input signal is present or the cable length is above the MUTEREF threshold 0: Input signal is present and cable length is below the MUTEREF threshold
MUTEREF	8	I, Analog	Mute reference input. Defines the cable length threshold at which the signal detect will be asserted. By connecting xSD to MUTE, it controls the maximum cable length after which the part will mute. This pin can be left floating or can be grounded for maximum equalization.
xCS	9	I, LVCMOS	**Hardware Mode** (MODE_SEL =0) Must be set LOW for normal operation. **Software Mode** (MODE_SEL =1) Chip Select Complement, Internal pullup.
MF1	12	I, LVCMOS	**Hardware Mode** (MODE_SEL =0) Automatic sleep control. Sleep mode has precedence over MUTE and BYPASS. 1: Automatic power down when no input is present 0: Normal mode, the equalizer is always active **Software Mode** (MODE_SEL =1) 4-wire: Signal Out Internal pull up

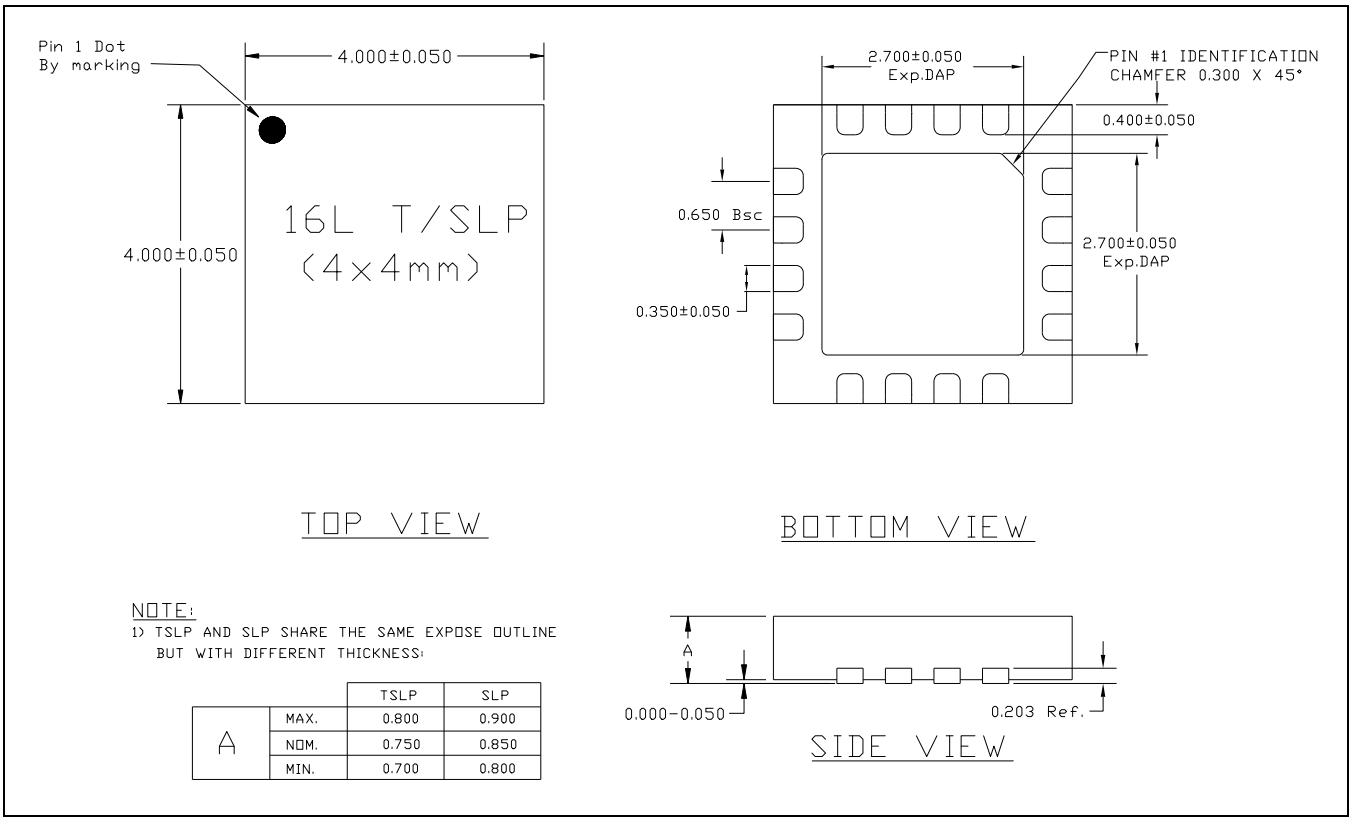
Table 3-3. M21564 Pin Descriptions (2 of 2)

Pin Name	Pin Number(s)	Type	Description
MF2	14	I, LVCMOS	**Hardware Mode** (MODE_SEL =0) Output mute. MUTE has precedence over BYPASS. 1: Outputs are muted 0: Normal operation **Software Mode** (MODE_SEL =1) 4-wire: SCLK Internal pull down
MF3	15	I, LVCMOS	**Hardware Mode** (MODE_SEL =0) xSD: Signal Detect 1: No input signal is present or the cable length is above the MUTEREF threshold 0: Input signal is present and cable length is below the MUTEREF threshold **Software Mode** (MODE_SEL =1) 4-wire: Signal In Internal pull down

3.9 M21564 Package Information

The M21564 is packaged in a 4 mm footprint, 16-pin QFN.

Figure 3-6. M21564 Packaging Drawing



		TSLP	SLP
A	MAX.	0.800	0.900
	NOM.	0.750	0.850
	MIN.	0.700	0.800

4.0 Functional Descriptions

The M21544/54/64 devices are part of the next generation cable equalizer family for SDI video applications. They allow the transmission of data over of 200 m Belden 1694A cable at 3 Gbps, 220 m at 1.5 Gbps and 400 m at 270 Mbps.

The equalizer has an integrated Automatic Rate Detect (ARD) circuitry that allows the jitter cleaner to be enabled for HD and 3G data rates and will be automatically bypassed and turned off for SD rates providing additional power consumption savings. The jitter cleaner can provide retimed one or two serial data outputs with very low alignment jitter. In addition, the jitter cleaner does not need the traditional 27 MHz crystal reference clock.

The M21544/54/64 support limited configuration through hardware pin settings (Hardware Mode) or for additional configuration settings, a digital interface is also available (Software Mode).

Figure 4-1. M21544/54 Block Diagram

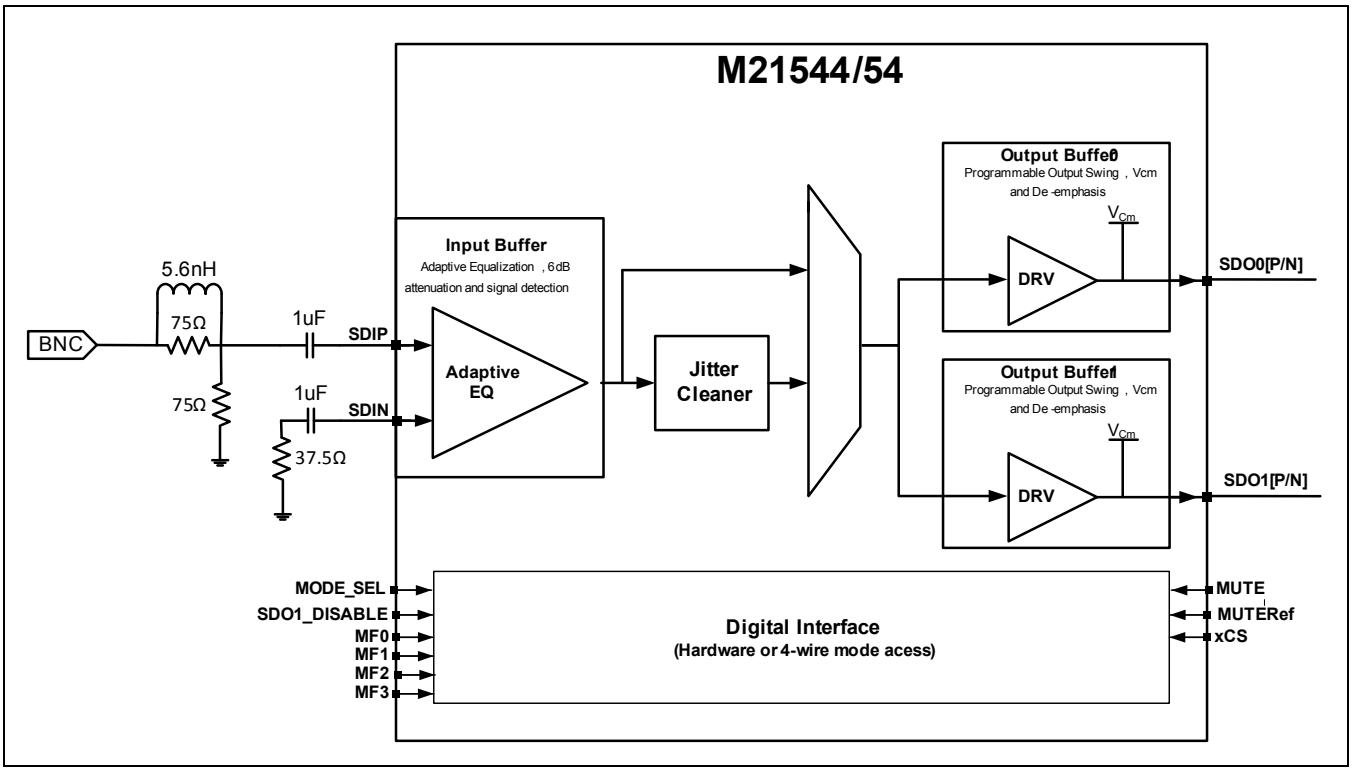
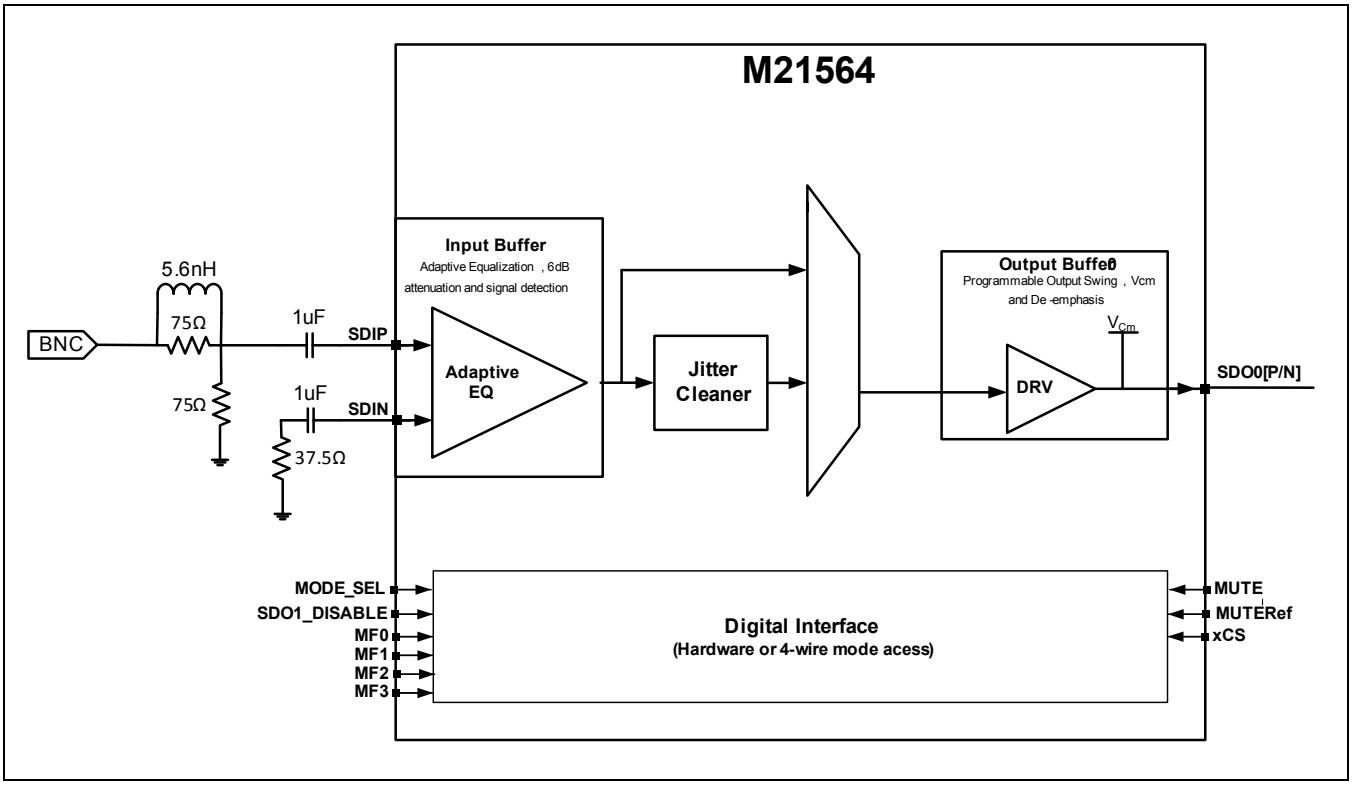


Figure 4-2. M21564 Block Diagram



4.1 High-Speed Input

Digital video coaxial cables are AC-coupled to the high-speed low-noise inputs (**SDIP/SDIN**). These are designed to operate in both single-ended or differential mode. The typical application is single-ended into the non-inverting **SDI** input with the inverting **SDI** input biased to match the bias on the input used.

The M21544/54/64 do not contain any internal input terminations and require both external input termination as well as the matching circuit to exceed the SMPTE input return loss specifications. The package and IC design have been optimized for high-speed performance, allowing them to exceed the SD/HD/3G SMPTE return loss.

For non-inverting single-ended operation, the recommended input circuit is shown in Figure 4-1. For differential operation, the matching/termination circuit on **SDIP** should be duplicated on **SDIN**.

4.1.1 Input Signal Detection

The high-speed input block offers a signal detect function that can be monitored either with pin.**MF3** or register.**GenConfig** bit[7]. The signal detect is also used to turn off the device if there is no signal present at the input. If desired, this function can be bypassed using register.**GenConfig** bit[4:3] or by setting pin.**MF1** = low in hardware mode.

4.1.2 Adaptive Equalizer

In typical hardware mode operation, the adaptive equalization is enabled with pin.**MF0** = Low (bypass disabled). However, with pin.**MF0**= High, the adaptive equalization and DC restore circuit are bypassed and the input is fed directly to the output buffers.

In software mode operation, the equalizer block can be bypassed by setting register.**GenConfig**.bit[5] to 1b.

The adaptive equalizer can be set to have a 6 dB gain for applications that have 400 mV_{PP} launch amplitude instead of 800 mV_{PP}. To have this 6 dB gain, register 00h bit[2] (**register.launch_ctrl**) must be set to 1b.

Once there is a signal detected at the input of the equalizer, the adaptive equalizer has the ability to report what length of Belden 1694A cable is being used. The cable length indicator results can be read on registers 05h bit[0] and register 06h bit[7:0]. The formulas to calculate the estimated cable length are:

CL(m) = 0.625*CLI, for 0-250 m

CL(m) = 2.5*(CLI - 400) + 250, for >250 m

where CLI is the decimal value of the 9 bits from registers 05h bit[0] (msb) and register 06h bit[7:0] (lsb) and CL is the estimated Belden 1694A cable length in meters. Table 4-1 has some of the decoded values for the cable length indicator registers.

Table 4-1. Cable Length Indicator Decoder

CLI Results	Estimated Cable Length*
000000000	0 m
000101000	25 m
001010000	50 m
001111000	75 m
010100000	100 m
011001000	125 m
011110000	150 m
100011000	175 m
101000000	200 m
101101000	225 m
110010000	250 m
110100100	300 m
110111000	350 m
111001100	400 m
111100000	450 m
* All cable length indicator values are approximate and are not guaranteed.	

4.1.3 6 dB Attenuation

The M21544/54/64 provide an option to compensate for 6 dB of flat attenuation in applications where the launch amplitude is a lot lower than 800 mV_{PPD}. When the expected launch amplitude is between ~300 mV_{PPD} and ~500 mV_{PPD}, setting register.**GenConfig**,bit[2] to 1b will improve the equalizer's performance specially for SD rates. For HD and 3G rates, having the jitter cleaner enabled will result in the best performance in addition to the 6 dB compensation.

4.2 Jitter Cleaner

The jitter cleaner on the M21544/54/64 is functional only for HD and 3G video data rates and will be automatically bypassed and turned off for SD rates providing additional power consumption savings.

The jitter cleaner features an Automatic Rate Detector (ARD) circuit that monitors the input signal rate and automatically sets the Jitter Cleaner to the correct video rate. The data rate determined by the ARD block may be read from register.**JitterCleaner**,bit[7:6].

Table 4-2. Jitter Cleaner Data Rate Detector

Register.JitterCleaner,bit[7:6]	Data Rate Detected
00b	SD
01b	HD
10b	3G
11b	HD or 3G (used when the Jitter cleaner is bypassed)

The jitter cleaner is always in auto-bypass mode. If the ARD cannot determine the rate of the input data stream, it will switch the Jitter Cleaner into bypass mode. This allows a data rate other than those specified to be passed through the Jitter Cleaner.

4.3 High-Speed Outputs

The high-speed LVDS differential outputs after equalization are made available on the pin.**SDO0[P/N]** and pin.**SDO1[P/N]** pins. Note that the M21564 has only one output available, pin.**SDO0[P/N]**.

There are three output swings available - 400 mV_{PP}, 600 mV_{PP} (default) and 800 mV_{PP}. The output swing levels can only be controlled via register.**OutputDriver**[1:0].bit[7:6].

In addition to controlling the output swing, the common mode voltage (V_{CM}), can also be modified to Auto mode for low common mode DC impedance, 0.8 V, 1.0 V or 1.2 V(default) by programming the desired value to register.**OutputDriver**[1:0].bit[5:4]. When the output driver is set to have automatic common mode voltage, it will sense the downstream device input common mode and it will match it. Note, the maximum common mode voltage is 1.2 V.

In order to improve signal integrity when used in large systems, each output also comes equipped with programmable de-emphasis (DE) for FR4 traces. There are four settings for output de-emphasis: 0 dB (or no DE), 2 dB, 4 dB, and 6 dB. In software mode, the output de-emphasis level for each input may be set by programming the desired value to register.**OutputDriver**[1:0].bit[3:1].

4.4 Control Modes

The M21544/54/64 may be configured in two separate control modes. The control mode is determined by the setting of the MODE_SEL pin as shown in Table 4-3 below.

Table 4-3. Control Mode Setting

MODE_SEL	Control Mode
MODE_SEL = L	Hardware Mode
MODE_SEL = H	Software Mode (4-wire digital interface)

4.4.1 Hardware Mode

Configuring the M21544/54/64 in hardware mode avoids the complication of adding a microcontroller, but offers limited control options. When in hardware mode, the MF (Multi Function IO) pins are configured as shown in Table 4-4 below.

Table 4-4. MF Pin Configuration in Hardware Mode (MODE_SEL = 0)

Pin Name	Hardware Mode Pin Name	Function
MF0	BYPASS	EQ and Jitter Cleaner bypass*
MF1	AUTOSLEEP	Power down EQ when no input signal is present
MF2	MUTE	Output mute
MF3	xSD	Signal Detect (Active Low)
* Please see pin descriptions for more details.		

4.4.2 Software Mode (4-wire Digital Interface Access)

In this mode, a four-wire serial interface is used to program the device's internal registers, configuring the operation of the M21544/54/64. When in software mode, MF[3:0] pins comprise the four-wire bus as well as additional diagnostics as shown in Table 4-5 below.

Table 4-5. MF Pin Configuration in Software mode (4-wire Interface Mode, MODE_SEL = 1)

Pin Name	4-Wire Mode Pin Name	Function
MF0	xSD	Signal Detect (Active Low)
MF1	SO	Serial Data Output
MF2	SCK	Serial Data Clock
MF3	SI	Serial Data Input
xCS	xCS	Chip Select (Active Low)

4.5 Digital Interface

The 4-wire serial interface is selected with pin.**MODE_SEL** =H.

The interface shifts data in from the external controller on the rising edge of the serial clock (**SCLK**). The serial I/O operation is gated by chip select (**xCS**). Data is shifted to the M21544/54/64 from the Host (Master) on the serial input (**SI**) on the falling edge of **SCLK**, and shifted out through the serial output (**SO**) on the rising edge of **SCLK**.

To address a register, a 10-bit input needs to be shifted using **SI**, consisting of the Start Bit (SB) = 1, the Operation bit (OP) = 1 for read, = 0 for write; and the 8-bit address (MSB first).

Figure 4-3. 4-wire Serial Digital Interface

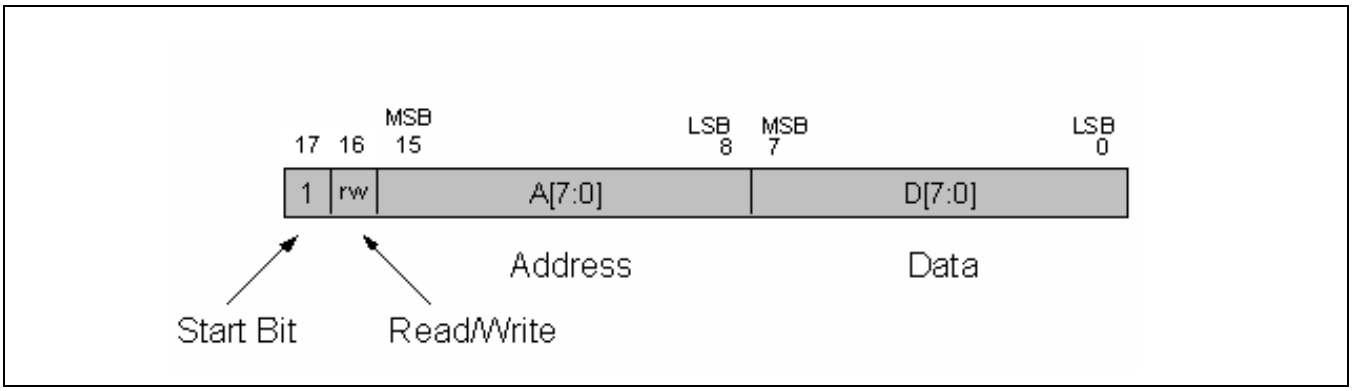


Figure 4-4 illustrates the Serial Write Mode. To initiate a Write sequence, **xCS** goes low before the falling edge of **SCLK.** On each falling edge of the clock, the 18 bits consisting of the Start Bit = 1, OP = 0 for write, ADDR (8-bit), and DATA (8-bit), are latched into the input shift register through "**SI.**" The rising edge of **xCS** must occur before the falling edge of **SCLK** for the last bit. Upon receipt of the last bit, one additional cycle of **SCLK** is necessary before DATA transfers from the input shift register to the addressed register.

Figure 4-6 illustrates the Serial Read mode to initiate a read sequence. **xCS** goes low before the falling edge of **SCLK.** On each falling edge of **SCLK**, the 10 bits consisting of Start Bit = 1, OP = 1 for read, and the 8-bit ADDR are written to the serial input shift register and copied to the serial output shift register. On the next rising edge after the address LSB, the SB and 8 bits of the DATA are shifted out.

The 4-wire serial interface supports multiple consecutive writes and reads, see Figure 4-5and Figure 4-7 respectively. In these cases, the address header is not needed and each additional 8 bits of data will be written into consecutive addresses. If consecutive read/write cycles are being performed, it is not necessary to insert an extra clock cycle between read/write cycles, however one extra clock cycle is needed after the last data bit of the last read/write cycle.

Notes: On a Write cycle, any bits that follow the expected number of bits will be ignored. On a Read cycle, any extra clock cycles will result in the repeat of the data LSB. An invalid SB or OP renders the operation undefined. The falling edge of "**xCS**" always resets the serial operation for a new Read or Write cycle.

Figure 4-4. 4-wire Random WRITE Timing Diagram

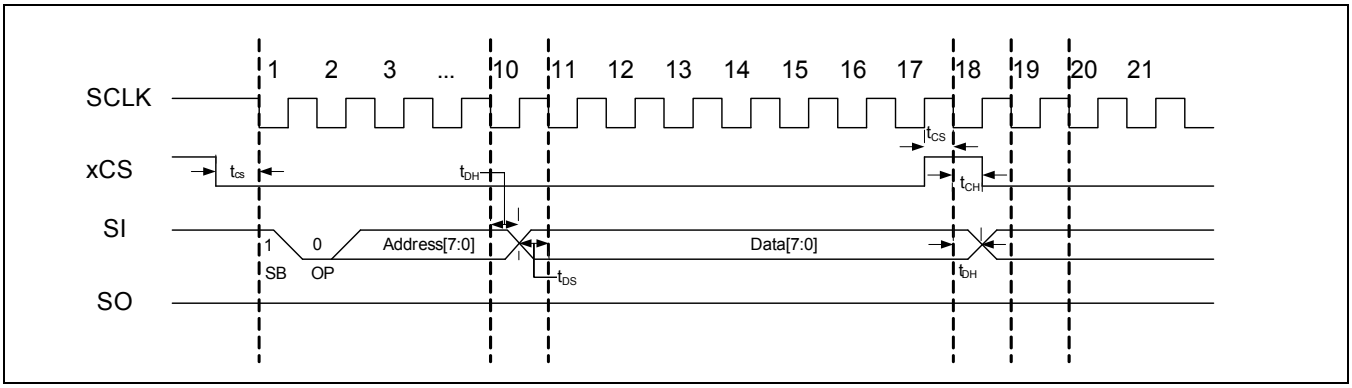


Figure 4-5. 4-wire Sequential WRITE Timing Diagram

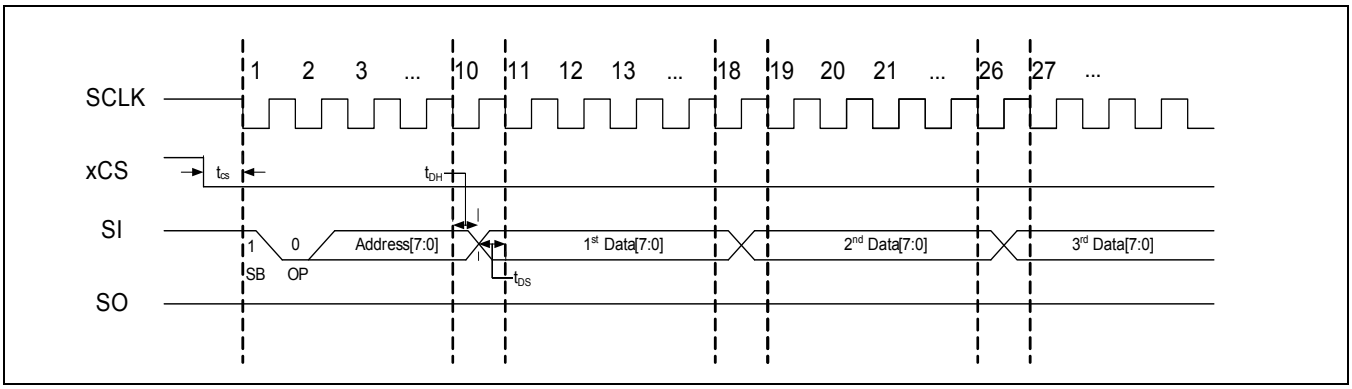


Figure 4-6. 4-wire Random READ Timing Diagram

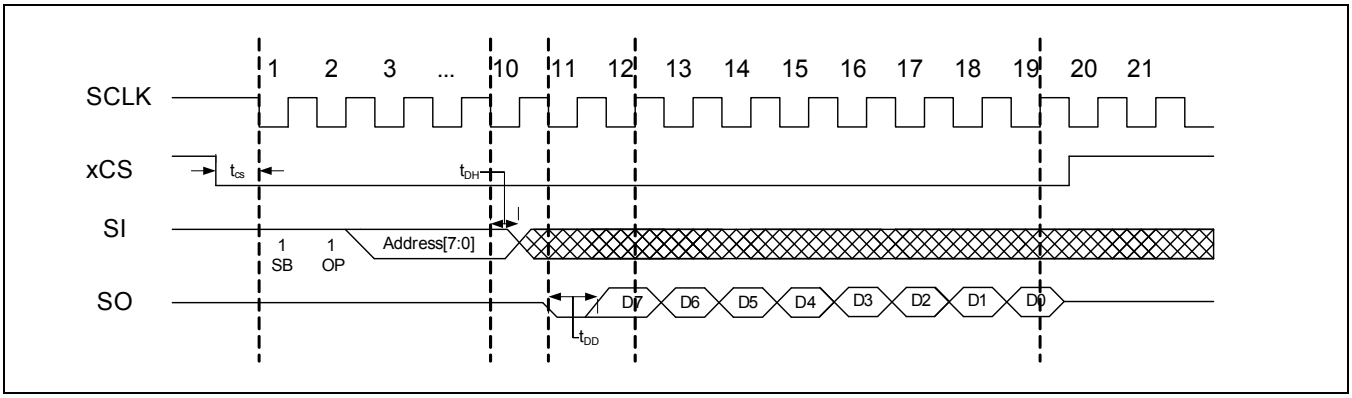


Figure 4-7. 4-wire Sequential READ Timing Diagram

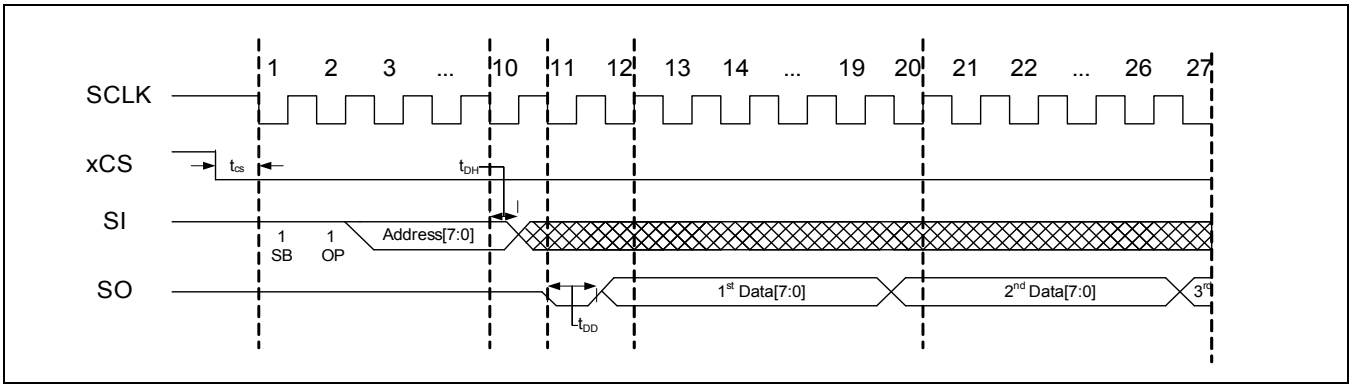


Table 4-6. 4-wire Serial Interface Specifications

Timing Symbol	Description	Min	Typ	Max	Unit
Tds	Data set-up time	2	—	—	ns
Tdh	Data hold time	2.5	—	—	ns
Tcs	xCS set-up time	2	—	—	ns
Tch	xCS hold time	2.5	—	—	ns
Tdd	Read data output delay (for max load capacitor 30 pF and DV_{DDO}@3.3 V)	2	—	16	ns
T_{FREQW}	Write 4-Wire clock Frequency	—	—	100	MHz
T_{FREQR}	Read 4-Wire clock Frequency	—	—	25	MHz
T_{DCD}	SCLK pulse width	45	—	55	%

5.0 Control Register Descriptions

Table 5-1. Register Summary

Address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
00h	GenConfig	signal_detect	mute	bypass	sleep mode		lanch_ctrl	master_rst	acq_rst	08'h	R/W
01h	OutputDriver0	output_swing0		offset_voltage0		de_emphasis0			Reserved	B0'h	R/W
02h	OutputDriver1	output_swing1		offset_voltage1		de_emphasis1			Reserved	B0'h	R/W
03h	Misc	muteref_mode	digital_muteref					Reserved	jc_bypass	7C'h	R/W
04h	JitterCleaner	rate_indicator		Reserved		die_rev				80'h	R
05h	CableLengthIndicator1	Reserved							cable_lenght_ind_bit8	na	R
06h	CableLengthIndicator0	cable_length_ind_bit7								na	R

5.1 Address Register Description

Address: 00h
Register Name: GenConfig
Default Value: 08'h
Description: General Configuration Register

Bit(s)	Name	Description	Default	Type
7	signal_detect	0b: No Signal detected 1b: Signal detected		R
6	mute	0b: Normal operation 1b: Equalizer muted	0b	R/W
5	bypass	0b: Normal operation 1b: Equalizer bypassed	0b	R/W
[4:3]	sleep_mode	00b: Forced enable of the equalizer 01b: Power down when no input signal detected 10b: Forced power down of the equalizer 11b: Reserved	01b	R/W

Bit(s)	Name	Description	Default	Type
2	launch_ctrl	0b: Equalizer expects 800 mV launch 1b: Equalizer expects 400 mV (6 dB attenuation)	0b	R/W
1	master_rst	0b: No reset 1b: Reset of registers and state machine (self clearing)	0b	R/W
0	acq_rst	0b: No reset 1b: Reset state machine only (self clearing)	0b	R/W

Address: 01h
Register Name: OutputDriver0
Default Value: B0'h
Description: Output Driver 0 Configuration Register

Bit(s)	Name	Description	Default	Type
[7:6]	output_swing	00b: Power down of driver 0 01b: 400 mV differential peak to peak swing 10b: 600 mV differential peak to peak swing 11b: 800 mV differential peak to peak swing	10b	R/W
[5:4]	offset_voltage	00b: Auto mode to drive a receiver presenting a low common mode DC impedance 01b: 0.8 V output common mode 10b: 1 V output common mode 11b: 1.2 V output common mode	11b	R/W
[3:1]	de_emphasis	000b: De-emphasis disable 001b: 2 dB de-emphasis 011b: 4 dB de-emphasis 101b: 6 dB de-emphasis 111b: 8 dB de-emphasis	000b	R/W
0	RSVD	Reserved (set to default)	0b	R/W

Address: 02h
Register Name: OutputDriver1
Default Value: B0'h
Description: Output Driver1 Configuration Register

Bit(s)	Name	Description	Default	Type
[7:6]	output_swing	00b: Power down of driver 1 01b: 400 mV differential peak to peak swing 10b: 600 mV differential peak to peak swing 11b: 800 mV differential peak to peak swing	10b	R/W
[5:4]	offset_voltage	00b: Auto mode to drive a receiver presenting a low common mode DC impedance 01b: 0.8 V output common mode 10b: 1 V output common mode 11b: 1.2 V output common mode	11b	R/W
[3:1]	de_emphasis	000b: De-emphasis disable 001b: 2 dB de-emphasis 011b: 4 dB de-emphasis 101b: 6 dB de-emphasis 111b: 8 dB de-emphasis	000b	R/W
0	RSVD	Reserved (set to default)	0b	R/W

Address: 03h
Register Name: Misc
Default Value: 7C'h
Description: MuteRef Configuration and Jitter Cleaner Bypass Register

Bit(s)	Name	Description	Default	Type
7	muteref_mode	0b: Analog MuteRef with external pin voltage 1b: Digital MuteRef	0b	R/W
[6:2]	digital_muteref	0 0000b: Mute when cable > 10 m 0 0010b: Mute when cable > 25 m … 0 1010b: Mute when cable > 100 m 0 1100b: Mute when cable > 125 m 0 1111b: Mute when cable > 150 m 1 0001b: Mute when cable > 175 m 1 0100b: Mute when cable > 200 m … 1 1001b: Mute when cable > 250 m 1 1010b: Mute when cable > 300 m 1 1011b: Mute when cable > 350 m 1 1100b: Mute when cable > 400 m 1 1110b: Mute when cable > 450 m 1 1111b: Never mute	1 1111b	R/W
1	RSVD	Reserved (set to default)	0b	R/W
0	jc_bypass	0b: Jitter cleaner active 1b: Jitter cleaner bypassed	0b	R/W

Address: 04h
Register Name: JitterCleaner
Default Value: 00'h
Description: Jitter Cleaner Configuration and Status Register

Bit(s)	Name	Description	Default	Type
[7:6]	rate_indicator	00b: SD rate 01b: 1.5 Gbps 10b: 3 Gbps 11b: HD rates (1.5 Gbps or 3 Gbps)	00b	R
[5:4]	RSVD	Reserved	00b	R/W
[3:0]	die_rev	0000b: Die revision	0001b	R

Address: 05h
Register Name: CableLengthIndicator1
Default Value: na
Description: Adaptation Results of Equalizer

Bit(s)	Name	Description	Default	Type
[7:1]	RSVD	Reserved (set to default)	0b	R
0	cable_lenght_ind_bit8	Cable_length_ind[8]. Bit 8 of the cable length indication	NA	R

Address: 06h
Register Name: CableLengthIndicator0
Default Value: na
Description: Adaptation Results of Equalizer

Bit(s)	Name	Description	Default	Type
[7:0]	cable_lenght_ind_bit[7:0]	Cable_length[7:0]. Bits [7:0] of the cable length indication	NA	R

NOTES:

1. A numerical value of 0 corresponds to the shortest cable. The maximum value allowed for the cable length indicator is 101111011.

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