M21215 (HD/SD-SDI) Auto-rate Reclocker w/4:1 Selector

The M21215 is a high-speed, low-power reclocker designed to remove both random and inter-symbol interference (ISI) jitter from the input data for SMPTE and DVB-ASI serial digital video applications. Mindspeed's high-performance reclocker offers significant power reduction compared to legacy reclocking solutions.

The M21215 is based on a custom and proprietary reclocker core. The high-performance reclocker design results in high-jitter tolerance, especially in the presence of duty-cycle-distortion (DCD) that typically arises with AC coupling and video pathological test patterns. The M21215 also offers improved auto rate detect acquisition times over legacy reclocker solutions.

The M21215 supports SMPTE HD/SD-SDI data rates from 143 Mbps to 1485 Mbps. The M21215 is functionally and pin-for-pin compatible to the GS1535 for a true drop-in replacement but also provides a number of added benefits for new designs such as 2.5V operation, reduced output swing, additional loop bandwidth control, Auto Rate Detect optimization, and output common mode shifting for DC coupling to downstream LVPECL receivers.

Applications

- Serial Routing Switchers
- Distribution Amplifiers
- SMPTE Coaxial Cable Interface
- Studio video applications
- Broadcast video applications
- Distribution video applications

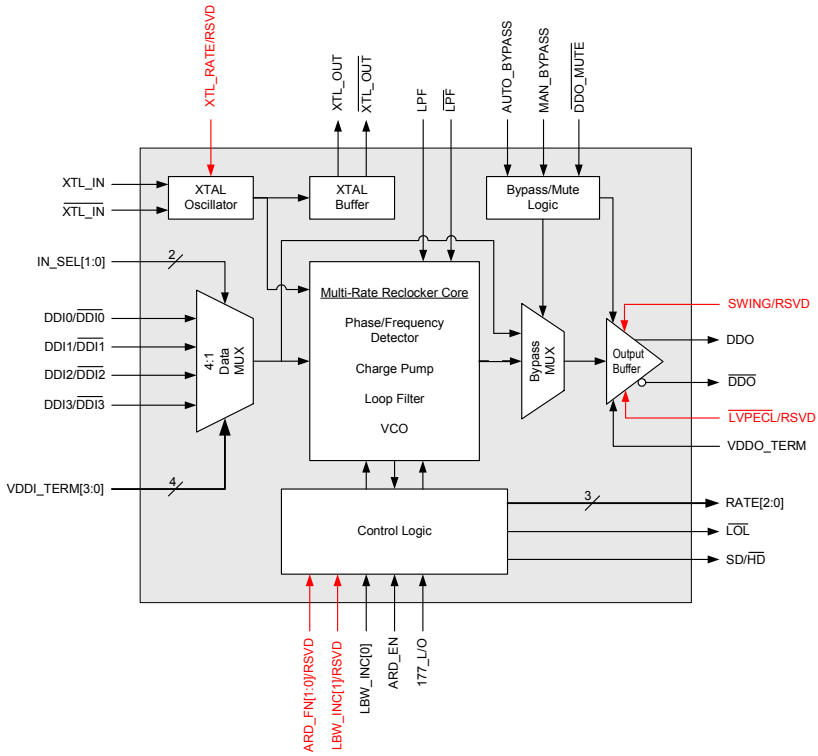
Standards Compliance

- SMPTE 259M, 292M, 344M and DVB-ASI

Features

- SD/HD operation: 143, 177, 270, 360, 540, 1483.5, 1485 Mbps and DVB-ASI at 270 Mbps
- Auto and manual rate selection modes with rate indication in Auto
- 4:1 Input MUX and Loss of Lock (LOL) indicator
- Input buffers are compatible with PCML, LVDS, or LVPECL voltage levels
- Differential I/O with on chip termination resistors
- Selectable auto MUTE or BYPASS with manual BYPASS option
- Pin to pin compatible with GS1535
- Low typical power dissipation (325 mW @ 2.5V, 430 mW @ 3.3V)
- 2.5V, or 3.3V power supply operation with GS1535 compatible operation at 3.3V
- Extended temperature operation: -10°C to +85°C

Functional Block Diagram



Note: Signal names in red indicate additional functions mapped to pins that are RSVD on the GS1535.

Ordering Information

Part Number	Package	Operating Data Rate	Operating Temperature
M21215G-16*	64-pin, 10 mm x 10 mm LQFP, RoHS compliant	143 - 1485 Mbps	–10 °C to 85 °C
* The letter “G” designator after the part number indicates that the device is RoHS-compliant. Refer to www.mindspeed.com for additional information.			

Revision History

Revision	Level	Date	Description
F	Released	June 2006	Updated ordering part number. Updated maximum current consumption. Revised jitter tolerance specification.
E	Advance	August 2005	Updated ordering part number. Updated output specification tables. Added application circuits for reference crystals.
D	Advance	February 2005	Separated HD/SD M21215 and SD only M21205 information into discrete datasheets. 1.8V operation removed.
C	Advance	January 2005	Added specifications for M21205.
B	Advance	July 2004	Revision B Release. - Power dissipation updated after initial characterization. - Added pin numbers to pin description Tables 1-2, 1-3, 1-4. - Jitter performance specifications update based on initial characterization results. - Updated ESD values.
A	Advance	April 2004	Initial Release

Table of Contents

Ordering Information ii
Revision History ii
Table of Contents iii
List of Figures iv
List of Tables v
1.0 Functional Description 1
1.1 General Description 1
1.1.1 Reclocker General Overview 1
1.1.2 Frequency Acquisition 1
1.2 Pin Descriptions 1
1.2.1 General Nomenclature 1
1.2.2 Pin Descriptions 2
1.2.2.1 Power/Reset 6
1.2.2.2 Input Selection Multiplexer 7
1.2.2.3 High-Speed I/O Pins 7
1.2.2.4 Reclocker Reference Frequency 8
1.2.2.5 Reclocker Loop Bandwidth 9
1.2.2.6 Loss of Lock Alarm 10
1.2.2.7 Auto Rate Detect (ARD) 10
1.2.2.8 Bypass and DDO_MUTE 11
2.0 Product Specification 12
2.1 General Specifications 12
2.2 Input/Output Level Specifications: 13
2.3 Reclocker Performance Specifications 15
2.4 Package Specification 17
3.0 Appendices 18
3.1 Glossary of Terms/Acronyms 18
3.2 Reference Documents 18
3.2.1 External 18

List of Figures

Figure 1-1. M21215 Pin Out 6
Figure 1-2. Input Circuit for GS1535 Drop-in 7
Figure 1-3. Input circuit for DC/AC coupled General Case 7
Figure 1-4. Application circuit when a series or parallel resonant crystal is used 8
Figure 2-1. Output Symbols Definition 16
Figure 2-2. Package Drawing 17

List of Tables

Table 1-1. Control/Interface/Low-Speed Pins 2
Table 1-2. Power Pins 4
Table 1-3. High-speed Signal Pins 5
Table 1-4. Reference Clock/Oscillator Input Specifications 9
Table 1-5. Loop Bandwidth Control Settings 9
Table 1-6. Rate Report Mapping when ARD is Enabled 10
Table 1-7. Rate Select with ARD Disabled 10
Table 1-8. ARD Search Pattern Selections 11
Table 1-9. Manual and Auto Bypass Settings 11
Table 2-1. Absolute Maximum Ratings 12
Table 2-2. Recommended Operating Conditions 12
Table 2-3. DC Power Electrical Specifications 13
Table 2-4. CMOS I/O Electrical Specifications 13
Table 2-5. High-Speed Input Electrical Specifications 14
Table 2-6. High-speed Output Electrical Specifications 14
Table 2-7. Reclocker Output Jitter Performance 15
Table 2-8. Reclocker High-speed Performance 15
Table 3-1. Glossary and Acronyms 18

1.0 Functional Description

1.1 General Description

1.1.1 Reclocker General Overview

The M21215 reclocker is a dual-loop based design. The primary phase-locked loop (PLL) functions to 1) lock the VCO to the incoming data rate and 2) to retime the incoming data to remove jitter. In general, the VCO tuning range for a multi-rate design is much larger than the frequency pull-in range of the reclocker phase detector. As a result, a secondary frequency-locked loop (FLL) is added to tune the VCO to the approximate data frequency so the clock and data recovery unit (CDR) can lock onto valid data. The FLL uses an external crystal as an absolute frequency reference. As a result, the external reference is only used to assist the CDR frequency locking and the jitter performance of the reference has no effect on the recovered data output jitter.

1.1.2 Frequency Acquisition

When the reclocker is out of lock ($\overline{LOL}$ = Low), the FLL is enabled. The FLL compares the input data to the external reference and drives the VCO towards a target frequency that is very close to the incoming data rate frequency. The FLL is shut off when the VCO frequency and the frequency of the input data are within +/- 2000 ppm of each other. When FLL is shut off, $\overline{LOL}$ = High, to indicate a lock condition. If data is present, then the phase lock loop of the reclocker will lock to the incoming data. When in lock, the FLL control circuit continues to monitor the frequency difference between the VCO and the reference. If the difference exceeds +/- 3000 ppm, a loss of lock condition is indicated and frequency acquisition is initiated. If there is no input data present, an internal loss of signal detector will keep $\overline{LOL}$=Low until an input signal has been detected. The output signal from the reclocker is undefined when there is no valid signal at the input of the reclocker. When a valid input signal is detected, frequency acquisition is initiated and the reclocker will lock to the appropriate data rate.

1.2 Pin Descriptions

1.2.1 General Nomenclature

Throughout this data sheet, physical pins will be denoted in **bold** print. An array of pins can be called by each individual pin name (e.g. **MF0**, **MF1**, **MF2**, **MF3**, and **MF6**) or as an array (e.g. **MF[0..3,6]** or **MF[0:3,6]**). The GS1535 has several reserved pins (RSVD) that are expected to be left floating in typical applications. These pins, when tied to either a logic High or logic Low are used to select additional features and options available only on the M21215.

1.2.2 Pin Descriptions

Table 1-1. Control/Interface/Low-Speed Pins (1 of 3)

Pin Name	Pin #	Function	Default	Type
XTL_IN/$\overline{\text{XTL\_IN}}$	52,53	Reference clock or crystal input. Defaults to 14.140 MHz for GS1535 compatible operation at 3.3V. 12.00MHz parallel resonance or 14.140MHz series resonance crystals supported.	Internal pull up	I-Analog
XTL_OUT/$\overline{\text{XTL\_OUT}}$	50,51	Reference frequency output for chained reclocker applications	-	O-Analog
XTL_RATE/RSVD	56	Selects the crystal ref frequency Low: 12.000 MHz parallel crystal input High: 14.140 MHz serial crystal input (floating default)	Internal pull up	I-CMOS
IN_SEL[1:0]	18,17	Input control signal that selects the active high-speed serial input 00b: Select **DDI0/$\overline{\text{DDI0}}$** 01b: Select **DDI1/$\overline{\text{DDI1}}$** 10b: Select **DDI2/$\overline{\text{DDI2}}$** 11b: Select **DDI3/$\overline{\text{DDI3}}$**	Internal pull down	I-CMOS
ARD_EN	21	Input control signal that enables Auto Rate Detect (ARD) functionality or manual rate setting mode. ARD_EN = High: Auto Rate Detector (ARD) enabled, ARD_EN = Low: Manual rate selection mode	Internal pull up	I-CMOS
ARD_FN[1:0]/RSVD	58,59	Input control signal used to select different ARD search orders to speed up acquisition times. This is an added function mapped to two RSVD pins on the GS1535. For existing designs, this function defaults to GS1535 compatible operation Sets the ARD search order and bit rates as follows: ARD_FN[High: High] Search order: 143→177→270→360→540→1483.5/1485→Repeat (floating default for GS1535 compatible operation) ARD_FN[High: Low] Search order: 270→360→540→1483.5/1485→Repeat ARD_FN[Low: High] Search order: 270→360→1485/1483.5→Repeat ARD_FN[Low: Low] Search order: 270→1485/1483.5-→Repeat	Internal pull up	I-CMOS

Table 1-1. Control/Interface/Low-Speed Pins (2 of 3)

Pin Name	Pin #	Function	Default	Type
RATE[2:0]	26,25,24	Bidirectional control signals used to indicate the data rate in ARD enabled mode or to force a data rate setting in Manual mode ARD_EN = High: RATE[2:0] pins indicate the date rate the M21215 is locked to according to pin decoding shown below ARD_EN = Low: RATE[2:0] pins are used to force a particular data rate according to the pin decoding shown below. RATE[2:0] = 000: 143 Mbps data rate RATE[2:0] = 001: 177 Mbps data rate RATE[2:0] = 010: 270 Mbps data rate RATE[2:0] = 011: 360 Mbps data rate RATE[2:0] = 100: 540 Mbps data rate RATE[2:0] = 101: 1483.5/1485 Mbps data rate	Internal pull down	I/O-CMOS
177_L/O	27	Input control signal used to lock out the 177Mbps data rate from the ARD search order sequences. This signal is mainly for drop-in compatibility with the GS1535 as the M21215 locks correctly with DVB-ASI data. 177_L/O = High: 177 Mbps data rate locked out from ARD search order 177_L/O = Low: 177 Mbps data rate included in ARD search order	Internal pull up	I-CMOS
LOL	28	Output Status indication signal for reclocker Loss of Lock. See the Frequency Acquisition section for more detailed information. $\overline{\text{LOL}}$ = High: Reclocker PLL is locked $\overline{\text{LOL}}$ = Low: Reclocker PLL is not locked	-	O-CMOS
SD/$\overline{\text{HD}}$	33	Output status indication signal to control slew rate of downstream cable driver. SD/$\overline{\text{HD}}$ = High: Reclocker locked to a SD data rate (143-540 Mbps) SD/$\overline{\text{HD}}$ = Low: Reclocker locked to a HD rate (1.4835/1.485 Gbps)	-	O-CMOS
AUTO_BYPASS	20	Input control signal that automatically bypasses the data directly from the input to the output if the Reclocker PLL can NOT lock to the incoming data stream. AUTO_BYPASS = High: Auto bypass reclocker if lock is not achieved AUTO_BYPASS = Low: Reclocker continues to attempt data lock but output data BER may be high.	Internal pull up	I-CMOS
MAN_BYPASS	19	Input control signal used to force a reclocker PLL bypass regardless of the setting of the AUTO_BYPASS signal. MAN_BYPASS = High: Force bypass (regardless of Autobypass state) MAN_BYPASS = Low: Enables normal AUTO_BYPASS operation	Internal pull down	I- CMOS
DDO_MUTE	36	Input control signal that forces the DDO/$\overline{\text{DDO}}$ outputs to logic low states. $\overline{\text{DDO-MUTE}}$ = High: Normal output operation $\overline{\text{DDO-MUTE}}$ = Low: Forces output to a logic low state	Internal pull up	I-CMOS

Table 1-1. Control/Interface/Low-Speed Pins (3 of 3)

Pin Name	Pin #	Function	Default	Type
LPF/$\overline{\text{LPF}}$	62/63	Loop Filter inputs on GS1535 that are left FLOATING on M21215. Loop filter is internal. Leave pins floating.	-	Analog
LBW_INC[1:0]	38,34	Input control signal used to increase the loop bandwidth (LBB) of the M21215. LBW_INC[0] pin 34 can be used alone to increase the LBW of the M21215 as a GS1535 compatible function. LBW_INC[1:0] = 00: 5.0 MHz HD LBW, 1.4 MHz SD LBW LBW_INC[1:0] = 01: 5.0 MHz HD LBW, 1.4 MHz SD LBW LBW_INC[1:0] = 10: 3.5 MHz HD LBW, 1.0 MHz SD LBW LBW_INC[1:0] = 11: (default) 1.5 MHz HD LBW, 0.52 MHz SD LBW	Internal pull up	I-CMOS
SWING/RSVD	39	Input control signal to reduce the output swing of the DDO/$\overline{\text{DDO}}$ outputs This is an added function on the M21215 that is mapped to a RSVD pin on the GS1535. SWING = High: GS1535 compatible output levels (floating default) SWING = Low: Reduced output swing	Internal pull up	I-CMOS
$\overline{\text{LVPECL}}$/RSVD	40	Input control signal to shift the output common mode level to enable DC coupling to downstream LVPECL receivers. This is an added function on the M21215 that is mapped to a RSVD pin on the GS1535. $\overline{\text{LVPECL}}$ = High: GS1535 compatible output common-mode (floating default) $\overline{\text{LVPECL}}$ = Low: Common-mode shift for DC couple to LVPECL	Internal pull up	I-CMOS
N/C	29	Reserved testing pin, leave floating	-	-

NOTES:

1. Internal pull-up/pull-down is 100 KΩ.
2. NAME/RSVD Indicates additional features of the M21215 that are mapped to the reserved pins of the GS1535. When left floating as recommended by the GS1535 data sheet, the M21215 defaults to a pin for pin and functionally compatible mode.

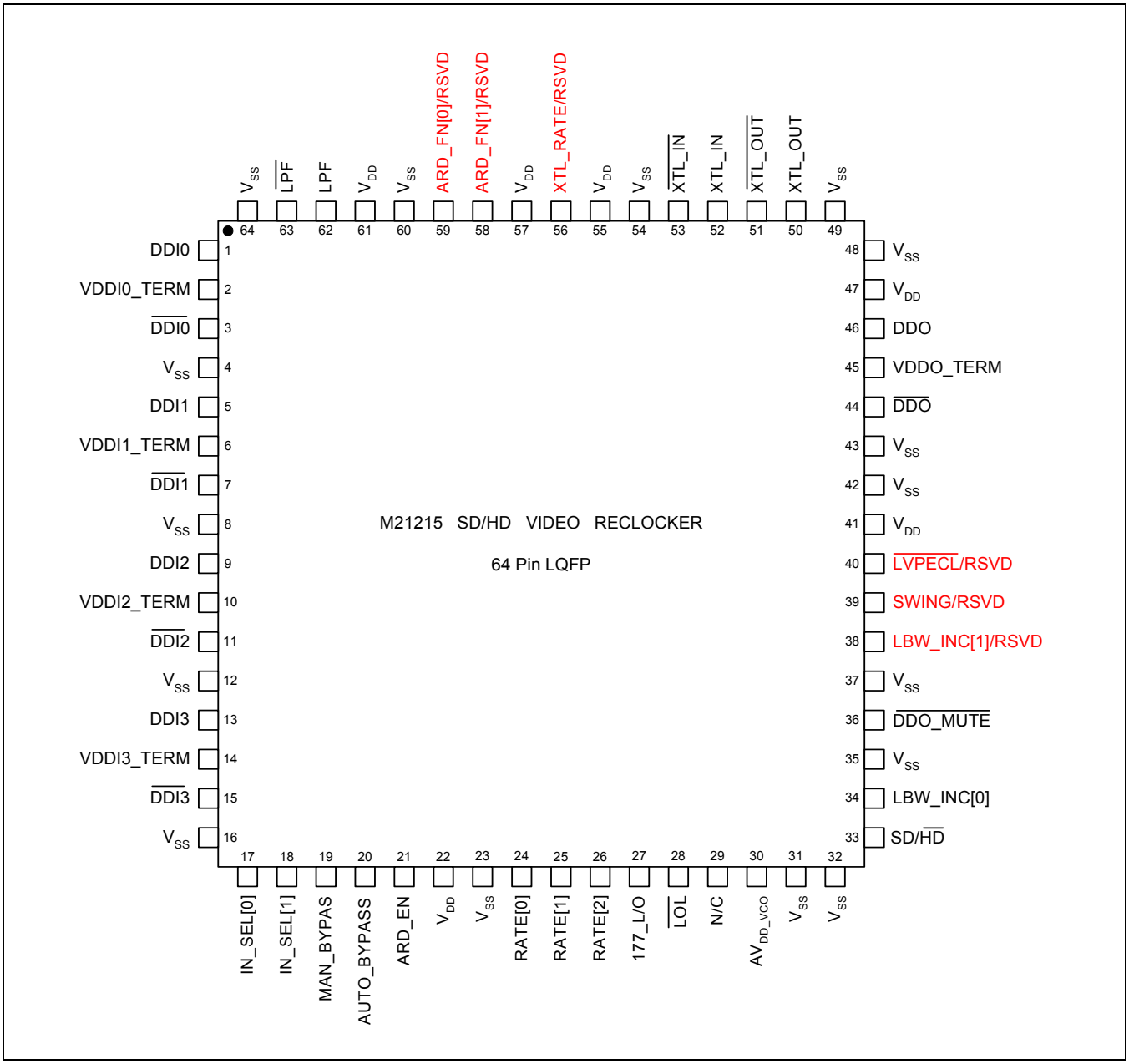
Table 1-2. Power Pins

Pin Name	Pin #	Function	Type
V_{SS}	4,8,12,16,23,31,32,35,37,42,43,48,49,54,60,64	Power Supply Ground	Power
V_{DD}	22,41,47,55,57,61	Positive Power Supply	Power
AV_{DD_VCO}	30	VCO Power Supply This pin should be connected to a “quiet” power supply.	Power

Table 1-3. High-speed Signal Pins

Pin Name	Pin #	Function	Default	Type
DDI/$\overline{\text{DDI}}$[3:0]	1,3,5,7,9, 11,13,15	Non-inverting and inverting high speed serial data inputs. Inputs are compatible with PCML, LVDS, or LVPECL voltage levels.	100Ω differential	I-High-speed
VDDI_TERM[3:0]	2,6,10,14	Input termination pin (center tap for 100Ω) Case 1: Tie to a positive supply for 50Ω to supply terminal Case 2: Leave floating and decouple to ground for 100Ω differential		I-Low-speed
DDO/$\overline{\text{DDO}}$	44,46	Non-inverting and inverting high speed serial data outputs.	100Ω differential	O-High-speed
VDDO_TERM	45	Output termination pins (center tap for 100Ω) Tie to a positive supply for 50Ω to supply terminal		O-Low-speed

Figure 1-1. M21215 Pin Out



1.2.2.1 Power/Reset

For a further reduction of power dissipation and to simplify the interface to the next generation of ASICs, the M21215 is designed to work at an extended power supply range from 2.5 to 3.3V compared to the 3.3V only GS1535. The M21215 reclocker automatically resets after power up thus an external reset is not required. The M21215 is fully operational 10 ms after the power supply has stabilized to within 10% of the final value.

1.2.2.2 Input Selection Multiplexer

The M21215 contains a 4:1 input selection multiplexer. The **IN_SEL[1:0]** pins select one of the four possible inputs that will be retimed by the reclocker block and passed to the output. The mapping of the multiplexer pins is shown in Table 1-1. If the **IN_SEL[1:0]** pins are left floating, the 4:1 input multiplexer defaults to input **DDI0/$\overline{\text{DDI0}}$.**

1.2.2.3 High-Speed I/O Pins

The high-speed inputs are designed to be used in both AC coupled and DC coupled (PCML, LVDS, and LVPECL) modes. The high-speed differential inputs contain on-chip 50Ω termination from **DDI[n]** to **VDDI_TERM[n]** as well as from **$\overline{\text{DDI[n]}}$** to **VDDI_TERM[n]**. With **VDDI_TERM[n]** tied to **V_{DD}**, the single-ended input impedance is 50Ω. This mode is recommended for AC coupled inputs or with DC coupled PCML when the PCML is driven from the same supply voltage. For use in other DC coupled situations, it is recommended that the termination voltage for the M21215 be floated. For backwards compatibility with the GS1535, **VDDI_TERM[n]** contains a weak internal bias near **V_{DD}** and the pin can be left floating for direct connection to the M21214 or the GS1524. In all cases, **VDDI_TERM[n]** should be decoupled to **V_{SS}** to reduce input noise with a 10nF capacitor. The GS1535 compatible input and an alternative is shown in Figure 1-2 and Figure 1-3.

Figure 1-2. Input Circuit for GS1535 Drop-in

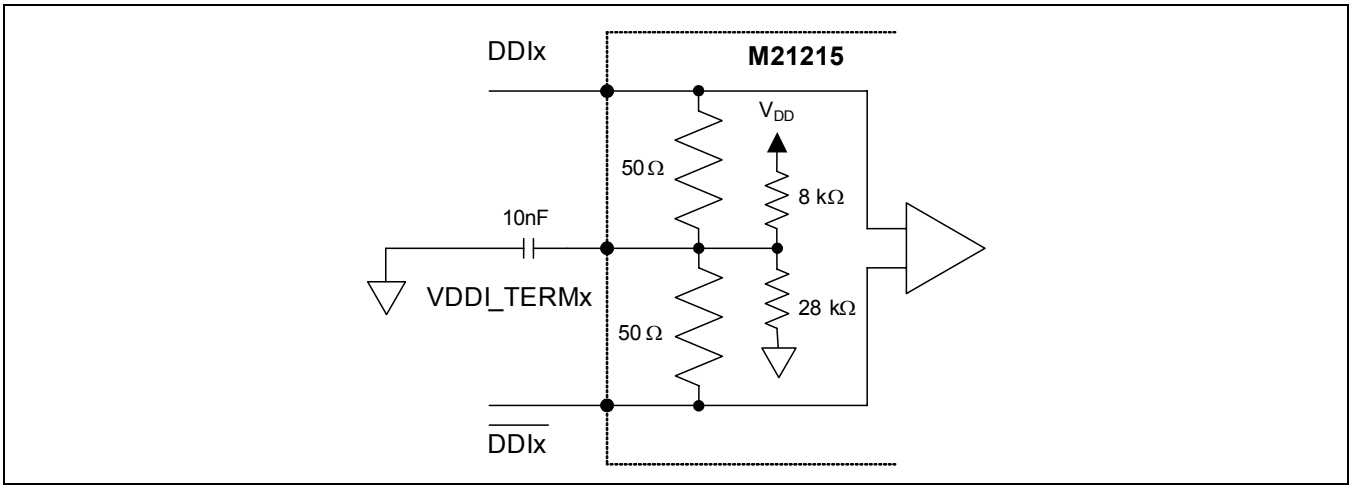
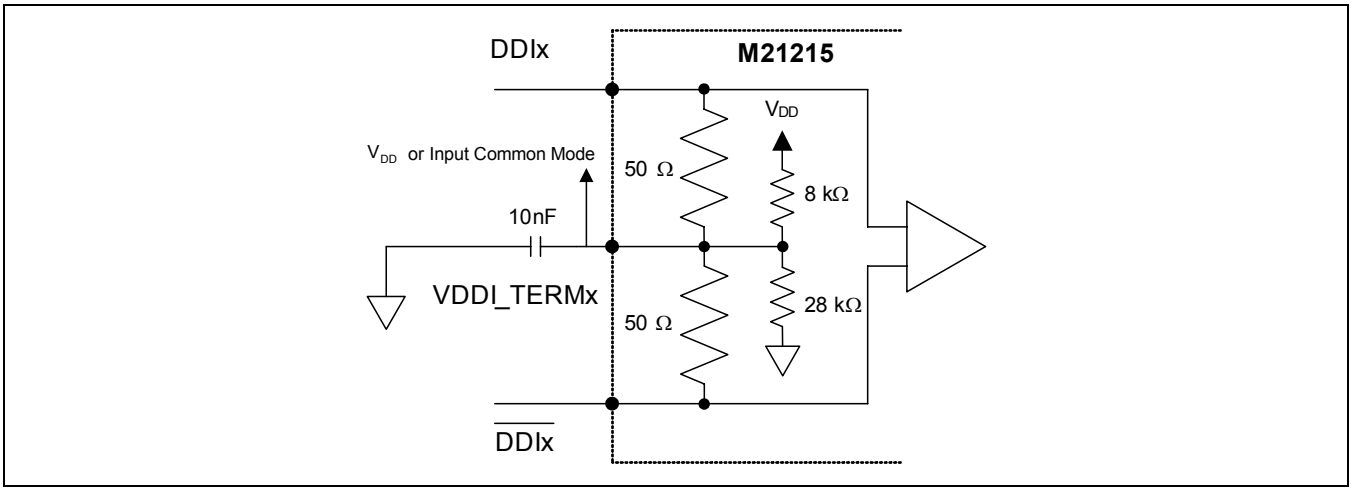


Figure 1-3. Input circuit for DC/AC coupled General Case



The high-speed output contains integrated 50Ω resistors from both **DDO** and **$\overline{\text{DDO}}$** to **VDDO_TERM**. **VDDO_TERM** should be bypassed to **V_{SS}** with a 10nF capacitor. By default, assuming all of the GS1535 reserved pins mapped to **SWING** and **$\overline{\text{LVPECL}}$** are floating, the M21215 defaults to the GS1535 output swing and common mode. **VDDO_TERM** is internally biased to **V_{DD}**.

If **$\overline{\text{LVPECL}}$** = High or floating, setting **SWING** = Low will reduce the swing from 1600 mV differential peak to peak to 800 mV differential peak to peak for a reduction in power dissipation. If **$\overline{\text{LVPECL}}$** = Low, then the LVPECL-compatible mode is selected which results in the proper LVPECL swing of approximately 1600 mVpp differential and **VDDO_TERM** is automatically biased for the proper common mode. This mode operates if **V_{DD}** = 3.3V.

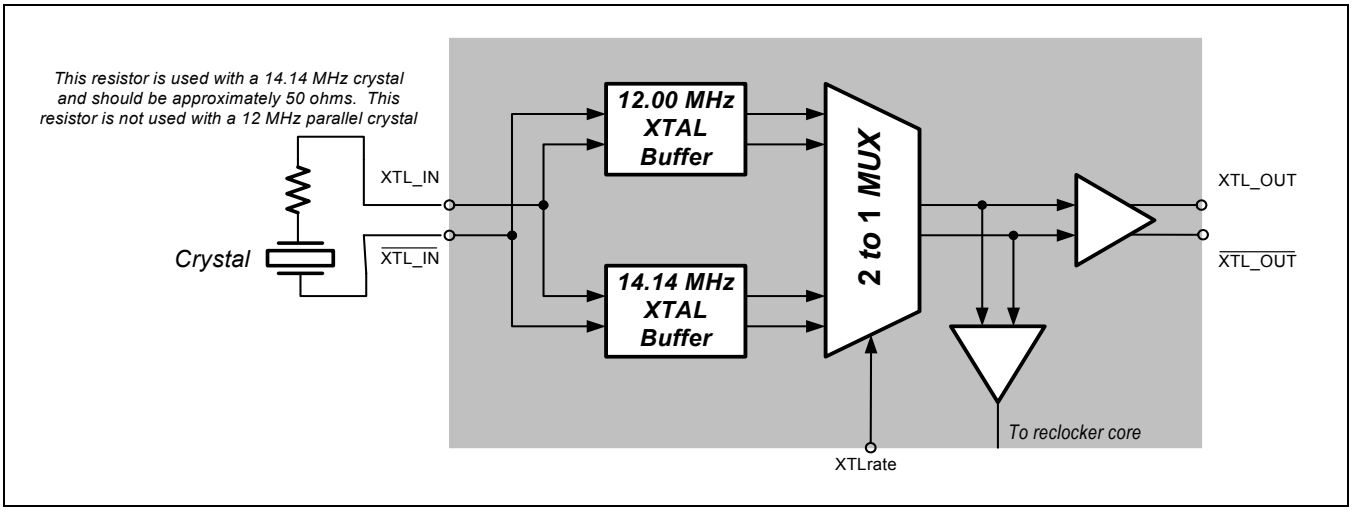
1.2.2.4 Reclocker Reference Frequency

The reclocker frequency acquisition requires an external crystal connected to **XTL_IN/$\overline{\text{XTL_IN}}$**. For daisy-chained reclocker applications, a buffered reference output is made available on **XTL_OUT/$\overline{\text{XTL_OUT}}$**.

Unlike the GS1535, the input reference frequency can be either 12.000 MHz or 14.140 MHz. By default, if **XTL_RATE** = High or Floating, the M21215 expects a 14.140 MHz series resonance crystal. The M21215 can also be used with a 12.000 MHz parallel resonance crystal which was selected based on the fact that it is a commonly-stocked low cost standard rate crystal. For pin to pin replacement applications, it is recommended that a 14.140 MHz series resonant crystal with the same form factor as the GO1535 crystal be used. With **XTL_RATE** = Low, the 12.000 MHz crystal option is selected. This mode supports both parallel and series resonance crystals. A 56Ω resistor is recommended for the series resonance case and the series resistor is set to 0 Ω for the 12.000 MHz parallel resonance crystal.

When a 14.14 MHz series or 12.00 MHz parallel resonant crystal is used with the M21215, the crystal should be connected as shown in Figure 1-4 below.

Figure 1-4. Application circuit when a series or parallel resonant crystal is used



The series resonant crystal should operate at 14.14MHz with a frequency stability of +/- 50 ppm or better, equivalent series resistance of 80Ω or less, drive level of < 0.2 mW, and static capacitance of less than 5.0 pF. The parallel resonant crystal should operate at 12.00 MHz with a frequency stability of +/- 50 ppm or better, equivalent series resistance of 80Ω or less, drive level of < 0.2 mW, and static capacitance of less than 5.0 pF.

The M21215 can also operate with a reference from an external clock buffer or oscillator instead of a crystal. The M21215 can accept a single ended or differential 14.14 MHz reference clock, and a single ended 12.00 MHz reference clock. When driving the M21215 with a single ended reference clock, the clock signal should be connected to the **XTL_IN** pin and the **$\overline{\text{XTL_IN}}$** pin should be left floating. If a 14.14 MHz reference clock is used,

the **XTL_RATE** pin must be pulled high, and if a 12.00 MHz reference clock is used, the **XTL_RATE** pin must be pulled low for proper operation of the M21215. If the **XTL_IN** pins on the M21215 are connected to a clock driver or oscillator, the requirements for the signal connected to the M21215 are detailed in Table 1-4.

The XTL_RATE pin has an internal pull up, so for default 14.140MHz operation, it can be left floating (as in GS1535) and doesn't require an external pull up.

Table 1-4. Reference Clock/Oscillator Input Specifications

Mode	14.14 MHz reference frequency		12.00 MHz reference frequency	
	Min	Max	Min	Max
Input Common Mode	V_{DD}-2.0	V_{DD}-1.2	0.8	1
Differential input swing (p-p)	500mV		N/A	N/A
Single ended input swing (p-p)	250mV		600mV	
Drive Impedance		60Ω		60Ω

NOTES:

1. When driving a reference clock single ended, connected the clock signl to the **XTL_IN** pin and leave the **$\overline{\text{XTL\_IN}}$** pin floating.
2. With a 12.00 MHz reference frequency, differential input is not supported.
3. TTL Input levels are supported for both 12.00 MHz and 14.14 MHz reference frequencies.
4. With a 14.14 MHz reference, the reference signal can be cascaded from one M21215 to another.

1.2.2.5 Reclocker Loop Bandwidth

Unlike the GS1535, the loop filter for the M21215 reclocker is fully integrated into the part. As a result, **LPF/$\overline{\text{LPF}}$** pins are used for Mindspeed testing and should be left floating. This can be accomplished by not populating the loop filter capacitor used with the GS1535. As in the GS1535, when **LBW_INC[0]** =Floating, a lower bandwidth of 1.5 MHz for 1485 Mbps data rates and 0.52 MHz for 270 Mbps data rates is selected.

For other SD-SDI rates, the bandwidth scales proportionately to the bit rate, using the 270 Mbps as a reference point. For example, at 540 Mbps, the bandwidth is 2x the 270 Mbps bandwidth. When **LBW_INC[0]** = Low, the bandwidth increases to 3.5 MHz for 1485 Mbps data rates and 1 MHz for 270 Mbps data rates.

For improved synchronous lock time, the M21215 offers a still higher loop bandwidth option of 5 MHz for 1485 Mbps data rates and 1.4 MHz for 270 Mbps data rates when **LBW_INC[0]** and **LBW_INC[1]** =Low. **LBW_INC[1]** is a GS1535 RSVD pin that is mapped as an additional feature in the M21215.

Table 1-5. Loop Bandwidth Control Settings

LBW_INC[1]	LBW_INC[0]	HD LOOP BANDWIDTH SETTING (1485 Mbps)	SD LOOP BANDWIDTH SETTING (270 Mbps)
0	0	5.0 MHz	1.4 MHz
0	1	5.0 MHz	1.4 MHz
1	0	3.5 MHz	1.0 MHz
1	1	1.5 MHz (default)	0.52 MHz (default)

NOTE:

Typical values. Loop bandwidth scales to lower frequency with reduced data rates.

1.2.2.6 Loss of Lock Alarm

A loss of lock alarm pin, **$\overline{\text{LOL}}$**, is provided to indicate if the reclocker is in lock. When the reclocker has achieved lock, **$\overline{\text{LOL}}$** = High. If the reclocker is out of lock, **$\overline{\text{LOL}}$** = Low. For synchronous switching at the same data rate, the lock time is lower if a higher loop bandwidth is selected.

1.2.2.7 Auto Rate Detect (ARD)

The reclocker is designed to operate in two modes. In the first mode, with **ARD_EN** = High, the Auto Rate Detect is enabled which automatically locks the CDR to the rates typically used in SD-SDI, HD-SDI, and DVB-ASI applications. The locked data rate is then reported with the **RATE[2:0]** pins as shown in Table 1-6.

The M21215 does not have any of the false lock issues exhibited by the GS1535 with DVB/ASI 8b/10b encoded data or idle patterns; however, for backwards compatibility, it is possible to lock out the 177 Mbps data rate by setting **177_L/O** = High which removes 177Mbps from the ARD search sequence.

Note that this pin is only active if **ARD_EN** = High. With the ARD disabled (**ARD_EN** = Low), the reclocker locking frequency is forced by using the **RATE[2:0]** pins as inputs and selecting the data rate as shown in Table 1-7. In this case, there are two additional non-standard rates that are supported by the M21215 part.

Table 1-6. Rate Report Mapping when ARD is Enabled

RATE[2:0]	Bit Rate
000b	143 Mbps
001b	177 Mbps
010b	270 Mbps
011b	360 Mbps
100b	540 Mbps
101b	1485/1483.5 Mbps

Table 1-7. Rate Select with ARD Disabled

RATE[2:0]	Bit Rate
000b	143 Mbps
001b	177 Mbps
010b	270 Mbps
011b	360 Mbps
100b	540 Mbps
101b	1485/1483.5 Mbps

For system reporting purposes as well as to set the output slew rate on the cable drivers, the **SD/$\overline{\text{HD}}$** output is used to indicate if the reclocker has locked to a HD rate. For SD-SDI rates, **SD/$\overline{\text{HD}}$** = High and for the HD-SDI rate **SD/$\overline{\text{HD}}$** =Low. This pin is used to set the output slew rate of the downstream cable driver.

To improve on the asynchronous lock times, the M21215 offers several options with the ARD algorithm. In a drop in application where **ARD_FN[1:0]** = Floating (11b by default), the ARD search order is the same as and compatible with GS1535. In the worst case, the ARD algorithm would result in an asynchronous lock time at last search rate in a maximum of 2 ms which is a 5x improvement over the GS1535.

177_L/O = High would remove the 177 Mbps rate from the search sequence resulting in a slightly faster asynchronous lock time but as there are not any false locking issues with DVB-ASI with the M21215 this is not required.

Also, if the M21215 is out-of-lock, the search pattern will not start unless the M21215 detects that there are transitions in the data through an internal loss of signal detector. To reduce the lock time even further, the M21215 offers several alternative ARD search sequences that are set with **ARD_FN[1:0]** and these are summarized in Table 1-8.

Table 1-8. ARD Search Pattern Selections

ARD_FN[1:0]	ARD Search Sequences
11b (default)	start→143→177→270→360→540→1483.5/1485→repeat
10b	start→270→360→540→1485/1483.5→repeat
01b	start→270→360→1485/1483.5→repeat
00b	start→270→1485/1483.5→repeat

1.2.2.8 Bypass and $\overline{\text{DDO\_MUTE}}$

The reclocker can be forced into the bypass mode (input data to output without retiming) with **MAN_BYPASS** = High. With **MAN_BYPASS** = Low (normal operation), **AUTO_BYPASS** = High enables the auto bypass mode that puts the reclocker into the bypass mode whenever $\overline{\textbf{LOL}}$ = Low (ie. the reclocker is out of lock).

This implies that if both **MAN_BYPASS** and **AUTO_BYPASS** = Low, when the reclocker is not in lock, undefined data may pass to the output. This mode may be used for troubleshooting or debug purposes.

The reclocker output can be forced to a logic low with $\overline{\textbf{DDO\_MUTE}}$ = Low. This function can be used to squelch the retimed noise output, or random transitions that are generated by AC coupled inputs when the upstream signals are disconnected.

Table 1-9. Manual and Auto Bypass Settings

MAN_BYPASS	AUTO_BYPASS	Functional Description
0	0	Retimed Reclocker Output
0	1	Bypass if Reclocker out of lock
1	0	Forced Bypass
1	1	Forced Bypass

2.0 Product Specification

2.1 General Specifications

Table 2-1. Absolute Maximum Ratings (1)

Symbol	Parameter	Minimum	Maximum	Units
V_{DD}	Device Power	V_{SS} - 0.5	V_{SS} + 3.6	V
V_{HS}	High-Speed Signal Pins	V_{SS} - 0.5	V_{SS} + 0.5	V
V_{ID}	Control/Interface Pins	V_{SS} - 0.5	V_{SS} + 0.5	V
T_{STORE}	Storage Temperature	–65	+150	°C
ESD_{HBML}	Human Body Model (low-speed pins)	2000	—	V
ESD_{HBMH}	Human Body Model (high-speed pins)	2000	—	V
ESD_{CDM}	Charged Device Model	500	—	V
I_{DC}	Maximum DC input current	—	25	mA

NOTE:

1. No Damage

Table 2-2. Recommended Operating Conditions

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
V_{DD}	Device Power	—	2.375	2.5/3.3	3.47	V
V_{SS}	V_{SS}: Chip Ground	—	—	0	—	V
T_{AMB}	Ambient Temperature	—	-10	—	+85	°C
θ_{JA}	Junction to ambient Thermal Resistance	—	—	40	—	°C/W

Table 2-3. DC Power Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
Total I_{DD}	Total I_{DD}(constant for all supply voltages)	1, 3	—	130	150	mA
Total $P_{DISS2.5V}$	Total P_{DISS} (@2.5V)	2	—	325	395	mW
Total $P_{DISS3.3V}$	Total P_{DISS} (@3.3V)	2	—	430	520	mW

NOTES:

1. Entire table specified at recommended operating conditions - see Table 2-2.
2. Typical computed with nominal power supply voltage, maximum computed with nominal +5% power supply voltage.
3. Current specified with 800 mV differential output swing.

2.2 Input/Output Level Specifications:

Table 2-4. CMOS I/O Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
V_{OH}	Output Logic High	1	0.8 x V_{DD}	V_{DD}	—	V
V_{OL}	Output Logic Low	1	—	0.0	0.2 x V_{DD}	V
I_{OH}	Output Current (logic high)	—	-10	—	0	mA
I_{OL}	Output Current (logic low)	—	0	—	10	mA
V_{IH}	Input Logic High	—	0.75 x V_{DD}	—	V_{DD} + 0.3	V
V_{IL}	Input Logic Low	—	0	—	0.25 x V_{DD}	V
I_{IH}	Input Current (logic high)	—	-100	—	100	µA
I_{IL}	Input Current (logic low)	—	-100	—	100	µA

NOTE:

1. Entire table specified at recommended operating conditions - see Table 2-2. Specification is for a maximum load of 20 pF.

Table 2-5. High-Speed Input Electrical Specifications (1)

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DR_{IN}	Input Bit Rate (reclocker bypassed)	—	0	—	1500	Mbps
DR_{IN}	Input Bit Rate (reclocker enabled)	—	143	—	1485	Mbps
V_{ID}	Input Differential Voltage (peak - peak)	2,3	100	—	2000	mV
V_{ICM}	Input Common-Mode Voltage	—	V_{SS} + 1.15	—	AV_{DD}	V
V_{IMAX}	Maximum Input High Voltage	—	—	—	AV_{DD} + 400	mV
V_{IMIN}	Minimum Input Low Voltage	—	V_{SS}+1.0	—	—	V
$\Delta V_T T$	Maximum voltage difference between input common-mode voltage and **VDDI_TERM[3:0]**	—	—	—	600	mV
R_{IN}	**VDDI_TERM[3:0]** input termination impedance to AV_{DD}	—	40	50	60	Ω

NOTES:

1. Specified at recommended operation conditions-see Table 2-2
2. Example 1200 mV_{pp} differential = 600 mV_{pp} for each single-ended terminal
3. Minimum input level defined as error free operation at 10^{-12} BER with PRBS input pattern

Table 2-6. High-speed Output Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
t_r/t_f	Rise/Fall Time (20-80%) for all levels	—	—	120	150	ps
V_{OCM}	**SWING** = High; $\overline{\textbf{LVPECL}}$ = High: Output Common Mode Voltage	—	V_{DD} –525	—	V_{DD} –350	mV
V_{OD}	**SWING** = High; $\overline{\textbf{LVPECL}}$ = High: Differential Output Voltage Swing	4	1300	1600	2000	mV
V_{OCM}	**SWING** = Low; $\overline{\textbf{LVPECL}}$ = High: Output Common Mode Voltage	—	V_{DD} –265	—	V_{DD} –200	mV
V_{OD}	**SWING** = Low; $\overline{\textbf{LVPECL}}$ = High: Differential Output Voltage Swing	4	600	800	1000	mV
V_{OCM}	**SWING** = High; $\overline{\textbf{LVPECL}}$ = Low: Output Common Mode Voltage	3	V_{DD} – 1400	—	V_{DD} – 1200	mV
V_{OD}	**SWING** = High; $\overline{\textbf{LVPECL}}$ = Low: Differential Output Voltage Swing	3, 4	1300	1600	2000	mV
V_{OCM}	**SWING** = Low; $\overline{\textbf{LVPECL}}$ = Low: Output Common Mode Voltage	3	V_{DD} –1000	—	V_{DD} –1100	mV
V_{OD}	**SWING** = Low; $\overline{\textbf{LVPECL}}$ = Low: Differential Output Voltage Swing	3, 4	600	800	1000	mV
R_O	**VDDO_TERM** Termination impedance to $\mathbf{V_{DD}}$	—	40	50	60	Ω

NOTES:

1. Specified at recommended operating conditions – see Table 2-2
2. Example 1200 mV $_{P-P}$ differential = 600 mV $_{P-P}$ for each single-ended terminal.
3. Operation with $\overline{\text{LVPECL}}$ = Low is valid when V_{DD} = 3.3V only.
4. Measured with a 50Ω high speed oscilloscope.

2.3 Reclocker Performance Specifications

Table 2-7. Reclocker Output Jitter Performance

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
J_{ERMS}	Reclocker Enabled Output Data Jitter @ 1.485 Gbps (RMS)	1,2	—	5.5	9	ps
J_{EPP}	Reclocker Enabled Output Data Jitter @ 1.485 Gbps (pp)	1,2	—	38	55	ps
J_{EPP}	Reclocker Enabled Output Data Jitter @ 1.485 Gbps (pp)	1,2	—	56	80	mUI
J_{BRMS}	Reclocker Bypassed Output Data Jitter @ 1.485 Gbps (RMS)	1,2	—	—	6	ps
J_{BPP}	Reclocker Bypassed Output Data Jitter @ 1.485 Gbps (pp)	1,2	—	—	35	ps
J_{BPP}	Reclocker Bypassed Output Data Jitter @ 1.485 Gbps (pp)	1,2	—	—	52	mUI
J_{EPP}	Reclocker Enabled Output Data Jitter @ < 600 Mbps (pp)	1,2	—	—	40	mUI
J_{ERMS}	Reclocker Enabled Output Data Jitter @ < 600 Mbps (RMS)	1,2	—	—	6.7	mUI
J_{BPP}	Reclocker Bypassed Output Data Jitter @ < 600 Mbps (pp)	1,2	—	—	30	mUI
J_{BRMS}	Reclocker Bypassed Output Data Jitter @ < 600 Mbps (RMS)	1,2	—	—	5	mUI

NOTES:

1. All jitter is measured using a 2^{23}-1 PRBS pattern, and/or HD/SD-SDI color bar test pattern.
2. All jitter is measured using a wideband scope (minimum 10 GHz bandwidth).

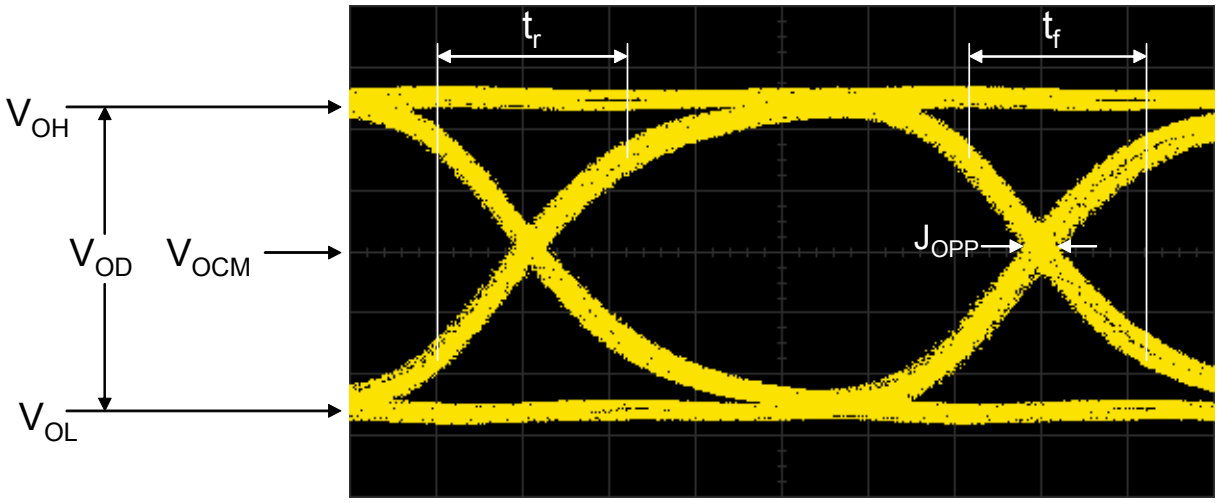
Table 2-8. Reclocker High-speed Performance

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
J_{TOL}	PLL pathological pattern jitter tolerance	2	0.4	—	—	UI
L_{BWPK}	Loop bandwidth peaking	3	—	0.1	—	dB
t_{LKA}	Asynchronous Lock (Auto Rate Detect lock time)	4	—	2	5	ms
t_{LKS}	Synchronous Switch Lock TIme @ 1.485 Gbps	5	—	110	150	ns
t_{LKS}	Synchronous Switch Lock TIme @ 270 Mbps	5	—	330	400	ns

NOTES:

1. Entire table specified at recommended operating conditions – see Table 2-2.
2. Jitter tolerance is measured with pathological test pattern.
3. **LBW_INC[1]** is a GS1535 RSVD pin that is mapped as an additional Loop Bandwidth boost pin for faster lock times on the M21215.
4. Switching from one data rate to a different data rate.
5. Switching from one data rate to the same data rate.

Figure 2-1. Output Symbols Definition



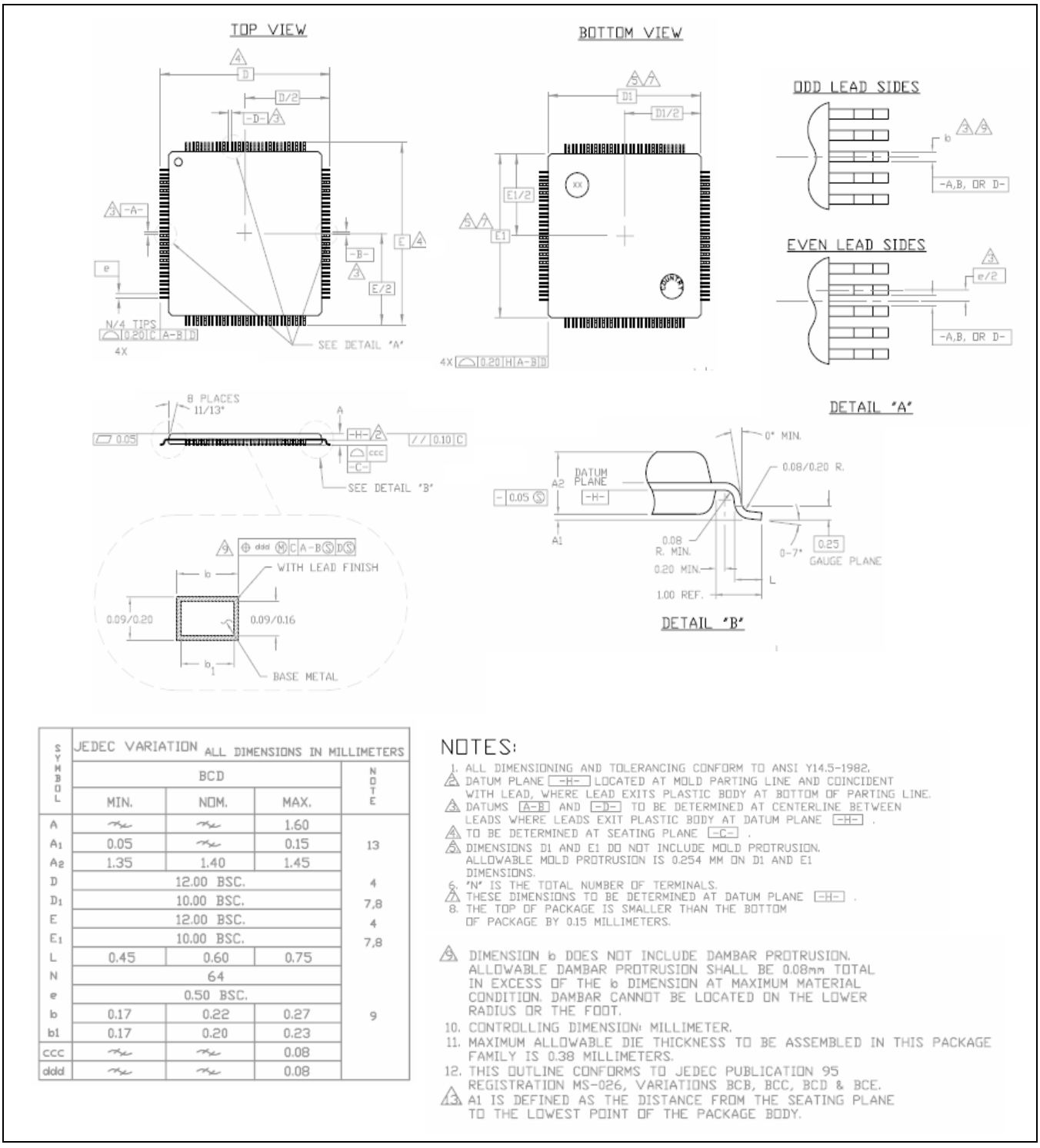
V_{OH}: Average voltage high level
V_{OL}: Average voltage low level
V_{OD}: (VOH) – (VOL)
V_{OCM}: Common Mode Voltage
J_{OPP}: Output Jitter Peak-Peak
t_r: 20-80% Rise Time
t_f: 80-20% Fall Time

NOTE: Waveform above is differential.

2.4 Package Specification

The M21215 is available in a 64 pin 10mm x 10mm LQFP package. The package drawing is shown in Figure 2-2. The M21215 is available in a package that is fully RoHS compliant.

Figure 2-2. Package Drawing



SYMBOL	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			NOTE
	BCD			
	MIN.	NOM.	MAX.	
A	---	---	1.60	
A1	0.05	---	0.15	13
A2	1.35	1.40	1.45	
D	12.00 BSC.			4
D1	10.00 BSC.			7,8
E	12.00 BSC.			4
E1	10.00 BSC.			7,8
L	0.45	0.60	0.75	
N	64			
e	0.50 BSC.			
b	0.17	0.22	0.27	9
b1	0.17	0.20	0.23	
ccc	---	---	0.08	
ddd	---	---	0.08	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE -H- LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DATUMS A-B AND -D- TO BE DETERMINED AT CENTERLINE BETWEEN LEADS WHERE LEADS EXIT PLASTIC BODY AT DATUM PLANE -H- .
4. TO BE DETERMINED AT SEATING PLANE -C- .
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
6. "N" IS THE TOTAL NUMBER OF TERMINALS.
7. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE -H- .
8. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
9. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
10. CONTROLLING DIMENSION: MILLIMETER.
11. MAXIMUM ALLOWABLE DIE THICKNESS TO BE ASSEMBLED IN THIS PACKAGE FAMILY IS 0.38 MILLIMETERS.
12. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-026, VARIATIONS BCB, BCC, BCD & BCE.
13. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

3.0 Appendices

3.1 Glossary of Terms/Acronyms

Table 3-1. Glossary and Acronyms

ASIC	Application Specific Integrated Circuit
DTV	Digital Television
DVB	Digital Video Broadcast
EQ	Equalizer or Equalization
HD	High Definition
SD	Standard Definition
SDI	Serial Digital Interface
SMPTE	Society of Motion Picture and Television Engineers

3.2 Reference Documents

3.2.1 External

Society of Motion Picture and Television Engineers

SMPTE 292M Bit-Serial Digital Interface for High-Definition Television Systems

SMPTE 259M 10-Bit 4:2:2 Component and $4f_{SC}$ Composite Digital Signals - Serial Digital Interface

SMPTE 344M 540Mb/s Serial Digital Interface

DVB-ASI Digital Video Broadcast

www.mindspeed.com

General Information:
Telephone: (949) 579-3000
Headquarters - Newport Beach
4000 MacArthur Blvd., East Tower
Newport Beach, CA 92660