M21131/M21151

72x72/144x144 3.2 Gbps Asynchronous Crosspoint Switch with Amplif-EYE Signal Conditioning

The M21131/M21151 is a 3.2 Gbps, 72/144 lane high-speed, low-power CMOS asynchronous non-blocking crosspoint switch. It operates from DC to 3.2 Gbps making it suitable for many telecom, datacom, and broadcast video applications.

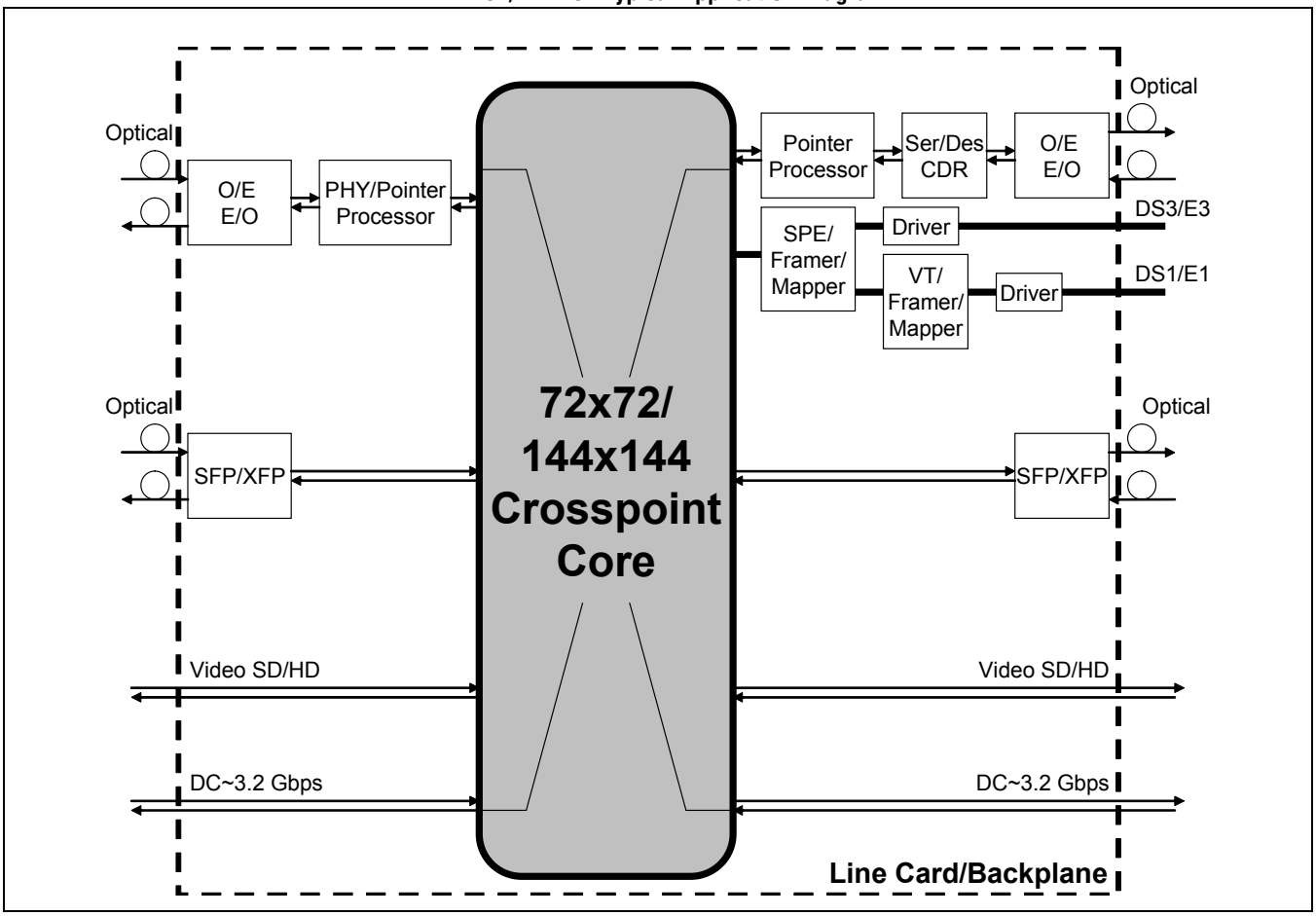
Applications

- Large NxN cascaded switch fabrics up to 10 Terabits/sec (Tbps)
- Dense-Wavelength-Division Multiplexing (DWDM) telecom/datacom Switcher/Router
- Serial Digital Video Switcher/Router (3G/HD/SD-SDI)
- Storage Area Network (SAN) Switcher/Router
- High-speed Automated Test Equipment (ATE)
- Disaster recovery and redundancy systems

Features

- 72/144 inputs by 72/144 outputs non-blocking crosspoint switch
- 3.2 Gbps Non-Return to Zero (NRZ) raw data bandwidth
- Global or individual lane programmable Input Equalization, output De-Emphasis, and drive levels
- Pinout and software compatible with the M21141/M21161
- Input signal activity monitor
- Flexible interface AVdd_IO +1.2/1.5/1.8/2.5V
- Built-in Pseudo-Random Bit Sequence (PRBS) generator/checker
- SmartPower™ dynamically reduces power consumption
- Green/RoHS compliant package

M21131/M21151 Typical Application Diagram



Ordering Information

72x72 3.2 Gbps Crosspoint Switch Ordering Information

Part Number	Package Type	Substrate Material	Green/ Eutectic	Operating Temperature	Availability
M21131-12 (1)	1156-terminal, 35 mm, BGA	Ceramic	Eutectic	0°C to 85 °C	Now
M21131G-12 (1)	1156-terminal, 35 mm, BGA	Ceramic	Green	0°C to 85 °C	Now
M21131G-13 (1,2)	1156-terminal, 35 mm, BGA	Ceramic	Green	0°C to 85 °C	Now
M21131-22	1156-terminal, 35 mm, BGA	CPCore	Eutectic	0°C to 85 °C	Production orders: 01/01/2011
M21131G-22	1156-terminal, 35 mm, BGA	CPCore	Green	0°C to 85 °C	Production orders: 01/01/2011
M21131G-23 (2)	1156-terminal, 35 mm, BGA	CPCore	Green	0°C to 85 °C	Production orders: 01/01/2011

(1) Not recommended for new designs

(2) Improved input sensitivity especially for SDI applications

144x144 3.2 Gbps Crosspoint Switch Ordering Information

Part Number	Package Type	Substrate Material	Green/ Eutectic	Operating Temperature	Availability
M21151-13 (1)	1156-terminal, 35 mm, BGA	Ceramic	Eutectic	0°C to 85 °C	Now
M21151G-13 (1)	1156-terminal, 35 mm, BGA	Ceramic	Green	0°C to 85 °C	Now
M21151G-14 (1,2)	1156-terminal, 35 mm, BGA	Ceramic	Green	0°C to 85 °C	Now
M21151-23	1156-terminal, 35 mm, BGA	CPCore	Eutectic	0°C to 85 °C	Production orders: 01/01/2011
M21151G-23	1156-terminal, 35 mm, BGA	CPCore	Green	0°C to 85 °C	Production orders: 01/01/2011
M21151G-24 (2)	1156-terminal, 35 mm, BGA	CPCore	Green	0°C to 85 °C	Production orders: 01/01/2011

(1) Not recommended for new designs

(2) Improved input sensitivity especially for SDI applications

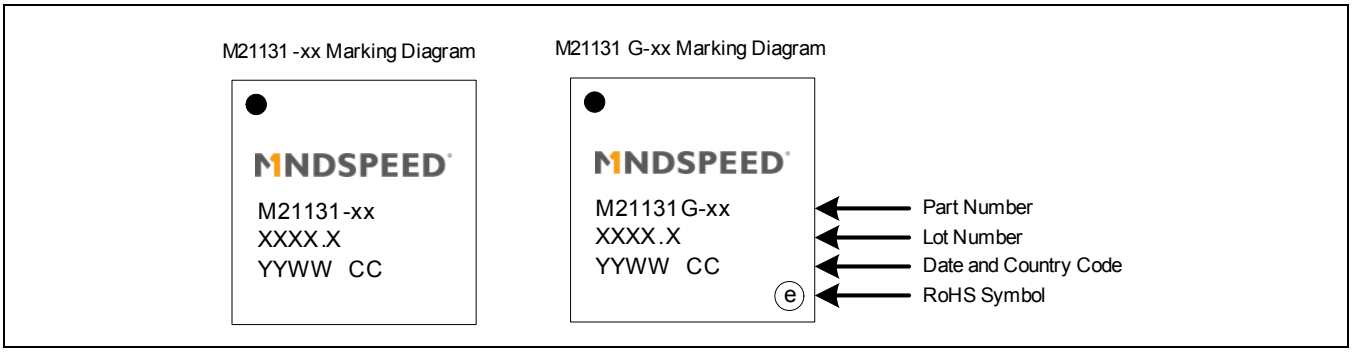
NOTE:

- Mindspeed is changing the package substrate material from Ceramic to CPCore. For traceability, the revision code will be changed from -1x to -2x to signify this change. The device silicon will remain unchanged during this transition. The differences between the CPCore and Ceramic packaged material are outlined in Section 2.1.3.
- These devices are shipped in trays.
- The letter “G” designator after the part number indicates that the device is RoHS compliant. Refer to www.mindspeed.com for additional information. The RoHS compliant devices are backwards compatible with 225 °C reflow profiles.

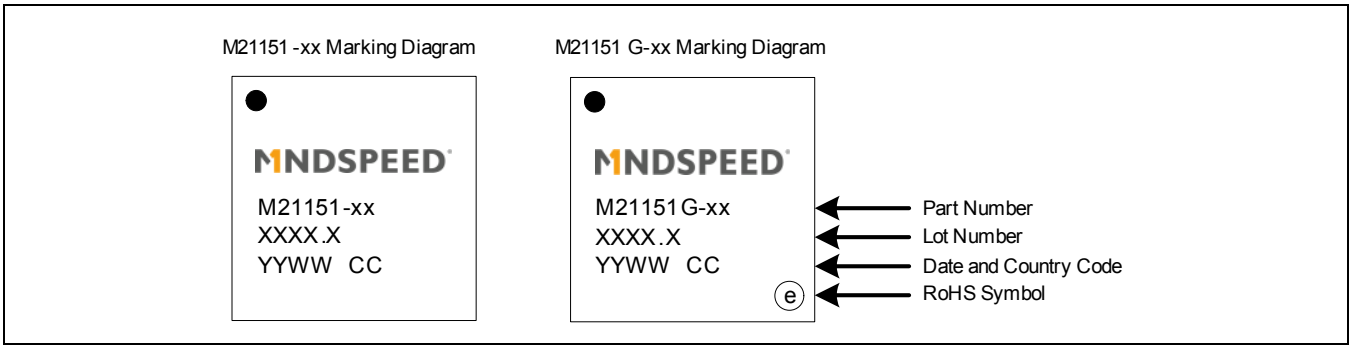
Revision History

Revision	Level	Date	Description
I	Released	December 2012	Corrected an error in table 1-1. Maximum voltage on CMOS inputs should be referenced to DVDD_IO instead of AVDD_IO
H	Released	July 2010	Expanded ordering matrix to include all current revisions.
G	Released	May 2010	Revised part numbers to -23 and -24. Corrected signal names on pin AF1 INP[117] and AF2 INN[117]. Updated Marking Diagrams. Update package from ceramic to CPCore. Please see Section 2.1.3 for package changes
F	Released	October 2009	Revised for M21131-13 part details. Added marking diagrams. Removed M21131-12 parameters from Table 1-6. Removed BGA Assignments by Ball Name Tables. Corrrected global control of de-emphasis duration values in Table 3-33.
E	Released	May 2009	See prior revisions for revision history details.
D	Released	September 2008	See prior revisions for revision history details.

M21131 Marking Diagrams



M21151 Marking Diagrams



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1.0 Electrical Characteristics

Unless noted otherwise, specifications in this section are valid with AV_{DD}_CORE = 1.2V, AV_{DD}_IO = 1.8V, and DV_{DD}_IO = 2.5V power supplies, 25 °C ambient temperature, 800 mVpp differential input/output data swing, PRBS 2^{15}– 1 test pattern at 3.2 Gbps, RL = 50Ω.

Table 1-1. Absolute Maximum Ratings (1)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
DV_{DD}_IO	Digital logic I/O supply	0		+3.6	V
AV_{DD}_IO	Switch I/O supply	0		+2.7	V
AV_{DD}_CORE	Switch core supply	0		+1.5	V
V_{CML}	DC input voltage (CML)	V_{SS} - 0.5	—	AV_{DD}_IO + 0.5	V
V_{CMOS}	DC input voltage (CMOS)	V_{SS} - 0.5	—	DV_{DD}_IO + 0.5	V
Tst	Storage temperature	-65		+150	°C
VESD	Human body model (low-speed)	1000		—	V
VESD	Human body model (high-speed)	500		—	V
VESD	Charge device model	150		—	V

NOTES:

1. Exposure to these conditions over extended periods of time may affect device reliability.

Table 1-2. Recommended Operating Conditions

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Unit
DV_{DD}_IO	Digital supply voltage	2	+1.71	+1.8/2.5/3.3	+3.47	V
AV_{DD}_IO	Analog I/O supply voltage	2	+1.14	+1.2/1.5/1.8/2.5	+2.63	V
AV_{DD}_CORE	Switch core supply voltage	2	+1.14	+1.2	+1.26	V
Tc	Package heat spreader temperature	1, 3	0	—	+85	°C
θ_{JC}	Junction to Case Thermal Resistance		0.3			C/W

NOTES:

1. Lower limit is ambient temperature and upper limit is case temperature.
2. Power supply tolerances are ±5%.
3. Please refer to the 144 XPS thermal Application Note for thermal design and bolted down heat sink recommendations for this product. The use of adhesively mounted heatsinks is prohibited.

Table 1-3. M21131 Power DC Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum(1)	Unit
AIDD_CORE	Core current consumption, small output swing, SmartPower on	1,2	—	4.2	4.4	A
	Core current consumption, small output swing, SmartPower off	1,2	—	8.6	9.0	A
AIDD_IO	I/O current consumption, small output swing, +1.2V I/O	2	—	1.3	1.4	A
	I/O current consumption, small output swing, +2.5V I/O	2	—	2.8	3.0	A
Pdiss	Power dissipation at +1.2V CORE, +1.2V I/O, SmartPower on	2	—	6.6	7.0	W
	Power dissipation at +1.2V CORE, +2.5V I/O, SmartPower on	2	—	12.1	12.8	W
AIDD_CORE	Core current consumption, medium output swing, SmartPower on	1,2	—	4.4	4.6	A
	Core current consumption, medium output swing, SmartPower off	1,2	—	8.8	9.2	A
AIDD_IO	I/O current consumption, medium output swing, +1.2V I/O	2	—	2.0	2.1	A
	I/O current consumption, medium output swing, +2.5V I/O	2	—	3.1	3.2	A
Pdiss	Power dissipation at +1.2V CORE, +1.2V I/O, SmartPower on	2	—	7.7	8.0	W
	Power dissipation at +1.2V CORE, +2.5V I/O, SmartPower on	2	—	12.9	13.5	W
AIDD_CORE	Core current consumption, high output swing, SmartPower on	1,2	—	4.5	4.7	A
	Core current consumption, high output swing, SmartPower off	1,2	—	8.9	9.4	A
AIDD_IO	I/O current consumption, high output swing, +1.2V I/O	2	—	2.5	2.7	A
	I/O current consumption, high output swing, +2.5V I/O	2	—	3.5	3.7	A
Pdiss	Power dissipation at +1.2V CORE, +1.2V I/O, SmartPower on	2	—	8.4	8.9	W
	Power dissipation at +1.2V CORE, +2.5V I/O, SmartPower on	2	—	14.2	14.9	W
DIDD_IO	Digital current consumption DV_{DD}_IO = +2.5V	2	—	0.626	25	mA

NOTES:

1. Core power supply is +1.26V, (+1.20V, +5%).
2. 1-to-1 mapping (Input0 to Output0, Input1 to Output1,...).

Table 1-4. M21151 Power DC Electrical Specifications (1)

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Unit
AIDD_CORE	Core current consumption, small output swing, SmartPower on	1,2	—	8.3	8.5	A
	Core current consumption, small output swing, SmartPower off	1,2	—	11.2	11.5	A
AIDD_IO	I/O current consumption, small output swing, +1.2V I/O	2	—	2.5	2.6	A
	I/O current consumption, small output swing, +2.5V I/O	2	—	3.6	3.7	A
Pdiss	Power dissipation at +1.2V CORE, +1.2V I/O, SmartPower on	2	—	12.9	13.3	W
	Power dissipation at +1.2V CORE, +2.5V I/O, SmartPower on	2	—	18.9	19.5	W
AIDD_CORE	Core current consumption, medium output swing, SmartPower on	1,2	—	8.4	8.7	A
	Core current consumption, medium output swing, SmartPower off	1,2	—	11.3	11.7	A
AIDD_IO	I/O current consumption, medium output swing, +1.2V I/O	2	—	3.6	3.8	A
	I/O current consumption, medium output swing, +2.5V I/O	2	—	4.7	4.9	A
Pdiss	Power dissipation at +1.2V CORE, +1.2V I/O, SmartPower on	2	—	14.4	15.0	W
	Power dissipation at +1.2V CORE, +2.5V I/O, SmartPower on	2	—	21.8	22.7	W
AIDD_CORE	Core current consumption, high output swing, SmartPower on	1,2	—	8.7	8.9	A
	Core current consumption, high output swing, SmartPower off	1,2	—	11.6	11.9	A
AIDD_IO	I/O current consumption, high output swing, +1.2V I/O	2	—	4.3	4.5	A
	I/O current consumption, high output swing, +2.5V I/O	2	—	5.5	6.1	A
Pdiss	Power dissipation at +1.2V CORE, +1.2V I/O, SmartPower on	2	—	15.5	16.1	W
	Power dissipation at +1.2V CORE, +2.5V I/O, SmartPower on	2	—	24.2	25.9	W
DIDD_IO	Digital current consumption DV_{DD}_IO = +2.5V	2	—	0.626	25	mA

NOTES:

1. Core power supply is +1.26V, (+1.20V +5%).
2. 1-to-1 mapping (Input0 to Output0, Input1 to Output1,...).

Table 1-5. CMOS DC Electrical Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{OH}	Output logic high I_{OH} = -100 µA	0.8 x DV_{DD}_IO	—	—	V
V_{OL}	Output logic low I_{OL} = 100 µA	—	—	0.2 x DV_{DD}_IO	V
V_{IH}	Input logic high	DV_{DD}_IO - 0.3	—	+3.6	V
V_{IL}	Input logic low	0	—	+0.3	V

Table 1-6. PCML Input Electrical Specifications (1)

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Unit
V_{ID}	Input differential voltage (peak-to-peak) PRBS SDI Pseudo-Pathological Pattern	1	100 —	— 350	1200 —	mV
V_{ICM}	Input common-mode voltage		—	AV_{DD}_IO - 300	—	mV
V_{IH}	Maximum input high voltage		—	—	AV_{DD}_IO + 300	mV
V_{IL}	Minimum input low voltage		AV_{DD}_IO - 800	—	—	mV
S_{11}	Input return loss (40 MHz to 2 GHz)		—	-10.0	—	dB
S_{11}	Input return loss (2 GHz to 5 GHz)		—	-5.0	—	dB

NOTES:

1. Input sensitivity specified @ 3.2 Gbps PRBS 2^{23}-1 and BER 10^{-12}.

Table 1-7. PCML Output Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Unit
DR_{OUT}	Operating data rate (NRZ data)	—	DC	—	3.2	Gbps
J_{OUTRMS}	Output data broadband jitter (RMS)	—	—	—	6.0	ps
J_{OUTP-P}	Output data broadband jitter (peak-to-peak)	—	—	—	36.0	ps
$T_{RISE/FALL}$	Rise time/fall time (20 to 80%)	2	—	—	145	ps
V_{OD}	Low swing: differential swing Medium swing: differential swing High swing: differential swing	— — 3	390 700 920	650 950 1225	700 1200 1600	mV
S_{22}	Output return loss (40 MHz to 2.5 GHz) Output return loss (2.5 GHz to 5 GHz)	1	— —	-15.0 -5.0	— —	dB
t_{DJ}	Output Deterministic Jitter (ISI)		—	125	—	mUI
t_{RJ}	Output Random Jitter		—	2	—	mUI RMS

NOTES:

1. RF parameters measured into a 50Ω load on M21131/M21151 EVM.
2. Rise/Fall time specification is for lowest output swing settings. Rise/Fall time improves with higher output swing settings.
3. Package and recommended heat sink are not rated for this mode at AV_{DD}_IO = +2.5 V due to high power dissipation; improved thermal management at the board level would be necessary to use this mode at AV_{DD}_IO = +2.5 V.

Figure 1-1. Input Equalization Test Setup

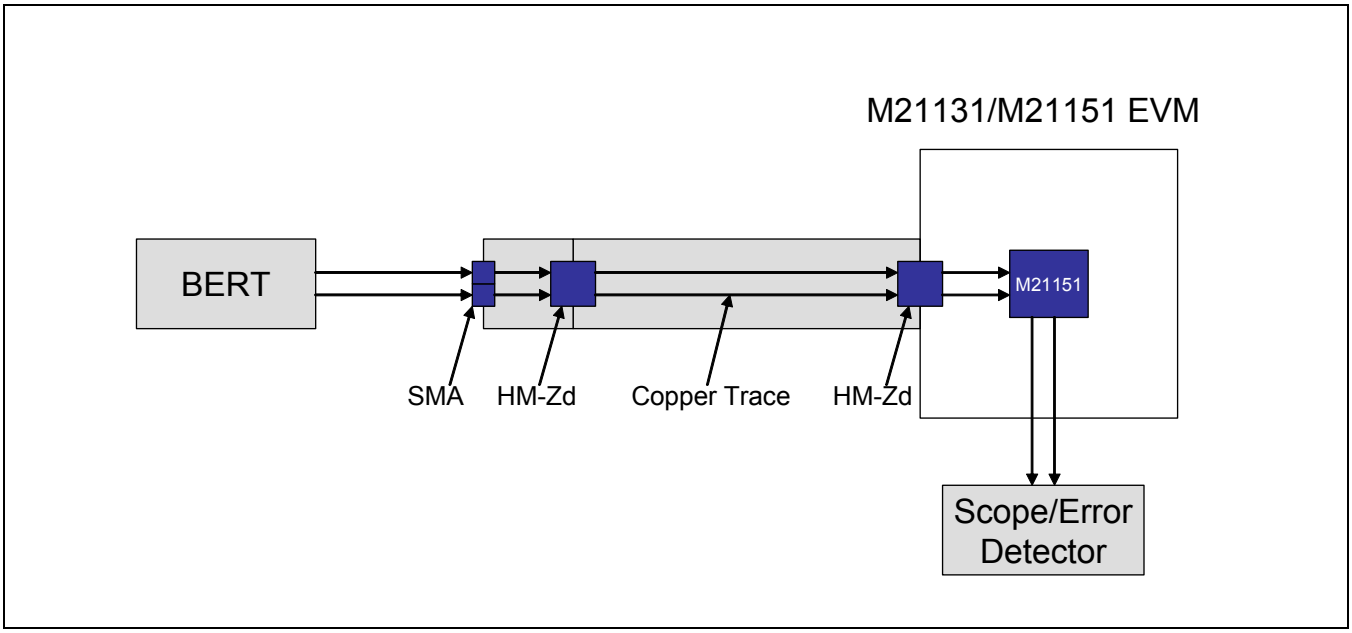
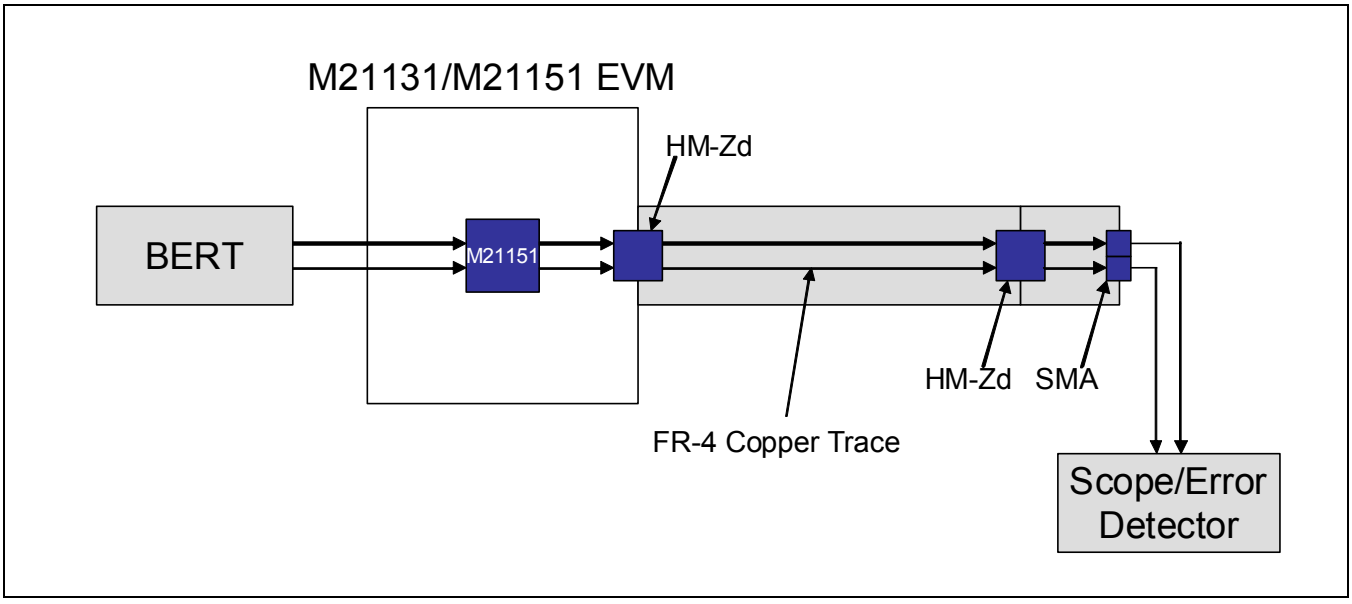


Figure 1-2. De-Emphasis Test Setup



2.0 Package Outline Drawing and Pin Descriptions

2.1 Package Outline Drawing

2.1.1 M21131 and M21151 Packaging Drawing (-12/-13/-14)

Figure 2-1 illustrates the M21131/M21151 (-12/-13/-14) overall package dimensions and a cross sectional view, Figure 2-2 is a bottom view of the package with ball assignments. The substrate thickness is 2.03 millimeters. All dimensions are in millimeters. The ball count is 1156, the width of each ball is 0.60 millimeters, and the ball pitch from center to center is 1.00 millimeters.

Figure 2-1. M21131/M21151 (-12/-13/-14) Package Outline Top View and Cross Sectional View (in mm)

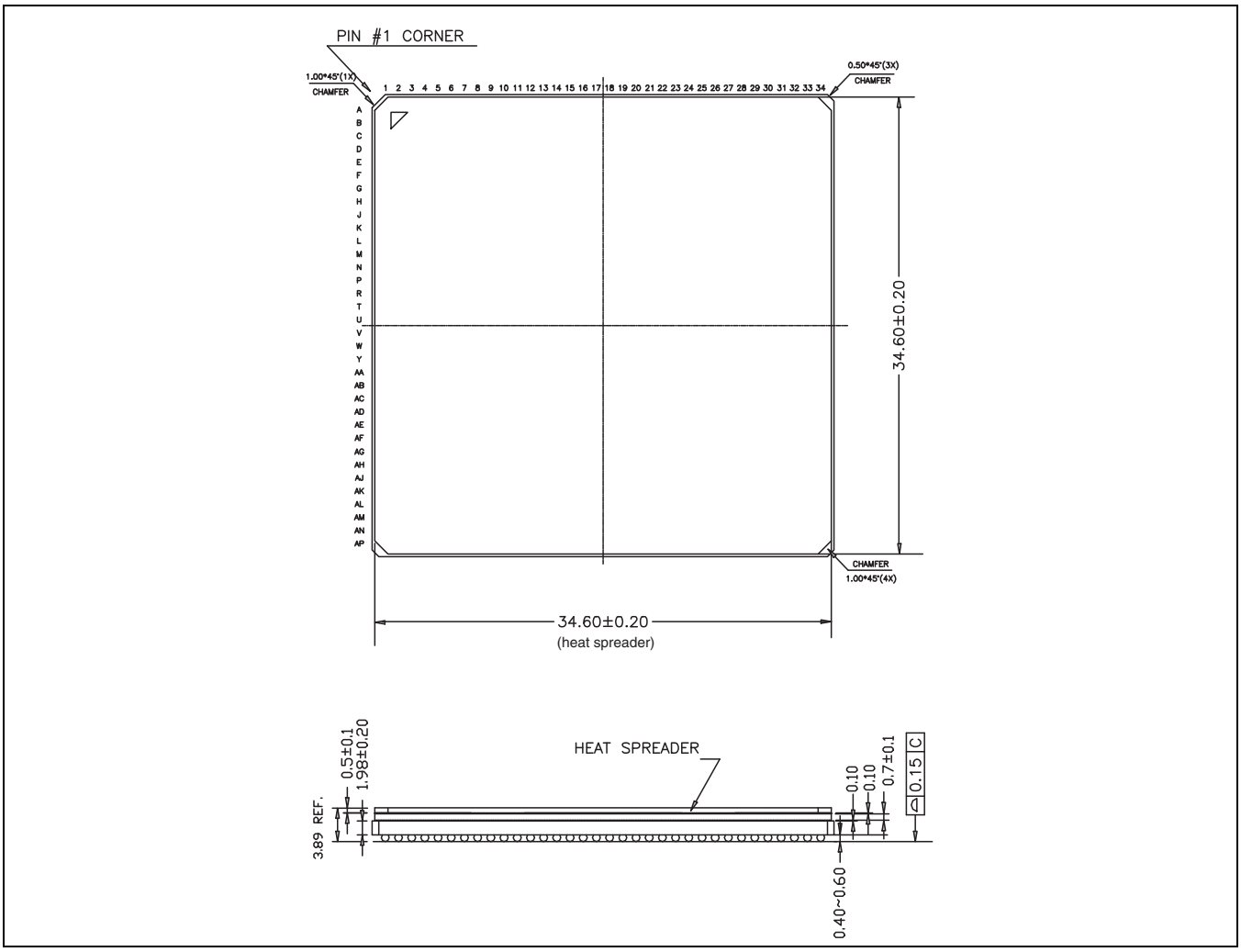
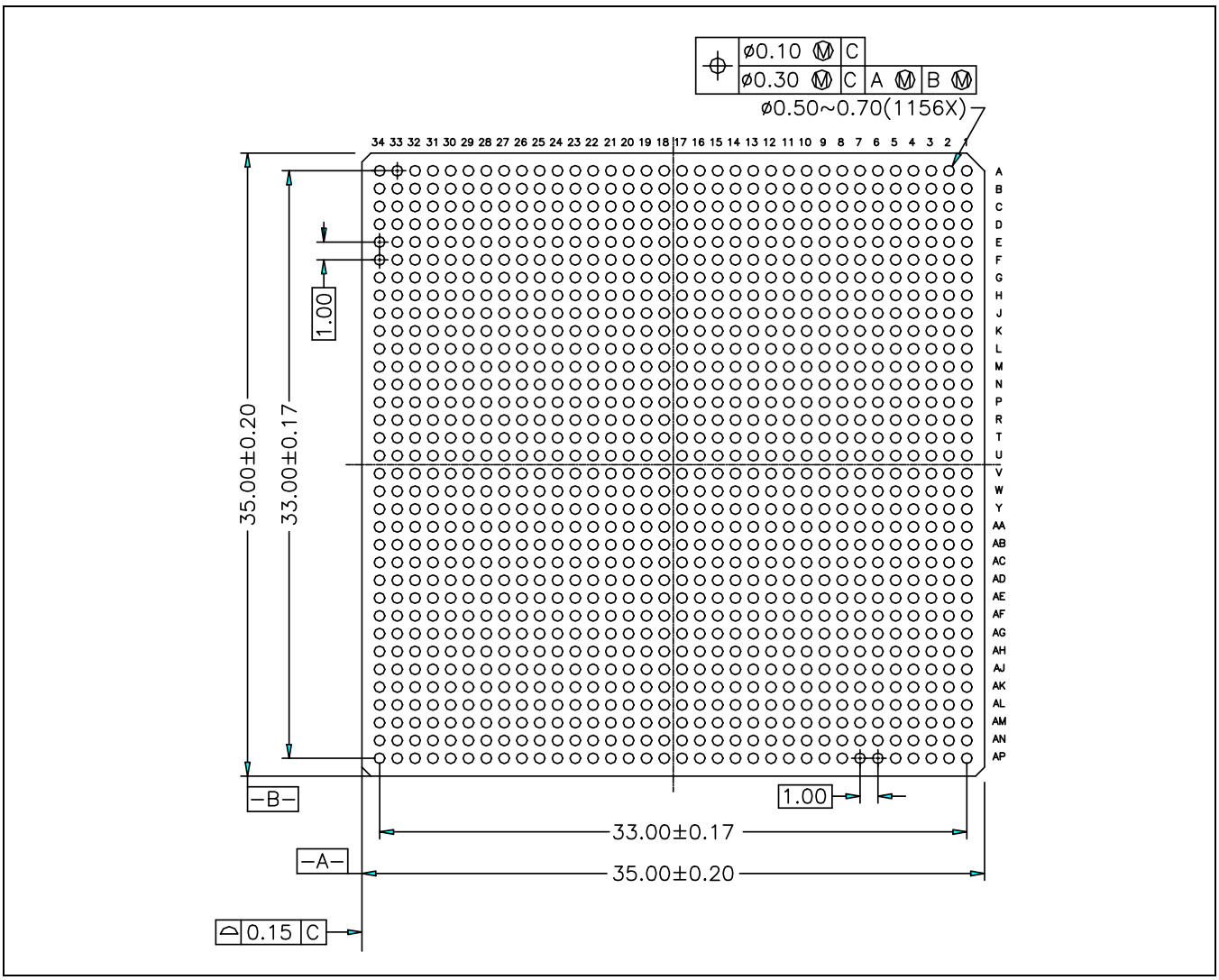


Figure 2-2. M21131/M21151 (-12-13/-14) Bottom View of Package (in mm)



2.1.2 M21131 and M21151 Packaging Drawing (-22/-23/-24)

Figure 2-3 illustrates the M21131/M21151 (-22/-23/-24) overall package dimensions and a cross sectional view, Figure 2-4 is a bottom view of the package with ball assignments. The substrate thickness is 2.03 millimeters. All dimensions are in millimeters. The ball count is 1156, the width of each ball is 0.60 millimeters, and the ball pitch from center to center is 1.00 millimeters.

Figure 2-3. M21131/M21151 (-22/-23/-24) Package Outline Top View and Cross Sectional View (in mm)

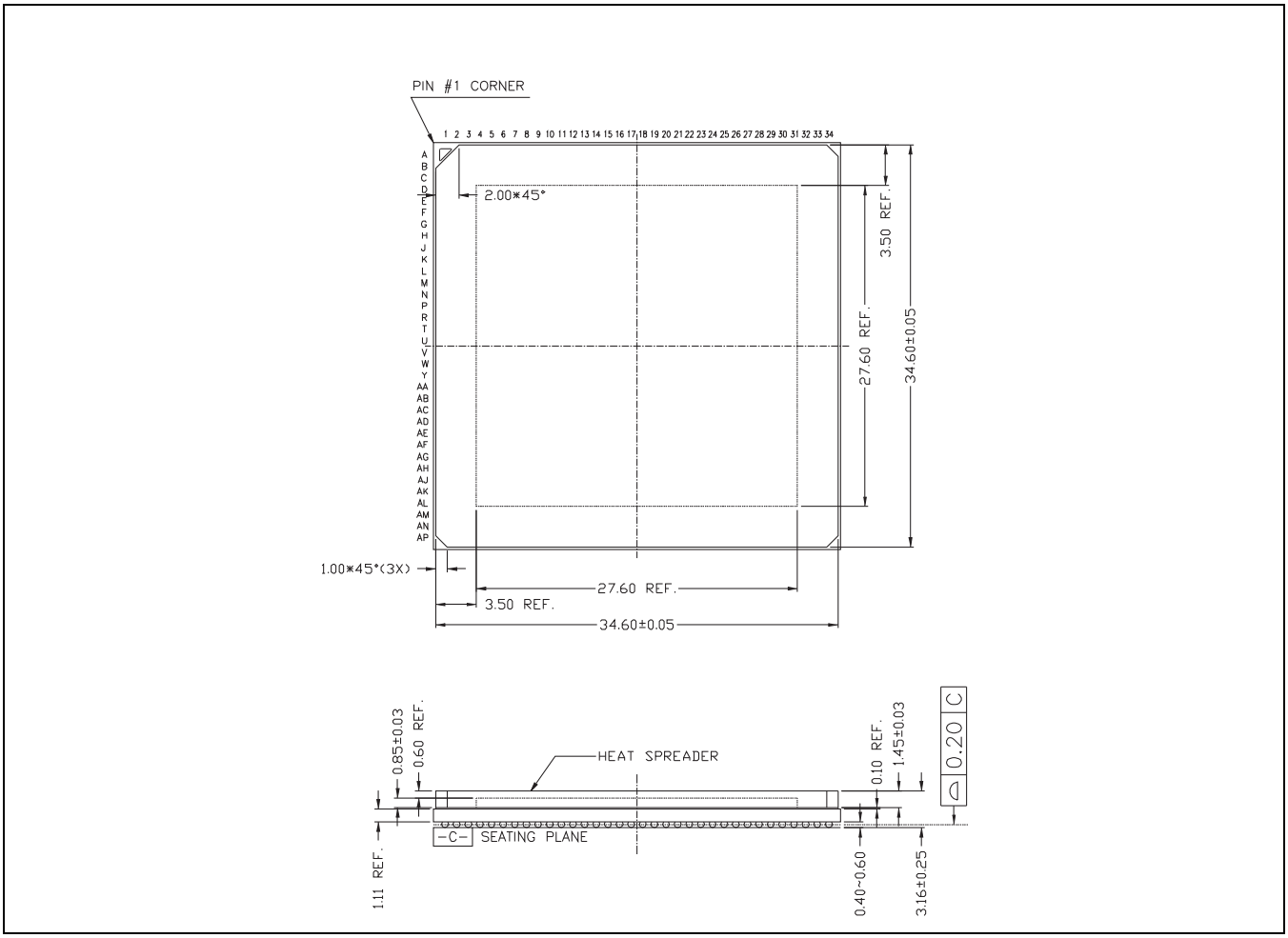
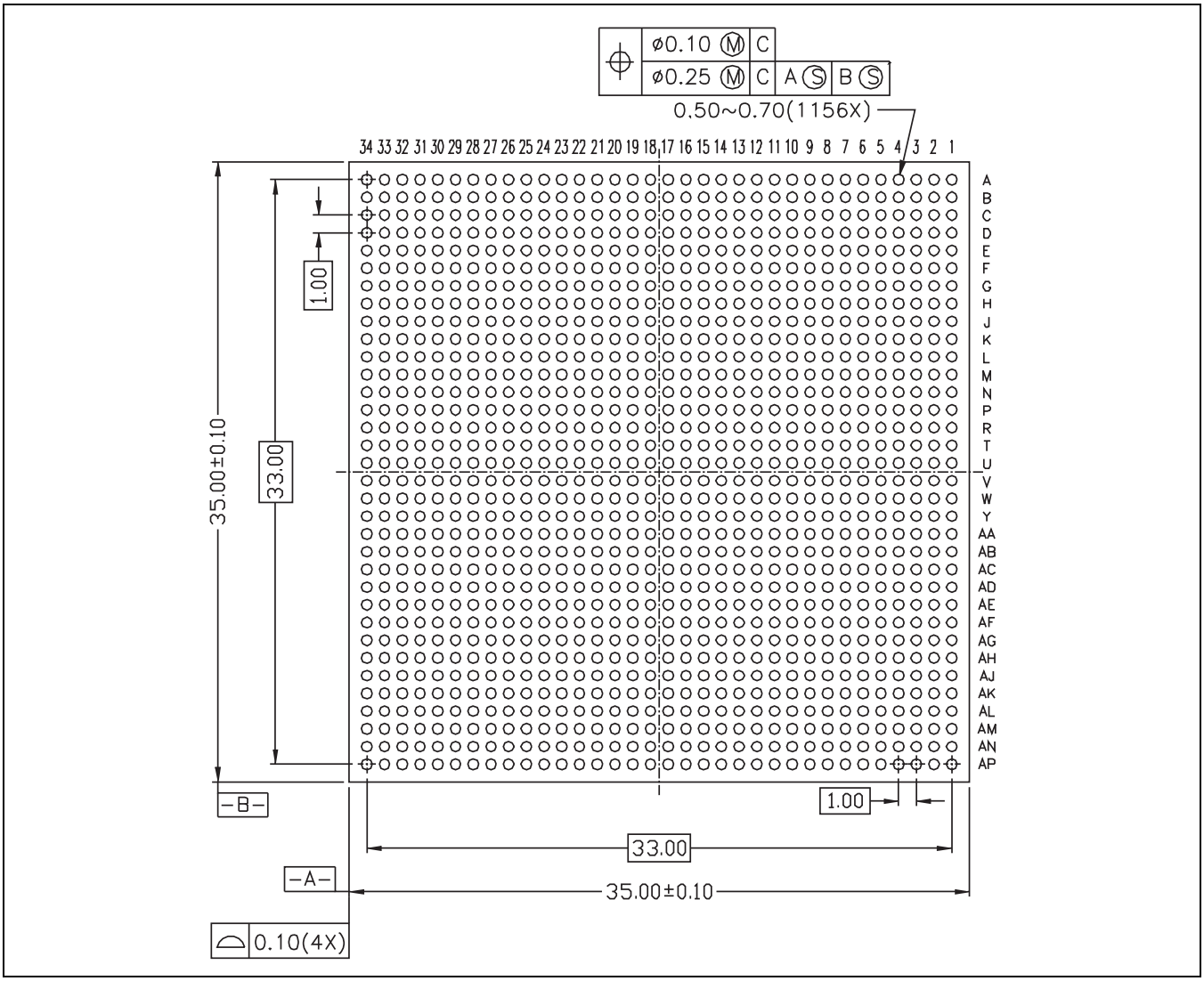


Figure 2-4. M21131/M21151 (-22/-23/-24) Bottom View of Package (in mm)



2.1.3 Package Changes

There are some differences between Ceramic and CPCore in package dimension and construction. They are listed below:

Table 2-1. Differences Between Ceramic and CPCore Packaging

Dimension	Differences		Units
	Ceramic	CPCore	
X dimension	35 +0.15/-0.20	35 +/-0.1	mm
Y dimension	35 +0.15/-0.20	35 +/-0.1	mm
Z dimension	3.85 +/-0.26	3.16 +/-0.25	mm
Coplanarity	0.15	0.20	mm

2.2 Pinout Diagram and Pin Descriptions

Table 2-2. BGA Assignments (1 of 8)

Note: For the M21131, the INP/N[72:143] and OUTP/N[72:143] pins are NC (No Connect).

Location	Name
A1	ADDR9
A2	DATA6
A3	XRST
A4	OUTP[134]
A5	OUTP[122]
A6	OUTP[138]
A7	OUTP[132]
A8	OUTP[126]
A9	OUTP[120]
A10	OUTP[114]
A11	OUTP[108]
A12	OUTP[102]
A13	OUTP[96]
A14	OUTP[90]
A15	OUTP[84]
A16	OUTP[78]
A17	OUTP[72]
A18	OUTP[66]
A19	OUTP[60]
A20	OUTP[54]
A21	OUTP[48]
A22	OUTP[42]
A23	OUTP[36]
A24	OUTP[30]
A25	OUTP[24]
A26	OUTP[18]
A27	OUTP[12]
A28	OUTP[6]
A29	OUTP[0]
A30	OUTP[20]
A31	OUTP[8]
A32	DIRXP[0]
A33	DOTXP[0]
A34	CLKTXREF[0]
B1	ADDR8
B2	DATA7

Location	Name
B3	R/XW
B4	OUTN[134]
B5	OUTN[122]
B6	OUTN[138]
B7	OUTN[132]
B8	OUTN[126]
B9	OUTN[120]
B10	OUTN[114]
B11	OUTN[108]
B12	OUTN[102]
B13	OUTN[96]
B14	OUTN[90]
B15	OUTN[84]
B16	OUTN[78]
B17	OUTN[72]
B18	OUTN[66]
B19	OUTN[60]
B20	OUTN[54]
B21	OUTN[48]
B22	OUTN[42]
B23	OUTN[36]
B24	OUTN[30]
B25	OUTN[24]
B26	OUTN[18]
B27	OUTN[12]
B28	OUTN[6]
B29	OUTN[0]
B30	OUTN[20]
B31	OUTN[8]
B32	DIRXN[0]
B33	DOTXN[0]
B34	TRIG[0]
C1	INP[7]
C2	INN[7]
C3	AVSS
C4	DATA5

Location	Name
C5	XCS
C6	XTEST
C7	AV_{SS}
C8	AV_{DD}_IO
C9	AV_{SS}
C10	AV_{DD}_IO
C11	AV_{SS}
C12	AV_{DD}_IO
C13	AV_{SS}
C14	AV_{DD}_IO
C15	AV_{SS}
C16	AV_{DD}_IO
C17	AV_{SS}
C18	AV_{DD}_IO
C19	AV_{SS}
C20	AV_{DD}_IO
C21	AV_{SS}
C22	AV_{DD}_IO
C23	AV_{SS}
C24	AV_{DD}_IO
C25	AV_{SS}
C26	AV_{DD}_IO
C27	AV_{SS}
C28	AV_{DD}_IO
C29	AV_{SS}
C30	MDSPDTEST[[3]
C31	MDSPDTEST[2]
C32	PERROR[0]
C33	INN[0]
C34	INP[0]
D1	INP[17]
D2	INN[17]
D3	XDS/SCLK
D4	ADDR7
D5	ADDR6
D6	DATA4

Location	Name
D7	OUTP[136]
D8	OUTP[140]
D9	OUTP[128]
D10	OUTP[116]
D11	OUTP[110]
D12	OUTP[104]
D13	OUTP[98]
D14	OUTP[92]
D15	OUTP[86]
D16	OUTP[80]
D17	OUTP[74]
D18	OUTP[68]
D19	OUTP[62]
D20	OUTP[56]
D21	OUTP[50]
D22	OUTP[44]
D23	OUTP[38]
D24	OUTP[32]
D25	OUTP[26]
D26	OUTP[14]
D27	OUTP[2]
D28	OUTP[34]
D29	OUTP[22]
D30	OUTP[10]
D31	XRSTRX[0]
D32	MDSPDTEST[1]
D33	INN[14]
D34	INP[14]
E1	INP[5]
E2	INN[5]
E3	ADDR5
E4	ADDR1
E5	ADDR4
E6	XSET
E7	OUTN[136]
E8	OUTN[140]

Table 2-2. BGA Assignments (2 of 8)

Location	Name	Location	Name	Location	Name	Location	Name
E9	OUTN[128]	F12	AV_{SS}	G15	OUTP[94]	H18	OUTN[76]
E10	OUTN[116]	F13	AV_{DD}_IO	G16	OUTP[88]	H19	OUTN[70]
E11	OUTN[110]	F14	AV_{SS}	G17	OUTP[82]	H20	OUTN[64]
E12	OUTN[104]	F15	AV_{DD}_IO	G18	OUTP[76]	H21	OUTN[58]
E13	OUTN[98]	F16	AV_{SS}	G19	OUTP[70]	H22	OUTN[52]
E14	OUTN[92]	F17	AV_{DD}_IO	G20	OUTP[64]	H23	OUTN[46]
E15	OUTN[86]	F18	AV_{SS}	G21	OUTP[58]	H24	OUTN[40]
E16	OUTN[80]	F19	AV_{DD}_IO	G22	OUTP[52]	H25	OUTN[28]
E17	OUTN[74]	F20	AV_{SS}	G23	OUTP[46]	H26	OUTN[16]
E18	OUTN[68]	F21	AV_{DD}_IO	G24	OUTP[40]	H27	OUTN[4]
E19	OUTN[62]	F22	AV_{SS}	G25	OUTP[28]	H28	CLKTXN[0]
E20	OUTN[56]	F23	AV_{DD}_IO	G26	OUTP[16]	H29	AV_{DD}_IO
E21	OUTN[50]	F24	AV_{SS}	G27	OUTP[4]	H30	INN[22]
E22	OUTN[44]	F25	AV_{DD}_IO	G28	CLKTXP[0]	H31	INP[22]
E23	OUTN[38]	F26	AV_{SS}	G29	AV_{SS}	H32	AV_{SS}
E24	OUTN[32]	F27	AV_{DD}_IO	G30	INN[16]	H33	INN[20]
E25	OUTN[26]	F28	AV_{SS}	G31	INP[16]	H34	INP[20]
E26	OUTN[14]	F29	AV_{DD}_IO	G32	AV_{DD}_IO	J1	INP[25]
E27	OUTN[2]	F30	INN[6]	G33	INN[12]	J2	INN[25]
E28	OUTN[34]	F31	INP[6]	G34	INP[12]	J3	AV_{SS}
E29	OUTN[22]	F32	AV_{SS}	H1	INP[21]	J4	INP[23]
E30	OUTN[10]	F33	INN[8]	H2	INN[21]	J5	INN[23]
E31	AV_{SS}	F34	INP[8]	H3	AV_{DD}_IO	J6	AV_{DD}_IO
E32	AV_{DD}_IO	G1	INP[13]	H4	INP[15]	J7	INP[3]
E33	INN[4]	G2	INN[13]	H5	INN[15]	J8	INN[3]
E34	INP[4]	G3	AV_{SS}	H6	DATA1	J9	AV_{SS}
F1	INP[9]	G4	INP[1]	H7	MDSPDTEST[5]	J10	MDSPDTEST[29]
F2	INN[9]	G5	INN[1]	H8	OUTN[142]	J11	AV_{SS}
F3	ADDR2	G6	XINDIS	H9	OUTN[130]	J12	AV_{DD}_IO
F4	XOUTDIS	G7	MDSPDTEST[4]	H10	OUTN[124]	J13	AV_{DD}_IO
F5	ADDR0	G8	OUTP[142]	H11	OUTN[118]	J14	AV_{DD}_CORE
F6	ADDR3	G9	OUTP[130]	H12	OUTN[112]	J15	AV_{DD}_CORE
F7	DATA2	G10	OUTP[124]	H13	OUTN[106]	J16	AV_{DD}_IO
F8	MDSPDTEST[28]	G11	OUTP[118]	H14	OUTN[100]	J17	AV_{DD}_IO
F9	AV_{DD}_IO	G12	OUTP[112]	H15	OUTN[94]	J18	AV_{DD}_CORE
F10	AV_{SS}	G13	OUTP[106]	H16	OUTN[88]	J19	AV_{DD}_CORE
F11	AV_{DD}_IO	G14	OUTP[100]	H17	OUTN[82]	J20	AV_{DD}_IO

Table 2-2. BGA Assignments (3 of 8)

Location	Name	Location	Name	Location	Name	Location	Name
J21	AV_{DD}_IO	K24	MDSPDTEST[32]	L27	INN[18]	M30	INN[46]
J22	AV_{DD}_CORE	K25	XENRX[0]	L28	INP[18]	M31	INP[46]
J23	AV_{DD}_CORE	K26	AV_{DD}_IO	L29	AV_{SS}	M32	AV_{SS}
J24	AV_{SS}	K27	INN[10]	L30	INN[38]	M33	INN[40]
J25	AV_{DD}_IO	K28	INP[10]	L31	INP[38]	M34	INP[40]
J26	AV_{SS}	K29	AV_{DD}_IO	L32	AV_{DD}_IO	N1	INP[45]
J27	INN[2]	K30	INN[32]	L33	INN[36]	N2	INN[45]
J28	INP[2]	K31	INP[32]	L34	INP[36]	N3	AV_{SS}
J29	AV_{SS}	K32	AV_{SS}	M1	INP[41]	N4	INP[47]
J30	INN[30]	K33	INN[28]	M2	INN[41]	N5	INN[47]
J31	INP[30]	K34	INP[28]	M3	AV_{DD}_IO	N6	AV_{DD}_IO
J32	AV_{DD}_IO	L1	INP[37]	M4	INP[39]	N7	INP[35]
J33	INN[24]	L2	INN[37]	M5	INN[39]	N8	INN[35]
J34	INP[24]	L3	AV_{SS}	M6	AV_{SS}	N9	AV_{DD}_CORE
K1	INP[29]	L4	INP[33]	M7	INP[27]	N10	AV_{SS}
K2	INN[29]	L5	INN[33]	M8	INN[27]	N11	AV_{SS}
K3	AV_{DD}_IO	L6	AV_{DD}_IO	M9	AV_{DD}_CORE	N12	AV_{DD}_IO
K4	INP[31]	L7	INP[19]	M10	DV_{DD}_IO	N13	AV_{DD}_IO
K5	INN[31]	L8	INN[19]	M11	AV_{SS}	N14	AV_{SS}
K6	AV_{SS}	L9	DV_{SS}_IO	M12	AV_{DD}_IO	N15	AV_{SS}
K7	INP[11]	L10	LOS	M13	AV_{DD}_IO	N16	AV_{DD}_CORE
K8	INN[11]	L11	DATA0	M14	AV_{SS}	N17	AV_{DD}_CORE
K9	N/C	L12	AV_{SS}	M15	AV_{SS}	N18	AV_{DD}_CORE
K10	SER/XPAR	L13	AV_{SS}	M16	AV_{DD}_CORE	N19	AV_{DD}_CORE
K11	DATA3	L14	AV_{SS}	M17	AV_{DD}_CORE	N20	AV_{SS}
K12	AV_{SS}	L15	AV_{SS}	M18	AV_{DD}_CORE	N21	AV_{SS}
K13	AV_{SS}	L16	AV_{SS}	M19	AV_{DD}_CORE	N22	AV_{DD}_IO
K14	AV_{SS}	L17	AV_{SS}	M20	AV_{SS}	N23	AV_{DD}_IO
K15	AV_{SS}	L18	AV_{SS}	M21	AV_{SS}	N24	AV_{SS}
K16	AV_{SS}	L19	AV_{SS}	M22	AV_{DD}_IO	N25	AV_{SS}
K17	AV_{SS}	L20	AV_{SS}	M23	AV_{DD}_IO	N26	AV_{DD}_CORE
K18	AV_{SS}	L21	AV_{SS}	M24	AV_{SS}	N27	INN[34]
K19	AV_{SS}	L22	AV_{SS}	M25	AV_{SS}	N28	INP[34]
K20	AV_{SS}	L23	AV_{SS}	M26	AV_{DD}_CORE	N29	AV_{SS}
K21	AV_{SS}	L24	MDSPDTEST[33]	M27	INN[26]	N30	INN[48]
K22	AV_{SS}	L25	XENTX[0]	M28	INP[26]	N31	INP[48]
K23	AV_{SS}	L26	AV_{SS}	M29	AV_{DD}_IO	N32	AV_{DD}_IO

Table 2-2. BGA Assignments (4 of 8)

Location	Name
N33	INN[44]
N34	INP[44]
P1	INP[53]
P2	INN[53]
P3	AV_{DD}_IO
P4	INP[49]
P5	INN[49]
P6	AV_{SS}
P7	INP[43]
P8	INN[43]
P9	AV_{DD}_IO
P10	AV_{SS}
P11	AV_{SS}
P12	AV_{DD}_IO
P13	AV_{DD}_IO
P14	AV_{SS}
P15	AV_{SS}
P16	AV_{DD}_CORE
P17	AV_{DD}_CORE
P18	AV_{DD}_CORE
P19	AV_{DD}_CORE
P20	AV_{SS}
P21	AV_{SS}
P22	AV_{DD}_IO
P23	AV_{DD}_IO
P24	AV_{SS}
P25	AV_{SS}
P26	AV_{DD}_IO
P27	INN[42]
P28	INP[42]
P29	AV_{DD}_IO
P30	INN[54]
P31	INP[54]
P32	AV_{SS}
P33	INN[52]
P34	INP[52]
R1	INP[57]

Location	Name
R2	INN[57]
R3	AV_{SS}
R4	INP[55]
R5	INN[55]
R6	AV_{DD}_IO
R7	INP[51]
R8	INN[51]
R9	AV_{DD}_IO
R10	AV_{SS}
R11	AV_{SS}
R12	AV_{DD}_IO
R13	AV_{DD}_IO
R14	AV_{SS}
R15	AV_{SS}
R16	AV_{DD}_CORE
R17	AV_{DD}_CORE
R18	AV_{DD}_CORE
R19	AV_{DD}_CORE
R20	AV_{SS}
R21	AV_{SS}
R22	AV_{DD}_IO
R23	AV_{DD}_IO
R24	AV_{SS}
R25	AV_{SS}
R26	AV_{DD}_IO
R27	INN[50]
R28	INP[50]
R29	AV_{SS}
R30	INN[62]
R31	INP[62]
R32	AV_{DD}_IO
R33	INN[56]
R34	INP[56]
T1	INP[61]
T2	INN[61]
T3	AV_{DD}_IO
T4	INP[63]

Location	Name
T5	INN[63]
T6	AV_{SS}
T7	INP[59]
T8	INN[59]
T9	AV_{DD}_CORE
T10	AV_{SS}
T11	AV_{SS}
T12	AV_{DD}_IO
T13	AV_{DD}_IO
T14	AV_{SS}
T15	AV_{SS}
T16	AV_{DD}_CORE
T17	AV_{DD}_CORE
T18	AV_{DD}_CORE
T19	AV_{DD}_CORE
T20	AV_{SS}
T21	AV_{SS}
T22	AV_{DD}_IO
T23	AV_{DD}_IO
T24	AV_{SS}
T25	AV_{SS}
T26	AV_{DD}_CORE
T27	INN[58]
T28	INP[58]
T29	AV_{DD}_IO
T30	INN[64]
T31	INP[64]
T32	AV_{SS}
T33	INN[60]
T34	INP[60]
U1	INP[69]
U2	INN[69]
U3	AV_{SS}
U4	INP[65]
U5	INN[65]
U6	AV_{DD}_IO
U7	INP[67]

Location	Name
U8	INN[67]
U9	AV_{DD}_CORE
U10	AV_{SS}
U11	AV_{SS}
U12	AV_{DD}_IO
U13	AV_{DD}_IO
U14	AV_{SS}
U15	AV_{SS}
U16	AV_{DD}_CORE
U17	AV_{DD}_CORE
U18	AV_{DD}_CORE
U19	AV_{DD}_CORE
U20	AV_{SS}
U21	AV_{SS}
U22	AV_{DD}_IO
U23	AV_{DD}_IO
U24	AV_{SS}
U25	AV_{SS}
U26	AV_{DD}_CORE
U27	INN[66]
U28	INP[66]
U29	AV_{SS}
U30	INN[70]
U31	INP[70]
U32	AV_{DD}_IO
U33	INN[68]
U34	INP[68]
V1	INP[73]
V2	INN[73]
V3	AV_{DD}_IO
V4	INP[71]
V5	INN[71]
V6	AV_{SS}
V7	INP[75]
V8	INN[75]
V9	AV_{DD}_IO
V10	AV_{SS}

Table 2-2. BGA Assignments (5 of 8)

Location	Name	Location	Name	Location	Name	Location	Name
V11	AV_{SS}	W14	AV_{SS}	Y17	AV_{DD}_CORE	AA20	AV_{SS}
V12	AV_{DD}_IO	W15	AV_{SS}	Y18	AV_{DD}_CORE	AA21	AV_{SS}
V13	AV_{DD}_IO	W16	AV_{DD}CORE	Y19	AV_{DD}_CORE	AA22	AV_{DD}_IO
V14	AV_{SS}	W17	AV_{DD}_CORE	Y20	AV_{SS}	AA23	AV_{DD}_IO
V15	AV_{SS}	W18	AV_{DD}_CORE	Y21	AV_{SS}	AA24	AV_{SS}
V16	AV_{DD}_CORE	W19	AV_{DD}_CORE	Y22	AV_{DD}_IO	AA25	AV_{SS}
V17	AV_{DD}_CORE	W20	AV_{SS}	Y23	AV_{DD}_IO	AA26	AV_{DD}_CORE
V18	AV_{DD}_CORE	W21	AV_{SS}	Y24	AV_{SS}	AA27	INN[98]
V19	AV_{DD}_CORE	W22	AV_{DD}_IO	Y25	AV_{SS}	AA28	INP[98]
V20	AV_{SS}	W23	AV_{DD}_IO	Y26	AV_{DD}_CORE	AA29	AV_{SS}
V21	AV_{SS}	W24	AV_{SS}	Y27	INN[90]	AA30	INN[94]
V22	AV_{DD}_IO	W25	AV_{SS}	Y28	INP[90]	AA31	INP[94]
V23	AV_{DD}_IO	W26	AV_{DD}_IO	Y29	AV_{DD}_IO	AA32	AV_{DD}_IO
V24	AV_{SS}	W27	INN[82]	Y30	INN[86]	AA33	INN[88]
V25	AV_{SS}	W28	INP[82]	Y31	INP[86]	AA34	INP[88]
V26	AV_{DD}_IO	W29	AV_{SS}	Y32	AV_{SS}	AB1	INP[93]
V27	INN[74]	W30	INN[80]	Y33	INN[84]	AB2	INN[93]
V28	INP[74]	W31	INP[80]	Y34	INP[84]	AB3	AV_{DD}_IO
V29	AV_{DD}_IO	W32	AV_{DD}_IO	AA1	INP[89]	AB4	INP[95]
V30	INN[78]	W33	INN[76]	AA2	INN[89]	AB5	INN[95]
V31	INP[78]	W34	INP[76]	AA3	AV_{SS}	AB6	AV_{SS}
V32	AV_{SS}	Y1	INP[85]	AA4	INP[87]	AB7	INP[107]
V33	INN[72]	Y2	INN[85]	AA5	INN[87]	AB8	INN[107]
V34	INP[72]	Y3	AV_{DD}_IO	AA6	AV_{DD}_IO	AB9	AV_{DD}_IO
W1	INP[77]	Y4	INP[81]	AA7	INP[99]	AB10	AV_{SS}
W2	INN[77]	Y5	INN[81]	AA8	INN[99]	AB11	AV_{SS}
W3	AV_{SS}	Y6	AV_{SS}	AA9	AV_{DD}_CORE	AB12	AV_{DD}_IO
W4	INP[79]	Y7	INP[91]	AA10	AV_{SS}	AB13	AV_{DD}_IO
W5	INN[79]	Y8	INN[91]	AA11	AV_{SS}	AB14	AV_{SS}
W6	AV_{DD}_IO	Y9	AV_{DD}_CORE	AA12	AV_{DD}_IO	AB15	AV_{SS}
W7	INP[83]	Y10	AV_{SS}	AA13	AV_{DD}_IO	AB16	AV_{DD}_CORE
W8	INN[83]	Y11	AV_{SS}	AA14	AV_{SS}	AB17	AV_{DD}_CORE
W9	AV_{DD}_IO	Y12	AV_{DD}_IO	AA15	AV_{SS}	AB18	AV_{DD}_CORE
W10	AV_{SS}	Y13	AV_{DD}_IO	AA16	AV_{DD}_CORE	AB19	AV_{DD}_CORE
W11	AV_{SS}	Y14	AV_{SS}	AA17	AV_{DD}_CORE	AB20	AV_{SS}
W12	AV_{DD}_IO	Y15	AV_{SS}	AA18	AV_{DD}_CORE	AB21	AV_{SS}
W13	AV_{DD}_IO	Y16	AV_{DD}_CORE	AA19	AV_{DD}_CORE	AB22	AV_{DD}_IO

Table 2-2. BGA Assignments (6 of 8)

Location	Name
AB23	AV_{DD}_IO
AB24	AV_{SS}
AB25	AV_{SS}
AB26	AV_{DD}_IO
AB27	INN[106]
AB28	INP[106]
AB29	AV_{DD}_IO
AB30	INN[96]
AB31	INP[96]
AB32	AV_{SS}
AB33	INN[92]
AB34	INP[92]
AC1	INP[101]
AC2	INN[101]
AC3	AV_{SS}
AC4	INP[97]
AC5	INN[97]
AC6	AV_{DD}_IO
AC7	INP[115]
AC8	INN[115]
AC9	AV_{DD}_IO
AC10	AV_{SS}
AC11	AV_{SS}
AC12	AV_{DD}_IO
AC13	AV_{DD}_IO
AC14	AV_{SS}
AC15	AV_{SS}
AC16	AV_{DD}_CORE
AC17	AV_{DD}_CORE
AC18	AV_{DD}_CORE
AC19	AV_{DD}_CORE
AC20	AV_{SS}
AC21	AV_{SS}
AC22	AV_{DD}_IO
AC23	AV_{DD}_IO
AC24	AV_{SS}
AC25	AV_{SS}

Location	Name
AC26	AV_{DD}_IO
AC27	INN[114]
AC28	INP[114]
AC29	AV_{SS}
AC30	INN[102]
AC31	INP[102]
AC32	AV_{DD}_IO
AC33	INN[100]
AC34	INP[100]
AD1	INP[105]
AD2	INN[105]
AD3	AV_{DD}_IO
AD4	INP[103]
AD5	INN[103]
AD6	AV_{SS}
AD7	INP[123]
AD8	INN[123]
AD9	AV_{SS}
AD10	PERROR[1]
AD11	MDSPDTEST[31]
AD12	AV_{SS}
AD13	AV_{SS}
AD14	AV_{SS}
AD15	AV_{SS}
AD16	AV_{SS}
AD17	AV_{SS}
AD18	AV_{SS}
AD19	AV_{SS}
AD20	AV_{SS}
AD21	AV_{SS}
AD22	AV_{SS}
AD23	AV_{SS}
AD24	AV_{SS}
AD25	AV_{SS}
AD26	AV_{DD}_IO
AD27	INN[122]
AD28	INP[122]

Location	Name
AD29	AV_{DD}_IO
AD30	INN[110]
AD31	INP[110]
AD32	AV_{SS}
AD33	INN[104]
AD34	INP[104]
AE1	INP[109]
AE2	INN[109]
AE3	AV_{SS}
AE4	INP[111]
AE5	INN[111]
AE6	AV_{DD}_IO
AE7	INP[131]
AE8	INN[131]
AE9	AV_{DD}_IO
AE10	TRIG[1]
AE11	MDSPDTEST[30]
AE12	AV_{SS}
AE13	AV_{SS}
AE14	AV_{SS}
AE15	AV_{SS}
AE16	AV_{SS}
AE17	AV_{SS}
AE18	AV_{SS}
AE19	AV_{SS}
AE20	AV_{SS}
AE21	AV_{SS}
AE22	AV_{SS}
AE23	AV_{SS}
AE24	AV_{SS}
AE25	AV_{SS}
AE26	MDSPDTEST[11]
AE27	INN[130]
AE28	INP[130]
AE29	AV_{SS}
AE30	INN[112]
AE31	INP[112]

Location	Name
AE32	AV_{DD}_IO
AE33	INN[108]
AE34	INP[108]
AF1	INP[117]
AF2	INN[117]
AF3	AV_{DD}_IO
AF4	INP[113]
AF5	INN[113]
AF6	AV_{SS}
AF7	INP[139]
AF8	INN[139]
AF9	AV_{SS}
AF10	AV_{DD}_IO
AF11	AV_{SS}
AF12	AV_{DD}_IO
AF13	AV_{DD}_IO
AF14	AV_{DD}_CORE
AF15	AV_{DD}_CORE
AF16	AV_{DD}_IO
AF17	AV_{DD}_IO
AF18	AV_{DD}_CORE
AF19	AV_{DD}_CORE
AF20	AV_{DD}_IO
AF21	AV_{DD}_IO
AF22	AV_{DD}_CORE
AF23	AV_{DD}_CORE
AF24	AV_{DD}_IO
AF25	AVDD_IO
AF26	MDSPDTEST[12]
AF27	INN[138]
AF28	INP[138]
AF29	AV_{DD}_IO
AF30	INN[118]
AF31	INP[118]
AF32	AV_{SS}
AF33	INN[116]
AF34	INP[116]

Table 2-2. BGA Assignments (7 of 8)

Location	Name
AG1	INP[121]
AG2	INN[121]
AG3	AV_{SS}
AG4	INP[119]
AG5	INN[119]
AG6	AV_{DD}_IO
AG7	CLKTXN[1]
AG8	OUTN[143]
AG9	OUTN[131]
AG10	OUTN[119]
AG11	OUTN[113]
AG12	OUTN[107]
AG13	OUTN[101]
AG14	OUTN[95]
AG15	OUTN[89]
AG16	OUTN[83]
AG17	OUTN[77]
AG18	OUTN[71]
AG19	OUTN[65]
AG20	OUTN[59]
AG21	OUTN[53]
AG22	OUTN[47]
AG23	OUTN[41]
AG24	OUTN[35]
AG25	OUTN[23]
AG26	OUTN[11]
AG27	OUTN[5]
AG28	MDSPDTEST[17]
AG29	AV_{SS}
AG30	INN[126]
AG31	INP[126]
AG32	AV_{DD}_IO
AG33	INN[120]
AG34	INP[120]
AH1	INP[125]
AH2	INN[125]
AH3	AV_{DD}_IO

Location	Name
AH4	INP[127]
AH5	INN[127]
AH6	AV_{SS}
AH7	CLKTXP[1]
AH8	OUTP[143]
AH9	OUTP[131]
AH10	OUTP[119]
AH11	OUTP[113]
AH12	OUTP[107]
AH13	OUTP[101]
AH14	OUTP[95]
AH15	OUTP[89]
AH16	OUTP[83]
AH17	OUTP[77]
AH18	OUTP[71]
AH19	OUTP[65]
AH20	OUTP[59]
AH21	OUTP[53]
AH22	OUTP[47]
AH23	OUTP[41]
AH24	OUTP[35]
AH25	OUTP[23]
AH26	OUTP[11]
AH27	OUTP[5]
AH28	MDSPDTEST[18]
AH29	MDSPDTEST[23]
AH30	INN[128]
AH31	INP[128]
AH32	AV_{SS}
AH33	INN[124]
AH34	INP[124]
AJ1	INP[133]
AJ2	INN[133]
AJ3	AV_{SS}
AJ4	INP[135]
AJ5	INN[135]
AJ6	AV_{DD}_IO

Location	Name
AJ7	AV_{SS}
AJ8	AV_{DD}_IO
AJ9	AV_{SS}
AJ10	AV_{DD}_IO
AJ11	AV_{SS}
AJ12	AV_{DD}_IO
AJ13	AV_{SS}
AJ14	AV_{DD}_IO
AJ15	AV_{SS}
AJ16	AV_{DD}_IO
AJ17	AV_{SS}
AJ18	AV_{DD}_IO
AJ19	AV_{SS}
AJ20	AV_{DD}_IO
AJ21	AV_{SS}
AJ22	AV_{DD}_IO
AJ23	AV_{SS}
AJ24	AV_{DD}_IO
AJ25	AV_{SS}
AJ26	AV_{DD}_IO
AJ27	AV_{SS}
AJ28	AV_{DD}_IO
AJ29	MDSPDTEST[24]
AJ30	INN[142]
AJ31	INP[142]
AJ32	AV_{DD}_IO
AJ33	INN[132]
AJ34	INP[132]
AK1	INP[137]
AK2	INN[137]
AK3	XRSTRX[1]
AK4	INP[143]
AK5	INN[143]
AK6	OUTN[137]
AK7	OUTN[125]
AK8	OUTN[141]
AK9	OUTN[129]

Location	Name
AK10	OUTN[117]
AK11	OUTN[111]
AK12	OUTN[105]
AK13	OUTN[99]
AK14	OUTN[93]
AK15	OUTN[87]
AK16	OUTN[81]
AK17	OUTN[75]
AK18	OUTN[69]
AK19	OUTN[63]
AK20	OUTN[57]
AK21	OUTN[51]
AK22	OUTN[45]
AK23	OUTN[39]
AK24	OUTN[33]
AK25	OUTN[27]
AK26	OUTN[15]
AK27	OUTN[3]
AK28	OUTN[29]
AK29	OUTN[17]
AK30	MDSPDTEST[21]
AK31	MDSPDTEST[9]
AK32	MDSPDTEST[6]
AK33	INN[136]
AK34	INP[136]
AL1	INP[141]
AL2	INN[141]
AL3	MDSPDTEST[27]
AL4	XENRX[1]
AL5	MDSPDTEST[25]
AL6	OUTP[137]
AL7	OUTP[125]
AL8	OUTP[141]
AL9	OUTP[129]
AL10	OUTP[117]
AL11	OUTP[111]
AL12	OUTP[105]

Table 2-2. BGA Assignments (8 of 8)

Location	Name	Location	Name	Location	Name	Location	Name
AL13	OUTP[99]	AM10	AV_{SS}	AN7	OUTN[127]	AP4	OUTP[123]
AL14	OUTP[93]	AM11	AV_{DD}_IO	AN8	OUTN[121]	AP5	OUTP[139]
AL15	OUTP[87]	AM12	AV_{SS}	AN9	OUTN[115]	AP6	OUTP[133]
AL16	OUTP[81]	AM13	AV_{DD}_IO	AN10	OUTN[109]	AP7	OUTP[127]
AL17	OUTP[75]	AM14	AV_{SS}	AN11	OUTN[103]	AP8	OUTP[121]
AL18	OUTP[69]	AM15	AV_{DD}_IO	AN12	OUTN[97]	AP9	OUTP[115]
AL19	OUTP[63]	AM16	AV_{SS}	AN13	OUTN[91]	AP10	OUTP[109]
AL20	OUTP[57]	AM17	AV_{DD}_IO	AN14	OUTN[85]	AP11	OUTP[103]
AL21	OUTP[51]	AM18	AV_{SS}	AN15	OUTN[79]	AP12	OUTP[97]
AL22	OUTP[45]	AM19	AV_{DD}_IO	AN16	OUTN[73]	AP13	OUTP[91]
AL23	OUTP[39]	AM20	AV_{SS}	AN17	OUTN[67]	AP14	OUTP[85]
AL24	OUTP[33]	AM21	AV_{DD}_IO	AN18	OUTN[61]	AP15	OUTP[79]
AL25	OUTP[27]	AM22	AV_{SS}	AN19	OUTN[55]	AP16	OUTP[73]
AL26	OUTP[15]	AM23	AV_{DD}_IO	AN20	OUTN[49]	AP17	OUTP[67]
AL27	OUTP[3]	AM24	AV_{SS}	AN21	OUTN[43]	AP18	OUTP[61]
AL28	OUTP[29]	AM25	AV_{DD}_IO	AN22	OUTN[37]	AP19	OUTP[55]
AL29	OUTP[17]	AM26	AV_{SS}	AN23	OUTN[31]	AP20	OUTP[49]
AL30	MDSPDTEST[22]	AM27	AV_{DD}_IO	AN24	OUTN[25]	AP21	OUTP[43]
AL31	MDSPDTEST[8]	AM28	AV_{SS}	AN25	OUTN[19]	AP22	OUTP[37]
AL32	MDSPDTEST[7]	AM29	AV_{DD}_IO	AN26	OUTN[13]	AP23	OUTP[31]
AL33	INN[140]	AM30	AV_{SS}	AN27	OUTN[7]	AP24	OUTP[25]
AL34	INP[140]	AM31	MDSPDTEST[19]	AN28	OUTN[1]	AP25	OUTP[19]
AM1	INP[129]	AM32	MDSPDTEST[10]	AN29	OUTN[21]	AP26	OUTP[13]
AM2	INN[129]	AM33	INN[134]	AN30	OUTN[9]	AP27	OUTP[7]
AM3	CLKTXREF[1]	AM34	INP[134]	AN31	MDSPDTEST[20]	AP28	OUTP[1]
AM4	XENTX[1]	AN1	DOTXN[1]	AN32	AV_{DD}_IO	AP29	OUTP[21]
AM5	MDSPDTEST[26]	AN2	DIRXN[1]	AN33	N/C	AP30	OUTP[9]
AM6	AVSS	AN3	OUTN[135]	AN34	MDSPDTEST[13]	AP31	MDSPDTEST[16]
AM7	AV_{DD}_IO	AN4	OUTN[123]	AP1	DOTXP[1]	AP32	MDSPDTEST[15]
AM8	AV_{SS}	AN5	OUTN[139]	AP2	DIRXP[1]	AP33	RXREFCLK
AM9	AV_{DD}_IO	AN6	OUTN[133]	AP3	OUTP[135]	AP34	MDSPDTEST[14]

Table 2-3. Digital Power Connections

Location	Connection
L9	DV_{SS}_IO
M10	DV_{DD}_IO

Table 2-4. BGA Connections to AV_{DD}_IO

Ball Location											
AA12	AC9	AF12	AJ12	AM17	C22	F29	K3	P3	R32	V12	Y12
AA13	AC12	AF13	AJ14	AM19	C24	G32	L6	P9	T3	V13	Y13
AA22	AC13	AF16	AJ16	AM21	C26	H3	L32	P12	T12	V22	Y22
AA23	AC22	AF17	AJ18	AM23	C28	H29	M12	P13	T13	V23	Y23
AA32	AC23	AF20	AJ20	AM25	E32	J6	M13	P22	T22	V26	Y29
AA6	AC26	AF21	AJ22	AM27	F09	J12	M22	P23	T23	V29	—
AB3	AC32	AF24	AJ24	AM29	F11	J13	M23	P26	T29	W6	—
AB9	AD03	AF25	AJ26	AN32	F13	J16	M29	P29	U6	W9	—
AB12	AD26	AF29	AJ28	C8	F15	J17	M3	R6	U12	W12	—
AB13	AD29	AG06	AJ32	C10	F17	J20	N6	R9	U13	W13	—
AB22	AE6	AG32	AM07	C12	F19	J21	N12	R12	U22	W22	—
AB23	AE9	AH3	AM9	C14	F21	J25	N13	R13	U23	W23	—
AB26	AE32	AJ6	AM11	C16	F23	J32	N22	R22	U32	W26	—
AB29	AF3	AJ8	AM13	C18	F25	K26	N23	R23	V3	W32	—
AC6	AF10	AJ10	AM15	C20	F27	K29	N32	R26	V9	Y3	—

Table 2-5. BGA Connections to AV_{DD}_CORE

Ball Locations					
AA9	AC18	J22	N19	T17	V18
AA16	AC19	J23	N26	T18	V19
AA17	AF14	M9	P16	T19	W16
AA18	AF15	M16	P17	T26	W17
AA19	AF18	M17	P18	U9	W18
AA26	AF19	M18	P19	U16	W19
AB16	AF22	M19	R16	U17	Y9
AB17	AF23	M26	R17	U18	Y16
AB18	J14	N9	R18	U19	Y17
AB19	J15	N16	R19	U26	Y18
AC16	J18	N17	T9	V16	Y19
AC17	J19	N18	T16	V17	Y26

2.3 Pin Definitions

Table 2-6. Power Pins

Pin Name	Function	Type
AV_{DD}_IO	Analog I/O positive supply	Power
AV_{DD}_CORE	Analog core positive supply	Power
AV_{SS}	Device ground	Power
DV_{DD}_IO	Digital I/O positive supply	Power
DV_{SS}_IO	Digital I/O negative supply	Power

Table 2-7. High-Speed Signal Pins (1 of 2)

Pin Name	Function	Termination	Type
INP[71:0] / INP[143:0]	Positive differential input data	50Ω internal pull-up to AV_{DD}_IO	Input/PCML
INN[71:0] / INN[143:0]	Negative differential input data	50Ω internal pull-up to AV_{DD}_IO	Input/PCML
OUTP[71:0] / OUTP[143:0]	Positive differential output data	50Ω internal pull-up to AV_{DD}_IO	Output/PCML
OUTN[71:0] / OUTN[143:0]	Negative differential output data	50Ω internal pull-up to AV_{DD}_IO	Output/PCML
XINDIS	Hardware disable of all inputs (active low)	100 kΩ internal pull-down	Input/CMOS
XOUTDIS	Hardware disable of all outputs (active low)	100 kΩ internal pull-down	Input/CMOS
A[9:0]	10 bit parallel address (bit 9: MSB, bit 0: LSB)	100 kΩ internal pull-up	Input/CMOS
D[5:0]	6 low bits of 8 bit parallel data (bit 0: LSB)	100 kΩ internal pull-up	I/O/CMOS
D[6]/SDI	7th bit of parallel data or serial data input	100 kΩ internal pull-up	I/O/CMOS
D[7]/SDO	8th bit of parallel data (MSB) or serial data output	100 kΩ internal pull-up	I/O/CMOS
DOTXP[1:0]	Positive differential output of 2^{23}-1 PRBS signal generator	50Ω internal pull-up to AV_{DD}_IO	Output/PCML
DOTXN[1:0]	Negative differential output of 2^{23}-1 PRBS signal generator	50Ω internal pull-up to AV_{DD}_IO	Output/PCML
CLKTXP[1:0]	Positive differential clock for 2^{23}-1 PRBS signal generator	50Ω internal pull-up to AV_{DD}_IO	Input/PCML
CLKTXN[1:0]	Negative differential clock for 2^{23}-1 PRBS signal generator	50Ω internal pull-up to AV_{DD}_IO	Input/PCML
CLKTXREF[1:0]	Low speed reference clock for 2^{23}-1 PRBS signal generator	(2, 3)	Input/CMOS
RXREFCLK	19.44 MHz clock reference for LOS detection	(2, 3)	Input/CMOS
XENTX[1:0]	Enable (active low) 2^{23}-1 PRBS signal generator clock	100 kΩ internal pull-up to AV_{DD}_IO	Input/CMOS
DIRXP[1:0]	Positive differential data for 2^{23}-1 PRBS signal receiver	50Ω internal pull-up to AV_{DD}_IO	Input/PCML
DIRXN[1:0]	Negative differential data for 2^{23}-1 PRBS signal receiver	50Ω internal pull-up to AV_{DD}_IO	Input/PCML
XENRX[1:0]	Enable (active low) 2^{23}-1 pseudorandom RX clock/data	100 kΩ internal pull-up to AV_{DD}_IO	Input/CMOS

Table 2-7. High-Speed Signal Pins (2 of 2)

Pin Name	Function	Termination	Type
XRSTRX[1:0]	Reset (active low) 2^{23}-1 pseudorandom RX clock/data	100 kΩ internal pull-up to AV_{DD}_IO	Input/CMOS
PERROR[1:0]	PRBS receiver bit error flag: latches High on first error (cleared on PRBS reset)	100 kΩ internal pull-up	Output/CMOS

NOTES:

1. In PRBS mode a portion of the PRBS signal will egress from the input terminal to which the PRBS transmitter is connected. The device normally connected to these terminals might need to be powered down or temporarily disconnected during PRBS operation; alternatively, any unused input can be used to route the PRBS signal to any output.
2. 100 kΩ internal pull-ups on all CMOS inputs, unless noted as pull-downs.
3. RXREFCLK and CLKTXREF[1:0] are CMOS inputs that are referenced to AV_{DD}_IO.

Table 2-8. Control, Interface, and Alarm Pins

Pin Name	Function	Termination	Type
R/XW	Parallel I/0: H = read, L = write	(1)	Input/CMOS
XDS/SCLK	Parallel I/0: data latch, serial I/0: serial clock (hysteresis)	(1)	Input/CMOS
XCS	Serial/parallel: active low I/O enable	(1)	Input/CMOS
SER/XPAR	Serial/parallel I/O select: H = serial, L = parallel	(1)	Input/CMOS
XRST	Hardware reset (active low)	(1)	Input/CMOS
XTEST	Mindspeed test terminal (active low)	(1)	Input/CMOS
XSET	Hardware xSet terminal enables switching multiple channel configurations simultaneously (active low)	(1)	Input/CMOS
MDSPDTEST[33:1]	Pins reserved for production test (should be left open)	(1)	N/C
TRIG[1:0]	CLKTX/16 for use as trigger	50Ω internal pull-up to AV_{DD}_IO	Output/PCML
LOS	Global loss of signal status	(1)	Output/CMOS

NOTE:

1. 100 kΩ internal pull-ups on all CMOS inputs, unless noted as pull-downs.

3.0 Control Registers Map and Descriptions

Table 3-1. Control Registers Map (1 of 2)

Addr	Register Name	d7	d6	d5	d4	d3	d2	d1	d0: LSB
Common Registers									
00	INCHSEL#0	InChSel[7]	InChSel[6]	InChSel[5]	InChSel[4]	InChSel[3]	InChSel[2]	InChSel[1]	InChSel[0]
01	INCHSEL#1	InChSel[7]	InChSel[6]	InChSel[5]	InChSel[4]	InChSel[3]	InChSel[2]	InChSel[1]	InChSel[0]
02	INCHSEL#2	InChSel[7]	InChSel[6]	InChSel[5]	InChSel[4]	InChSel[3]	InChSel[2]	InChSel[1]	InChSel[0]
⋮		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
8Fh	INCHSEL#143	InChSel[7]	InChSel[6]	InChSel[5]	InChSel[4]	InChSel[3]	InChSel[2]	InChSel[1]	InChSel[0]
100	CHANCFG#0	offset	eql[1]	eql[0]	en_pe	out_level[1]	out_level[0]	in_mode[1]	in_mode[0]
101	CHANCFG#1	offset	eql[1]	eql[0]	en_pe	out_level[1]	out_level[0]	in_mode[1]	in_mode[0]
102	CHANCFG#2	offset	eql[1]	eql[0]	en_pe	out_level[1]	out_level[0]	in_mode[1]	in_mode[0]
⋮		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
18Fh	CHANCFG#143	offset	eql[1]	eql[0]	en_pe	out_level[1]	out_level[0]	in_mode[1]	in_mode[0]
200	IN_CHAN_CTRL#0	0	0	0	0	inh_en	0	los_en	0
201	IN_CHAN_CTRL#1	0	0	0	0	inh_en	0	los_en	0
⋮		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
28Fh	IN_CHAN_CTRL#143	0	0	0	0	inh_en	0	los_en	0
300	LOS_DR_SEL#0	0	dr_range	data_rate[5]	data_rate[4]	data_rate[3]	data_rate[2]	data_rate[1]	data_rate[0]
301	LOS_DR_SEL#1	0	dr_range	data_rate[5]	data_rate[4]	data_rate[3]	data_rate[2]	data_rate[1]	data_rate[0]
⋮		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
38Fh	LOS_DR_SEL#143	0	dr_range	data_rate[5]	data_rate[4]	data_rate[3]	data_rate[2]	data_rate[1]	data_rate[0]
Even PRBS Registers									
A0	PRBSRXCTRL_EVEN	en_patrx	0	rxmux	rst_rx	en_rx	core2rx	rxcdr_pd	0
A1	PRBSRXCHSEL_EVEN	rxchsel[7]	rxchsel[6]	rxchsel[5]	rxchsel[4]	rxchsel[3]	rxchsel[2]	rxchsel[1]	rxchsel[0]
A2	PRBSERROR_EVEN	rxerr[7]	rxerr[6]	rxerr[5]	rxerr[4]	rxerr[3]	rxerr[2]	rxerr[1]	rxerr[0]
A3	PRBSRX_DLY_EVEN	0	0	0	prbsrx_dly[4]	prbsrx_dly[3]	prbsrx_dly[2]	prbsrx_dly[1]	prbsrx_dly[0]
A4	RXCDR_CTRLA_EVEN	lolwinctrl[1]	lolwinctrl[0]	0	0	0	1	los_en	1
A5	RXCDR_CTRLB_EVEN	softreset	reserved	data_rate[5]	data_rate[4]	data_rate[3]	data_rate[2]	data_rate[1]	data_rate[0]
A6	RXCDR_ALARMS_EVEN	reserved	reserved	reserved	reserved	reserved	reserved	los	lol
A7	PRBSTXCTRL1_EVEN	0	txmux[1]	txmux[0]	rst_tx	en_tx	tx2core	pll_pd	0
A8	PRBSTXCTRL2_EVEN	0	0	pe_amp	en_pe	pe_dur	sel_div2pat	en_pattx	pwr_trig
A9	PRBSTXCHSEL_EVEN	txchsel[7]	txchsel[6]	txchsel[5]	txchsel[4]	txchsel[3]	txchsel[2]	txchsel[1]	txchsel[0]
AA	PLL_CTRLA_EVEN	lolwinctrl[1]	lolwinctrl[0]	0	0	0	0	0	1
AB	PLL_CTRLB_EVEN	softreset	reserved	data_rate[5]	data_rate[4]	data_rate[3]	data_rate[2]	data_rate[1]	data_rate[0]
Odd PRBS Registers									
AC	PRBSRXCTRL_ODD	en_patrx	0	rxmux	rst_rx	en_rx	core2rx	rxcdr_pd	0
AD	PRBSRXCHSEL_ODD	rxchsel[7]	rxchsel[6]	rxchsel[5]	rxchsel[4]	rxchsel[3]	rxchsel[2]	rxchsel[1]	rxchsel[0]
AE	PRBSERROR_ODD	rxerr[7]	rxerr[6]	rxerr[5]	rxerr[4]	rxerr[3]	rxerr[2]	rxerr[1]	rxerr[0]
AF	PRBSRX_DLY_ODD	0	0	0	prbsrx_dly[4]	prbsrx_dly[3]	prbsrx_dly[2]	prbsrx_dly[1]	prbsrx_dly[0]
B0	RXCDR_CTRLA_ODD	lolwinctrl[1]	lolwinctrl[0]	0	0	0	1	los_en	1
B1	RXCDR_CTRLB_ODD	softreset	reserved	data_rate[5]	data_rate[4]	data_rate[3]	data_rate[2]	data_rate[1]	data_rate[0]
B2	RXCDR_ALARMS_ODD	reserved	reserved	reserved	reserved	reserved	reserved	los	lol
B3	PRBSTXCTRL1_ODD	0	txmux[1]	txmux[0]	rst_tx	en_tx	tx2core	pll_pd	0
B4	PRBSTXCTRL2_ODD	0	0	pe_amp	en_pe	pe_dur	sel_div2pat	en_pattx	pwr_trig
B5	PRBSTXCHSEL_ODD	txchsel[7]	txchsel[6]	txchsel[5]	txchsel[4]	txchsel[3]	txchsel[2]	txchsel[1]	txchsel[0]
B6	PLL_CTRLA_ODD	lolwinctrl[1]	lolwinctrl[0]	0	0	0	0	0	1
B7	PLL_CTRLB_ODD	softreset	reserved	data_rate[5]	data_rate[4]	data_rate[3]	data_rate[2]	data_rate[1]	data_rate[0]

Table 3-1. Control Registers Map (2 of 2)

Addr	Register Name	d7	d6	d5	d4	d3	d2	d1	d0: LSB
Local Registers									
B8	XSETMODE	0	0	0	0	0	0	xset[1]	xset[0]
B9	XSETCMD	xsetcmd[7]	xsetcmd[6]	xsetcmd[5]	xsetcmd[4]	xsetcmd[3]	xsetcmd[2]	xsetcmd[1]	xsetcmd[0]
BA	IOENABLE	offset	eql[1]	eql[0]	en_individ	out_level[1]	out_level[0]	in_mode[1]	in_mode[0]
BB	CORECTRL	0	0	0	pe_amp	pe_dur	en_pe	1	en_smartpwr
BF	SOFTRESET	srst[7]	srst[6]	srst[5]	srst[4]	srst[3]	srst[2]	srst[1]	srst[0]
C0	CHIPREV	rev[7]	rev[6]	rev[5]	rev[4]	rev[3]	rev[2]	rev[1]	rev[0]
C1	PRODCODE	prod[7]	prod[6]	prod[5]	prod[4]	prod[3]	prod[2]	prod[1]	prod[0]
C3	WIN_INLCK_LOL	win_inlck[7]	win_inlck[6]	win_inlck[5]	win_inlck[4]	win_inlck[3]	win_inlck[2]	win_inlck[1]	win_inlck[0]
C4	WIN_OUTLCK_LOL	win_outlck[7]	win_outlck[6]	win_outlck[5]	win_outlck[4]	win_outlck[3]	win_outlck[2]	win_outlck[1]	win_outlck[0]
CB	GLOBAL_CTRL	0	0	0	0	0	1	0	clear_alarm
1A2	LOS_STATn	los_stat[7]	los_stat[6]	los_stat[5]	los_stat[4]	los_stat[3]	los_stat[2]	los_stat[1]	los_stat[0]
1A3	LOS_STATN	los_stat[7]	los_stat[6]	los_stat[5]	los_stat[4]	los_stat[3]	los_stat[2]	los_stat[1]	los_stat[0]
⋮		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1B3	LOS_STATN	los_stat[7]	los_stat[6]	los_stat[5]	los_stat[4]	los_stat[3]	los_stat[2]	los_stat[1]	los_stat[0]

NOTES:

D[7]... D[0] represent the internal bus, which is mapped to the data in both the serial and parallel mode.

Blank register bits are undefined for a write and read.

3.1 Control Registers Descriptions

Table 3-2. Input Channel Selection (INCHSEL: Address 00h–47h/00h–8Fh) (Output channel = address Input to route to output = data)

Bits	Type	Default	Label	Description
7:0	R/W	00h	INCHSEL	Select input channel (data) to route to selected output (address). In#0 = 00h, In#1 = 01h, …In#143 = 8Fh.

Table 3-3. I/O Input/Output Configuration (CHANCFG: Address 100h–147h/100h–18Fh) (Selected channel + 100h is the address)

Bits	Type	Default	Label	Description
7	R/W	0	DC offset	Input DC offset 0: DC offset enable (default) 1: DC offset disable
6:5	R/W	01	eq	Input equalization 00: Minimum EQ (≈ 9 dB) 01: Small EQ (≈ 12 dB) (default) 10: Medium EQ (≈ 15 dB) 11: Large EQ (≈ 18 dB)
4	R/W	0	en_pe	Enable de-emphasis—*en_individ* (BAh, bit 4) must be set to 1 for this bit to be functional. 0: Disabled. 1: Enabled.
3:2	R/W	11	out_level	*en_individ* (BAh, bit 4) must be set to 1 for these bits to be functional. 00: 500 mVp–p differential output. 01: 900 mVp–p differential output. 10: 1200 mVp–p differential output. 11: Disable output.
1:0	R/W	10	in_mode	*en_individ* (BAh, bit 4) must be set to 1 for these bits to be functional. 00: Reserved. 01: Reserved. 10: Input channel is powered down. 11: Input channel is active.

Table 3-4. Input Channel Control (IN_CHAN_CTRL: Address 200h–247h/200h–28Fh)

Bits	Type	Default	Label	Description
7:4	R/W	0000	—	Reserved, set to 0.
3	R/W	0	inh_en	0: Inhibit disabled. 1: Inhibit enabled.
2	R/W	1	—	Reserved, defaults to 1 but must be set to 0.
1	R/W	1	los_en	0: LOS disabled. 1: LOS enabled (default).
0	R/W	1	—	Reserved, defaults to 1 but must be set to 0.

Table 3-5. Individual Channel LOS Data Rate Control (Select Channel 300h-347h/300h-38Fh)

Bits	Type	Default	Label	Description
7	R/W	0	LOS_dr_sel	Reserved, default to 0.
6	R/W	0	dr_range	0: 2–3.2 Gbps operation (default). 1: 1–1.6 Gbps operation.
5:0	R/W	011010	—	Select data rate. See Section 4.3.9.1. for data rate programming. 011010: 2.488 Gbps (default).

3.1.1 Even PRBS Registers

Table 3-6. PRBS RX Control (Even) (PRBSRXCTRL_EVEN: Address A0h)

Bits	Type	Default	Label	Description
7	R/W	0	en_patrx	0: PRBSRX configured for 2^{23}-1 PRBS pattern. 1: PRBSRX configured for simple “1010” or “1100” pattern.
6	R/W			Reserved, must be set to 0.
5	R/W	1	rxmux	Select RX data input. 0: Select input form cross point core. 1: Select input from terminals DIRXP/N.
4	R/W	1	rst_rx	Reset RX PRBS receiver. 0: RX PRBS receiver enabled. 1: RX PRBS in reset.
3	R/W	0	en_rx	0: RX PRBS disabled. 1: RX PRBS enabled.
2	R/W	0	core2rx	0: Disconnect all cross point outputs from PRBS RX. 1: Route cross point outputs to PRBS receiver.
1	R/W	1	rxcdr_pd	PRBS receiver CDR control. 0: CDR is enabled. 1: CDR is disabled.
0	R/W	—	—	Reserved, must be set to 0.

Table 3-7. PRBS RX Channel Select (even) (PRBSRXCHSEL_EVEN: Address A1h)

Bits	Type	Default	Label	Description
7:0	R/W	00h	rxchSel	Selects channel for PRBS RX.

Table 3-8. PRBS RX Error Count (Read Only) (PRBSERROR_EVEN: Address A2h)

Bits	Type	Default	Label	Description
7:0	RO	—	rxerr	PRBS RX error count register (read-only). Although this is a read-only register, a write of any value must be performed to latch the latest error count. A PRBS RX reset (address A0h, bit 4) will clear the PRBS RX error count register.

Table 3-9. PRBS RX Delay Select (even) (PRBSRX_DLY_EVEN: Address A3h)

Bits	Type	Default	Label	Description
7:5	R/W	—	—	Reserved, must be set to 0
4:0	R/W	00101	prbsrx_dly	PRBS RX delay select in increments of 1/32 of a bit time (12.5 ps for 2.488 GHz operation). 00000: No Delay. 00001: 1/32 of a bit time (12.5 ps for 2.488 GHz operation). … 00101: 5/32 of a bit time (62.5 ps for 2.488 GHz operation) (default). … 11111: One bit time (400 ps for 2.488 GHz operation).

Table 3-10. PRBS RX CDR Control A (even) (RXCDR_CTRLA_EVEN: Address A4h)

Bits	Type	Default	Label	Description
7:6	R/W	00	lolwinctrl	00: LOL window settings are taken from global register. 01: LOL window settings are fixed to 48h (narrow) and 55h (wide). 10: LOL window settings are fixed to 91h (narrow) and AAh (wide) (recommended settings). 11: Content of register RXCDR_CTRLB is stored into a separate register, which programs the offset of the VCO counter start value.
5:4	R/W	—	—	Reserved, must be set to 0.
3	R/W	1	—	0: Autoinhibit disabled. 1: Autoinhibit enabled.
2	R/W	—	—	Reserved, must be set to 1.
1	R/W	1	los_en	0: LOS circuit disabled. 1: LOS enabled.
0	R/W	—	—	Reserved, must be set to 1.

Table 3-11. PRBS RX CDR Control B (even) (RXCDR_CTRLB_EVEN: Address A5h)

Bits	Type	Default	Label	Description
7	R/W	0	softreset	0: CDR is in normal mode. 1: CDR is in reset.
6	R/W	0	MSPD	Reserved, defaults to “0”, must be set to “1” to use PRBS RX CDR.
5:0	R/W	011010	data_rate	Select data rate. Please refer to Table 4-6 in the PRBS CDR Control Parameters section for data rate programming. 011010: Reference frequency multiplied by 128d.

Table 3-12. PRBS RX Alarms (Read Only) (even) (RXCDR_ALARMS_EVEN: Address A6h) (Cleared on write, a high alarm status gets latched into the register)

Bits	Type	Default	Label	Description
7:2	RO	—	—	Reserved.
1	RO	—	los	Loss of Signal alarm.
0	RO	—	lol	Loss of Lock alarm.

Table 3-13. PRBS TX Control 1 (even) (PRBSTXCTRL1_EVEN: Address A7h)

Bits	Type	Default	Label	Description
7	R/W	—	—	Reserved, must be set to 0.
6:5	R/W	10	txmux	Select PRBS TX clock input. 00: Select clock generated by PRBS TX PLL. 01: Select clock recovered from PRBS RX CDR. 10: Select clock from input pins CLKTXP/N. 11: None.
4	R/W	1	rst_tx	0: PRBS TX pattern generator in normal operation. 1: Reset PRBS TX pattern generator.
3	R/W	0	en_tx	0: TX PRBS disabled. 1: TX PRBS enabled.
2	R/W	0	tx2core	0: Disable the PRBS TX from going to the inputs. 1: Route PRBS TX pattern through cross point.
1	R/W	1	pll_pd	PRBS TX PLL control. 0: TX PLL enabled. 1: TX PLL disabled.
0	R/W	—	—	Reserved, must be set to 0.

Table 3-14. PRBS TX Control 2 (even) (PRBSTXCTRL2_EVEN: Address A8h)

Bits	Type	Default	Label	Description
7:6	R/W	—	—	Reserved, must be set to 0.
5	R/W	0	pe_amp	Control of de-emphasis amplitude. 0: 50% DE. 1: 67% DE.
4	R/W	0	en_pe	Enable de-emphasis. 0: Disable. 1: Enable.
3	R/W	1	pe_dur	Control of de-emphasis duration. 0: Approximately 1200 ps. 1: Approximately 600 ps.
2	R/W	0	sel_div2_pat	Select TX pattern. *en_pattx* has to be high for this bit to be functional. 0: Select 1010 pattern. 1: Select 1100 pattern.
1	R/W	0	en_pattx	Select TX PRBS or simple pattern. 0: Select PRBS TX pattern. 1: Select simple pattern: 1010 or 1100 determined by *sel_div2_pat*.
0	R/W	0	pwr_trig	0: TX PRBS trigger disabled. 1: TX PRBS trigger enabled.

Table 3-15. PRBS TX Channel Select (even) (PRBSTXCHSEL_EVEN: Address A9h)

Bits	Type	Default	Label	Description
7:0	R/W	01h	txchSel	Select channel for PRBS TX.

Table 3-16. PRBS TX PLL Control A (even) (PLL_CTRLA_EVEN: Address AAh)

Bits	Type	Default	Label	Description
7:6	R/W	00	lolwinctrl	00: LOL window settings are taken from global register. 01: LOL window settings are fixed to 48h (narrow) and 55h (wide). 10: LOL window settings are fixed to 91h (narrow) and AAh (wide) (recommended setting). 11: Content of register PLL_CTRLB is stored into a separate register, which programs the offset of the VCO counter start value.
5:1	R/W	—	—	Reserved, must be set to 0.
0	R/W	—	—	Reserved, must be set to 1.

Table 3-17. PRBS TX PLL Control B (even) (PLL_CTRLB_EVEN: Address ABh)

Bits	Type	Default	Label	Description
7	R/W	0	softreset	0: PLL is in normal mode. 1: PLL is in reset.
6	R/W	0	MSPD	Reserved, defaults to “0”, must be set to “1” to use PRBS Tx PLL.
5:0	R/W	011010	data_rate	Select data rate. Please refer to Table 4-6 in the PRBS CDR Control Parameters section for data rate programming. 011010: Reference frequency multiplied by 128d.

3.1.2 Odd PRBS Registers

Table 3-18. PRBS RX Control (Odd) (PRBSRXCTRL_ODD: Address ACh)

Bits	Type	Default	Label	Description
7	R/W	0	en_patrx	0: PRBSRX configured for 2^{23}-1 PRBS pattern. 1: PRBSRX configured for simple “1010” or “1100” pattern.
6	R/W			Reserved, must be set to 0.
5	R/W	1	rxmux	Select RX data input. 0: Select input from cross point core. 1: Select input from terminals DiRxP/N.
4	R/W	1	rst_rx	Reset RX PRBS receiver. 0: RX PRBS receiver enabled. 1: RX PRBS in reset.
3	R/W	0	en_rx	0: RX PRBS disabled. 1: RX PRBS enabled.
2	R/W	0	core2rx	0: Disconnect all cross point outputs from PRBS RX. 1: Route cross point outputs to PRBS receiver.
1	R/W	1	rxcdr_pd	PRBS receiver CDR control. 0: CDR is enabled. 1: CDR is disabled.
0	R/W	—	—	Reserved, must be set to 0.

Table 3-19. PRBS RX Channel Select (odd) (PRBSRXCHSEL_ODD: Address ADh)

Bits	Type	Default	Label	Description
7:0	R/W	01h	rxchSel	Selects channel for PRBS RX.

Table 3-20. PRBS RX Error Count (Read Only) (odd) (PRBSERROR_ODD: Address AEh)

Bits	Type	Default	Label	Description
7:0	RO	—	rxerr	PRBS RX error count register (read-only). Although this is a read-only register, a write of any value must be performed to latch the latest error count. A PRBS RX reset (address A0h, bit 4) will clear the PRBS RX error count register.

Table 3-21. PRBS RX Delay Select (odd) (PRBSRX_DLY_ODD: Address AFh)

Bits	Type	Default	Label	Description
7:5	R/W			Reserved, must be set to 0.
4:0	R/W	00101	prbsrx_dly	PRBS RX delay select in increments of 1/32 of a bit time (12.5 ps for 2.488 GHz operation). 00000: No Delay. 00001: 1/32 of a bit time (12.5 ps for 2.488 GHz operation). … 00101: 5/32 of a bit time (62.5 ps for 2.488 GHz operation). … 11111: One bit time (400 ps for 2.488 GHz operation).

Table 3-22. PRBS RX CDR Control A (odd) (RXCDR_CTRLA_EVEN: Address B0h)

Bits	Type	Default	Label	Description
7:6	R/W	00	lolwinctrl	00: LOL window settings are taken from global register. 01: LOL window settings are fixed to 48h (narrow) and 55h (wide). 10: LOL window settings are fixed to 91h (narrow) and AAh (wide) (recommended setting). 11: Content of register RXCDR_CTRLB is stored into a separate register, which programs the offset of the VCO counter start value.
5:4	R/W	—	—	Reserved, must be set to 0.
3	R/W	1	—	0: Autoinhibit disabled. 1: Autoinhibit enabled.
2	R/W	—	—	Reserved, must be set to 1.
1	R/W	1	los_en	0: LOS circuit disabled. 1: LOS enabled.
0	R/W	—	—	Reserved, must be set to 1.

Table 3-23. PRBS RX CDR Control B (odd) (RXCDR_CTRLB_ODD: Address B1h)

Bits	Type	Default	Label	Description
7	R/W	0	softreset	0: CDR is in normal mode. 1: CDR is in reset.
6	R/W	0	MSPD	Reserved, defaults to “0”, must be set to “1” to use PRBS RX CDR.
5:0	R/W	011010	data_rate	Select data rate. Please refer to Table 4-6 in the PRBS CDR Control Parameters section for data rate programming. 011010: Reference frequency multiplied by 128d.

Table 3-24. PRBS RX Alarms (Read Only) (odd) (RXCDR_ALARMS_ODD: Address B2h)

Bits	Type	Default	Label	Description
7:2	RO	—	—	Reserved.
1	RO	—	los	Loss of Signal alarm.
0	RO	—	lol	Loss of Lock alarm.

Table 3-25. PRBS TX Control 1 (odd) (PRBSTX_ctrl1_odd: Address B3h)

Bits	Type	Default	Label	Description
7	R/W	—	—	Reserved, must be set to 0.
6:5	R/W	10	txmux	Select PRBS TX clock input. 00: Select clock generated by PRBS TX PLL. 01: Select clock recovered from PRBS RX CDR. 10: Select clock from input terminals CLKTXP/N. 11: None.
4	R/W	1	rst_tx	0: PRBS TX pattern generator in normal operation. 1: Reset PRBS TX pattern generator.
3	R/W	0	en_tx	0: TX PRBS disabled. 1: TX PRBS enabled.
2	R/W	0	tx2core	0: Disable the PRBS TX from going to the inputs. 1: Route PRBS TX pattern through cross point.
1	R/W	1	pll_pd	PRBS TX PLL control. 0: TX PLL is enabled. 1: TX PLL is disabled.
0	R/W	—	—	Reserved, must be set to 0.

Table 3-26. PRBS TX Control 2 (odd) (PRBSTX_ctrl2_odd: Address B4h)

Bits	Type	Default	Label	Description
7:6	R/W	—	—	Reserved, must be set to 0.
5	R/W	0	pe_amp	Control of de-emphasis amplitude. 0: 50% PE. 1: 67% PE.
4	R/W	0	en_pe	Enable de-emphasis. 0: Disable. 1: Enable.
3	R/W	1	pe_dur	Control of de-emphasis duration. 0: Approximately 1200 ps. 1: Approximately 600 ps.
2	R/W	0	sel_div2_pat	Select TX pattern. *en_pattx* has to be high for this bit to be functional. 0: Select 1010 pattern. 1: Select 1100 pattern.
1	R/W	0	en_pattx	Select TX PRBS or simple pattern. 0: Select PRBS TX pattern. 1: Select simple pattern: 1010 or 1100 determined by *sel_div2_pat*.
0	R/W	0	pwr_trig	0: TX PRBS trigger disabled. 1: TX PRBS trigger enabled.

Table 3-27. PRBS TX Channel Select (odd) (PRBSTXCHSEL_ODD: Address B5h)

Bits	Type	Default	Label	Description
7:0	R/W	01h	txchSel	Selects channel for PRBS TX.

Table 3-28. PRBS TX PLL Control A (odd) (PLL_CTRLA_ODD: Address B6h)

Bits	Type	Default	Label	Description
7:6	R/W	00	lolwinctrl	00: LOL window settings are taken from global register. 01: LOL window settings are fixed to 48h (narrow) and 55h (wide). 10: LOL window settings are fixed to 91h (narrow) and AAh (wide) (recommended setting). 11: Content of register PLL_ctrlB is stored into a separate register, which programs the offset of the VCO counter start value.
5:1	R/W	—	—	Reserved, must be set to 0.
0	R/W	—	—	Reserved, must be set to 1.

Table 3-29. PRBS TX PLL Control B (odd) (PLL_CTRLB_ODD: Address B7h)

Bits	Type	Default	Label	Description
7	R/W	0	softreset	0: CDR is in normal mode. 1: CDR is in reset.
6	R/W	0	MSPD	Reserved, defaults to “0”, must be set to “1” to use PRBS TX PLL.
5:0	R/W	011010	data_rate	Select data rate. Please refer to Table 4-6 in the PRBS CDR Control Parameters section for data rate programming. 011010: Reference frequency multiplied by 128d.

3.1.3 Global Registers

Table 3-30. XSET MODE (xSET mode: Address B8h)

Bits	Type	Default	Label	Description
7:2	R/W	—	—	Reserved, must be set to 0.
1:0	R/W	00	xset	Selects the XSET mode. 00: ACL latches are transparent. Any switch setting written immediately affects the core configuration. 01: ACL latches are controlled through register B9h (software XSET). 10: ACL latches are controlled by terminal **XSET** (hardware control). 11: N/A.

Table 3-31. Software xSET (Read back always 00h) (xSET cmd: Address B9h)

Bits	Type	Default	Label	Description
7:0	R/W	—	xsetcmd	Register B8h (XSET mode) needs to be set to 01 in order for this register to be functional. Any value written to this register will update the ACL with the ICL.

Table 3-32. I/O Enable (IOENABLE: Address BAh)

Bits	Type	Default	Label	Description
7	R/W	0	DC offset	Input DC offset 0: DC offset enable (default) 1: DC offset disable
6:5	R/W	01	EQ	Input equalization 00: Minimum EQ (≈ 9 dB) 01: Small EQ (≈ 12 dB) (default) 10: Medium EQ (≈ 15 dB) 11: Large EQ (≈ 18 dB)
4	R/W	0	en_individ	This bit controls individual IO control. 0: Individual input/output configuration (100 to 147h/100h to 18Fh) is bypassed. 1: Input/outputs are individually controlled by registers 100 to 147h/100h to 18Fh.
3:2	R/W	11	out_level	*en_individ* (BAh, bit 4) must be set to 0 for these bits to be functional. 00: 500 mVp–p differential on all outputs. 01: 900 mVp–p differential on all outputs. 10: 1200 mVp–p differential on all outputs. 11: Disable all outputs.
1:0	R/W	10	in_mode	*en_individ* (BAh, bit 4) must be set to 0 for these bits to be functional. 00: Reserved. 01: Reserved. 10: All input channels are powered down. 11: All input channels are active.

Table 3-33. Core Control (CORECTRL: Address BBh)

Bits	Type	Default	Label	Description
7:5	R/W	—	—	Reserved, must be set to 0.
4	R/W	0	pe_amp	Global control of de-emphasis amplitude. 0: 50% PE. 1: 67% PE.
3	R/W	1	pe_dur	Global control of de-emphasis duration. 0: Approximately 1200 ps. 1: Approximately 600 ps (default).
2	R/W	0	en_pe	*en_individ* (BAh, bit 4) must be set to 0 for this bit to be functional. 0: Disable de-emphasis for all outputs. 1: Enable de-emphasis for all outputs.
1	R/W	—	—	Reserved, must be set to 1.
0	R/W	1	en_smartpwr	Core SmartPower™ control. 0: Core fully powered. 1: Core in low power mode.

Table 3-34. Software Reset (SOFTRESET: Address BFh)

Bits	Type	Default	Label	Description
7:0	R/W	00h	srst	Software reset: Needs two consecutive Writes with DATA = AAh. If second Write is not a reset, register is cleared. Third Write required to bring out of reset.

Table 3-35. Chip Revision (CHIPREV: Address C0h)

Bits	Type	Default	Label	Description
7:0	RO	—	rev	Chip Revision Number: M21131-13/M21131G-13: 05h M21131-23/M21131G-23: 05h M21151-14/M21151G-14: 05h M21151-23/M21151G-23: 05h

Table 3-36. Product Code (PRODCODE: Address C1h)

Bits	Type	Default	Label	Description
7:0	RO	—	prod	Product Code Number M21131 = 40h M21151 = C0h

Table 3-37. Global LOL Window Detector Inlock Value (WIN_INLCK_LOL: Address C3h)

Bits	Type	Default	Label	Description
7:0	R/W	1Eh	win_inlck	Sets the in lock window value.

Table 3-38. Global LOL Window Detector Outlock Value (WIN_OUTLCK_LOL: Address C4h)

Bits	Type	Default	Label	Description
7:0	R/W	03	win_outlck	Sets the out lock window value.

Table 3-39. Global Control (GLOBAL_CTRL: Address CBh)

Bits	Type	Default	Label	Description
7:3	R/W	—	—	Reserved, must be set to 0.
2	R/W	—	—	Reserved, must be set to 1.
1	R/W	—	—	Reserved, must be set to 0.
0	R/W	0	clear_alarms	0: All input and PRBS LOS alarms are active. 1: Clear all PRBS and input LOS alarms.

Table 3-40. LOS Alarms Register Bank 1 to 18 (LOS_STATn: 1A2–1B3h)

Bits	Type	Default	Label	Description
7:0	RO	—	los_stat	(Read only, cleared by clear_alarms). 0: LOS alarm on CDR (n*8 +[I]) is not present. 1: LOS alarm on CDR (n*8 +[I]) is present.

4.0 Functional Description

4.1 Overview

The M21131/M21151, designed for today's demanding telecom and datacom applications, is a low-power CMOS, high-speed 72x72/144x144 crosspoint switch with input equalization, output de-emphasis, and built-in system test features.

The SmartPower™ features offer dynamically scalable switch settings to further reduce power consumption without affecting the operation of the remaining channels.

To improve signal quality each input buffer is preceded by a programmable input equalizer (IE) and each output includes output de-emphasis (PE). The IE removes ISI jitter which is usually caused by PCB skin effect losses. The IE circuit opens the input data eye in applications where long PCB traces and cables are used. The PE provides a boost of the high frequency content of the output signal, such that the data eye remains open after passing through a long interconnect of PCB traces and cables. There are two amplitude settings and two duration settings that can be selected on a global basis. De-emphasis can be enabled on a per-channel basis.

The device supports data rates from 0 to 3.2 Gbps on each channel, allowing any combination of SONET, Fibre Channel (1x and 2x), InfiniBand, Gigabit Ethernet and 10 Gbps Ethernet traffic.

The switch includes a pair of on-board 2^{23}-1 pseudo-random bit sequence transmitters (PRBS TX) and receivers (PRBS RX) for system verification purposes.

Three-stage switch fabrics with up to 2,880 x 2,880 ports, carrying over 10 Terabits per second of traffic, can be designed using this non-blocking switch, with multi-cast and broadcast abilities.

All inputs and outputs are differential PCML (positive current mode logic) with supply voltages ranging from 1.2V to 2.5V. The output levels are programmable at 500 mV, 900 mV, and 1200 mV.

The M21131/M21151 is available in a 1156 terminal, 35 mm, CBGA (Ceramic Ball Grid Array) package. The green 72x72/144x144 crosspoint switch is the M21131G/M21151G. The green devices share the same features, specifications, and pinout as the non-green devices.

Figure 4-1. Jitter Removal by Input Equalization and Output De-Emphasis at 3.2 Gbps

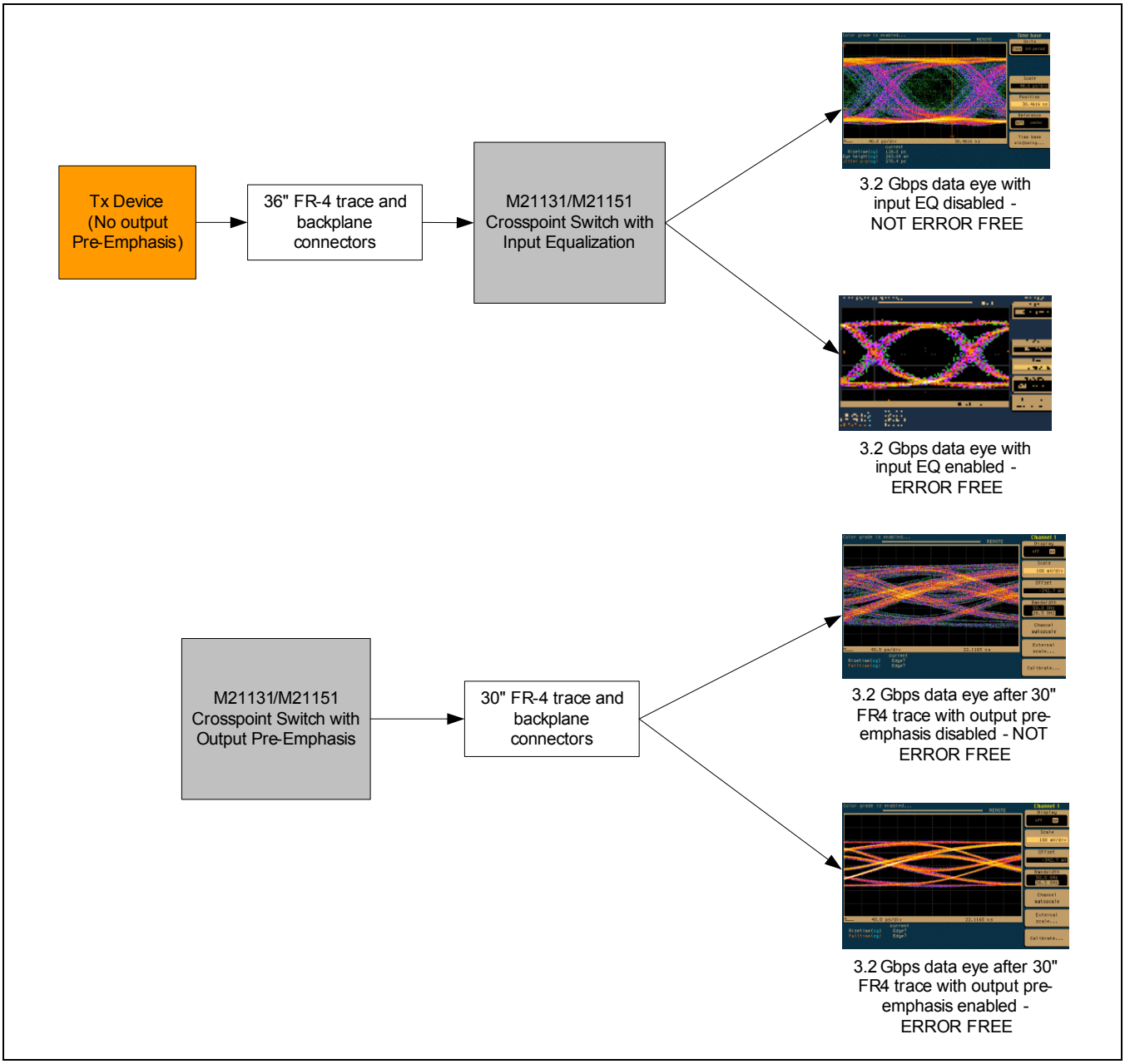


Figure 4-2. M21131/M21151 Functional Block Diagram

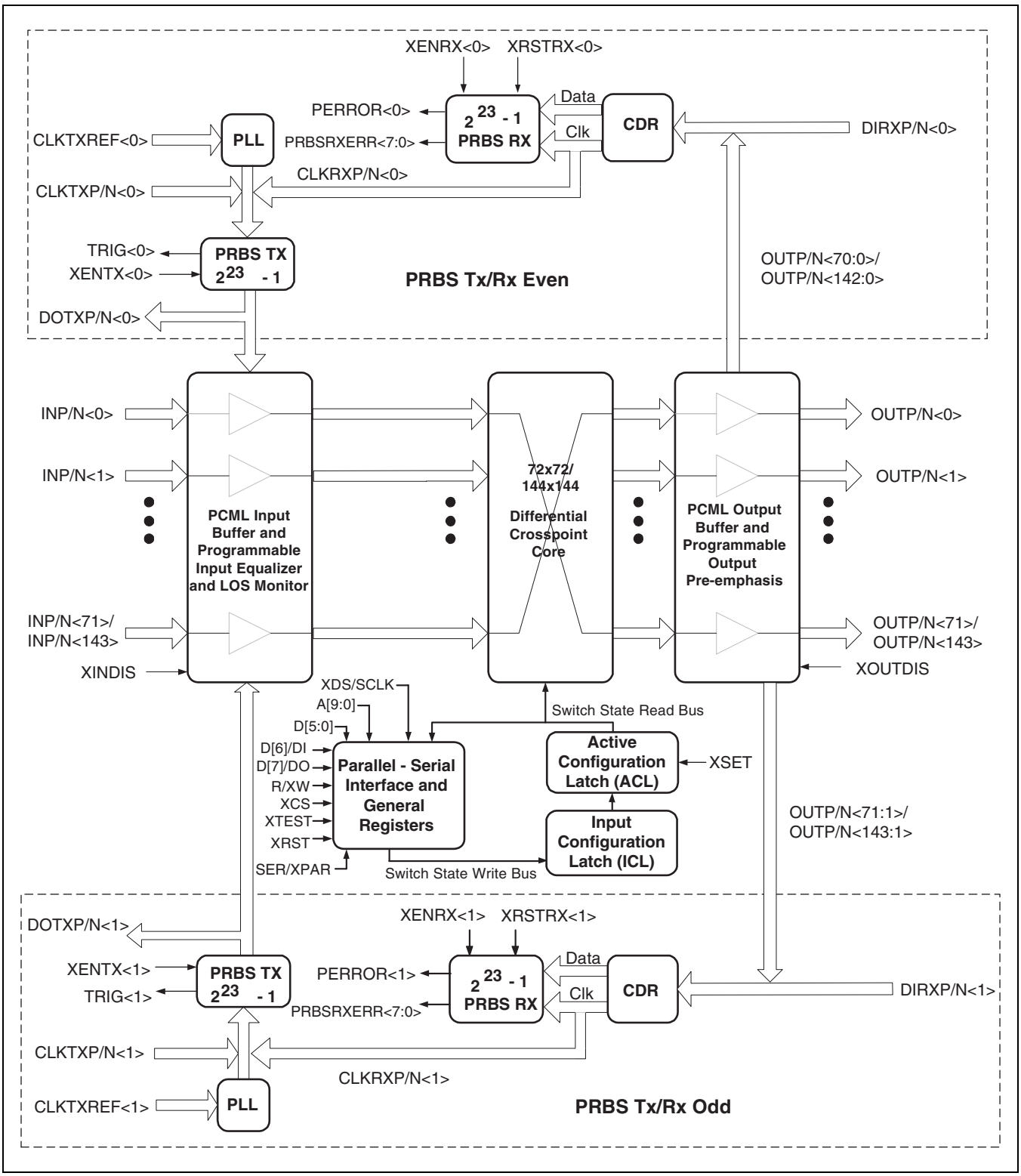


Figure 4-3. PCML Input and Output Equivalent Circuits

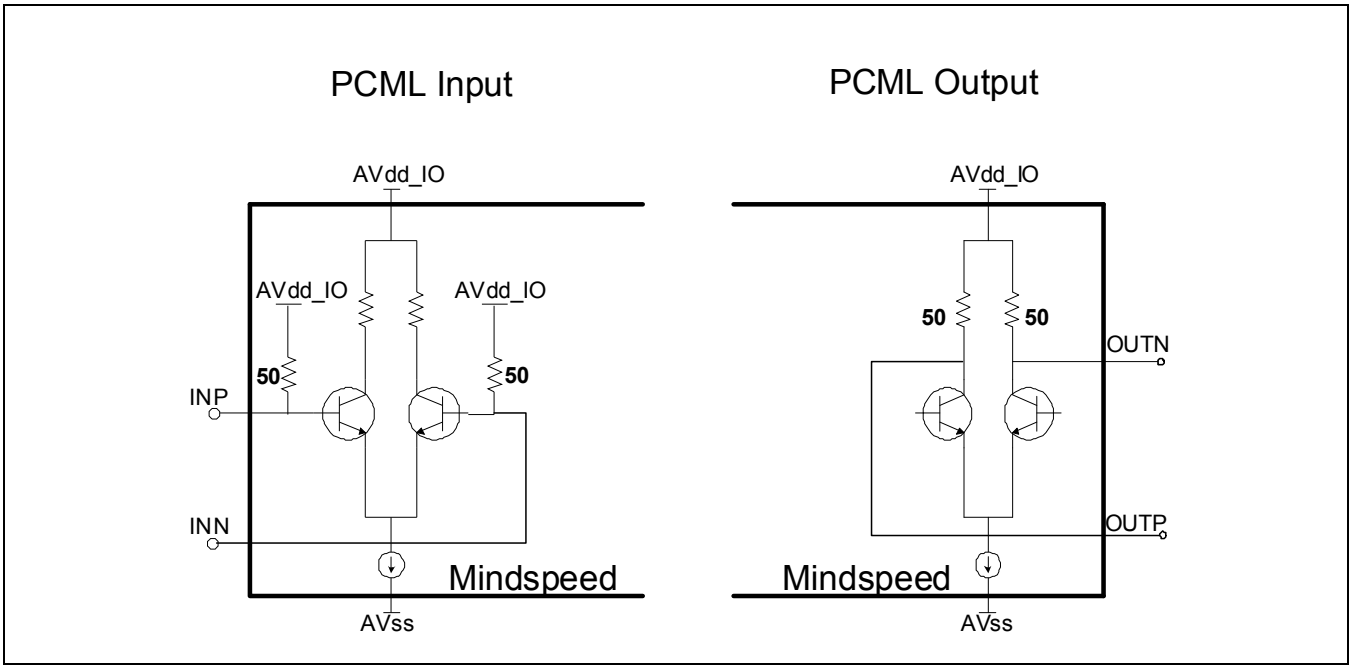
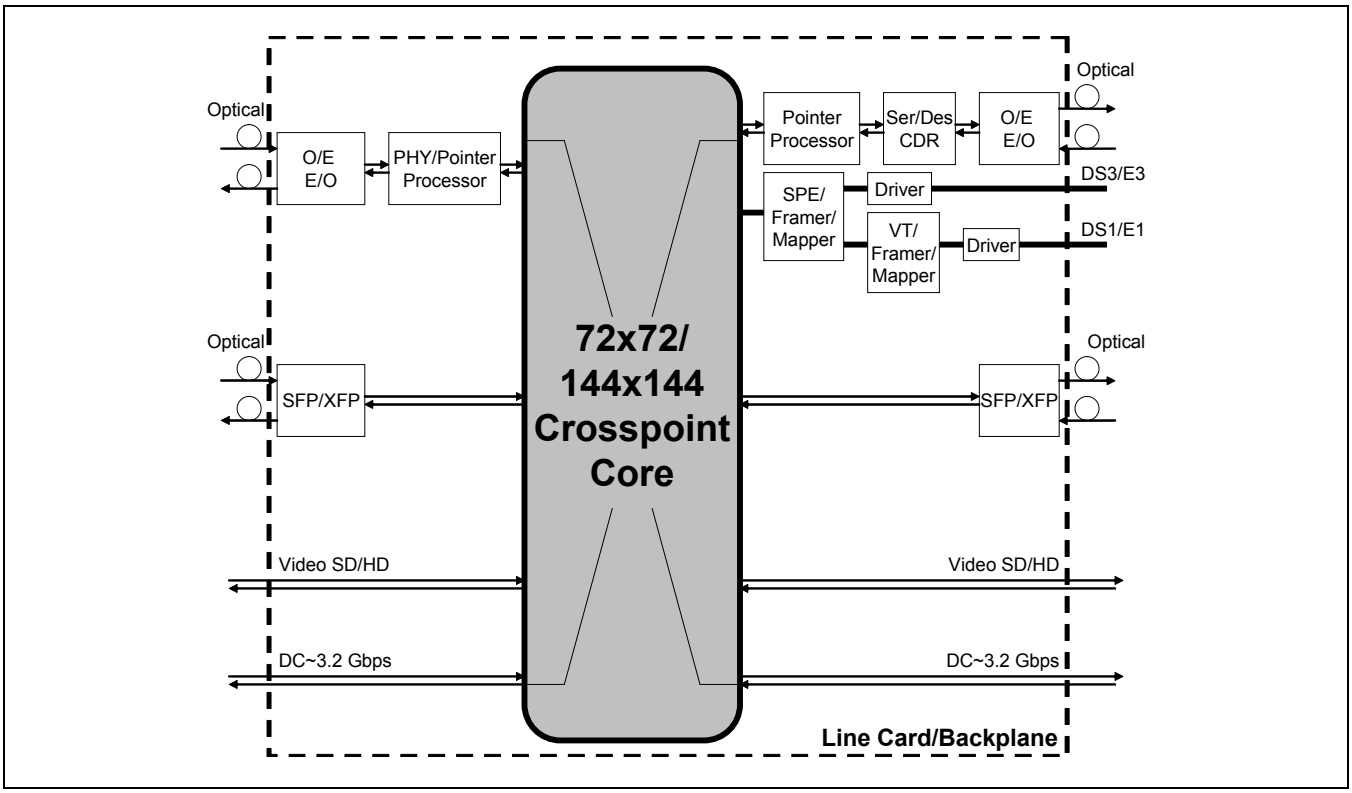


Figure 4-4. Crosspoint Application Example



4.2 Detailed Description

4.2.1 Document Conventions

This document uses the following text styling conventions:

Signal names and terminal numbers are listed in all upper case letters denoting each functional name part, with its related signal polarity indicated by a upper case 'N' or 'P'. Thus, data input signal names are indicated, for example as: 'DINP' and 'DINN'.

A signal name and an associated channel number (0 through 71/0 through 143) are indicated as DINP[n] and DINN[n] where 'n' is a channel number.

A register name is typed in all upper case preceded by the word register with each functional name part separated by an underscore, additionally, brackets group register bit numbers, and sub-function names are in initial caps such as for example only: 'register CONTROL_FUNCTION[5:4] Los_hyst'.

In order to distinguish terminal names from internally generated signals, the word ‘terminal’ is included in reference to an input, output, or control, such as: ‘the signal on terminal ABC controls function x', or ‘when the signal on terminal ABC = H function x is enabled'.

Terminal function descriptions generally do not repeat the word terminal.

4.2.2 Power Supply Configurations

Below is a summary of possible voltage configurations for the switch core and input/output buffers.

- 2.5V IO, 1.2V core
- 1.8V IO, 1.2V core
- 1.5V IO, 1.2V core
- 1.2V IO, 1.2V core (tied together externally)

The I/O supply voltage can be chosen independently, no register bit setting is required. The AV_{DD}_IO and AV_{DD}_CORE supplies are separate from the DV_{DD}_IO supply, and can be any combination of values specified in Table 1-2.

4.3 Serial Interface and Switch Programming

The crosspoint switch uses +1.8V/+2.5V/+3.3V CMOS interface levels to program the switch state (SS). All input terminals have a 100 KΩ internal pull-up, except XINDIS and XOUTDIS, which have internal 100 KΩ pull-downs. The communication protocol may be either a serial synchronous interface or a parallel asynchronous interface using eight or ten bits. Either interface can:

- Program the switch state
- Individually enable/disable inputs or outputs
- Access control registers and auxiliary functions
- Read back the current state of the switch
- Control the programmable equalization

This section details the operation of the I/O interface and switch programming in Section 4.3.4. The auxiliary functions and address mapping are described in the section, Switch Function Details.

4.3.1 Switch State Register Concept

The various switch functions are accessed through 8-bit registers (memory), which are addressed with the 10-bit address bus. The contents of the registers are transferred via an 8-bit data bus during a read or write.

The M21131/M21151 switch-state controller uses a double-buffered register. The active configuration latch (ACL) holds the actual switch setting while the input configuration latch (ICL) holds either the actual switch setting or the next switch setting, depending on the mode of operation.

The XSETMODE register selects one of three modes of operation:

- **Default Mode**—core configuration updated after every register write.

  With XSETMODE = 00h, the first mode is enabled and is the default mode after a reset. Consequently, the state of the switch changes with each write to a register determining the switch state. In the write mode, as soon as the signal on terminal XDS makes a low-to-high transition, the input channel specified by data for the output selected by the 10-bit address bus passes directly through the double buffer memory (ICL/ACL). As soon as the desired data passes through the ACL, the crosspoint core routes the selected input to the desired output to physically change the switch state. On the rising edge of XDS, this channel is stored (latched) into both the ICL and ACL.

- **XSET Mode**—core configuration updated after hardware XSET command.

  When register XSETMODE = 10b the hardware XSET mode is enabled. In this mode, the desired switch state (which may contain one or more routing changes) is written first to the ICL, but the switch state does not change since the data is blocked from the ACL. With either the hardware or software XSET command, the contents of the ICL are transferred to the ACL, which physically changes the switch state in the switching core. This mode allows 1 to 144 channels to change at the same time. On the falling edge of the XSET signal, the ICL contents are passed to the ACL and the switch state changes. On the rising edge of the XSET signal, the switch state is latched.

- **XSET Mode**—core configuration updated after software XSET command.

  When register XSETMODE = 01b the software XSET mode is selected, and the desired switch routing is written into the appropriate registers to update the ICL without affecting the ACL. Then, a write of any value to the XSETCMD register will update the ACL with the current contents of the ICL, and the switch state changes. The interface is configured into the parallel mode by forcing terminal SER/XPAR low.

4.3.2 Parallel I/O Overview

A 10-bit address bus and the register contents (read or write) are transferred via a bidirectional 8-bit data bus. The active-low data strobe (XDS) latches (stores) the data into the register on the rising edge of XDS. To change the switch state, the double buffer (ICL/ACL) is transparent (mode1) when signal XDS = L in relationship to the data, consequently the switch state will change on the falling edge of signal XDS. On the rising edge of XDS, the switch state will be stored into the register.

The active low terminal XCS gates the I/O and input control signal R/XW selects either a read or write operation. Figure 4-5 illustrates the timing diagram for a parallel write operation.

Table 4-1 shows the parallel write timing specifications as defined in Figure 4-5.

Figure 4-5. Parallel Write Timing Diagram

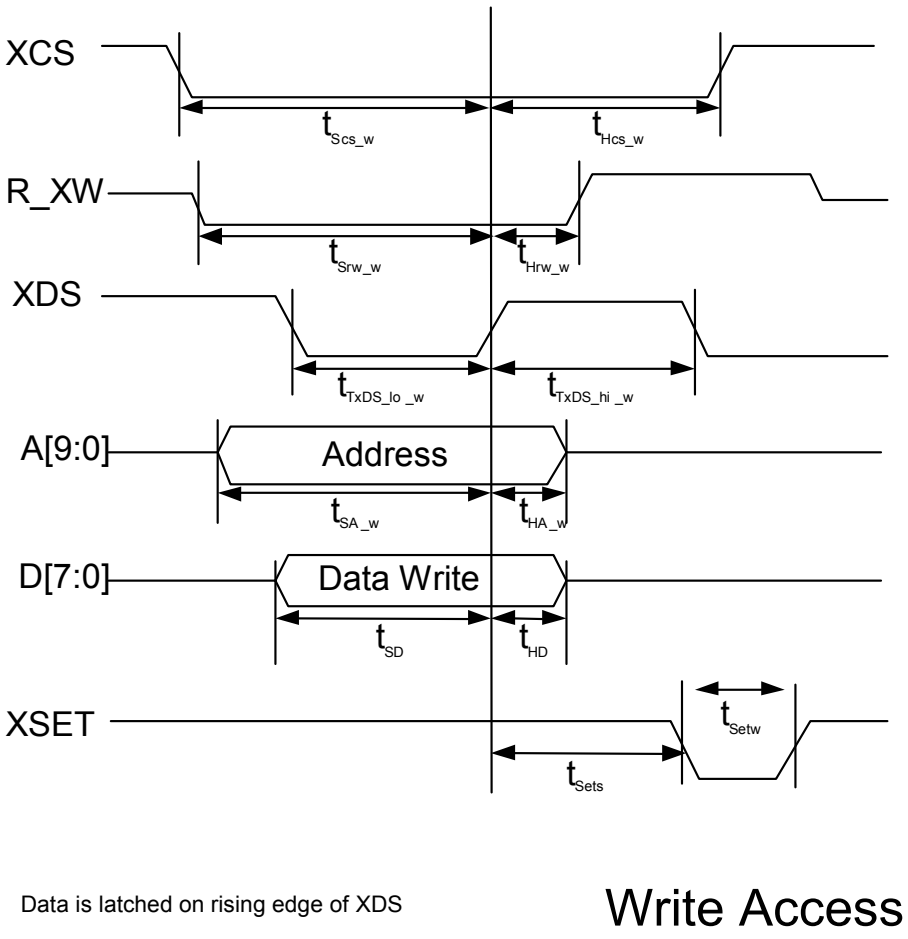


Table 4-1. Parallel I/O Write Timing

Parameter	Description	Minimum	Typical	Maximum
t_{Scs_w}	XCS Falling Edge before XDS Rising Edge	5 ns	—	—
t_{Hcs_w}	XCS Hold after Rising Edge of XDS	0 ns	—	—
t_{Hrw_w}	R/XW Hold after Rising Edge of XDS	0 ns	—	—
t_{Srw_w}	R/XW Setup before Rising Edge of XDS	9 ns	—	—
t_{TxDSl_w}	XDS Low Period	8 ns	—	—
t_{TxDSh_w}	XDS High Period	8 ns	—	—
t_{SA_w}	Address Setup before Rising Edge of XDS	6 ns	—	—
t_{HA_w}	Address Hold after Rising Edge of XDS	3 ns	—	—
t_{SD_w}	Data Setup before Rising Edge of XDS	3 ns	—	—
t_{HD_w}	Data Hold after Rising Edge of XDS	3 ns	—	—
t_{setw}	Hardware XSET pulse width	20 ns	—	—
t_{sets}	Hardware XSET setup time	3 ns	—	—

Figure 4-6 shows the timing diagram for a parallel read operation. Table 4-2 shows the parallel read timing specifications as defined in Figure 4-6.

Figure 4-6. Parallel Read Timing Diagram

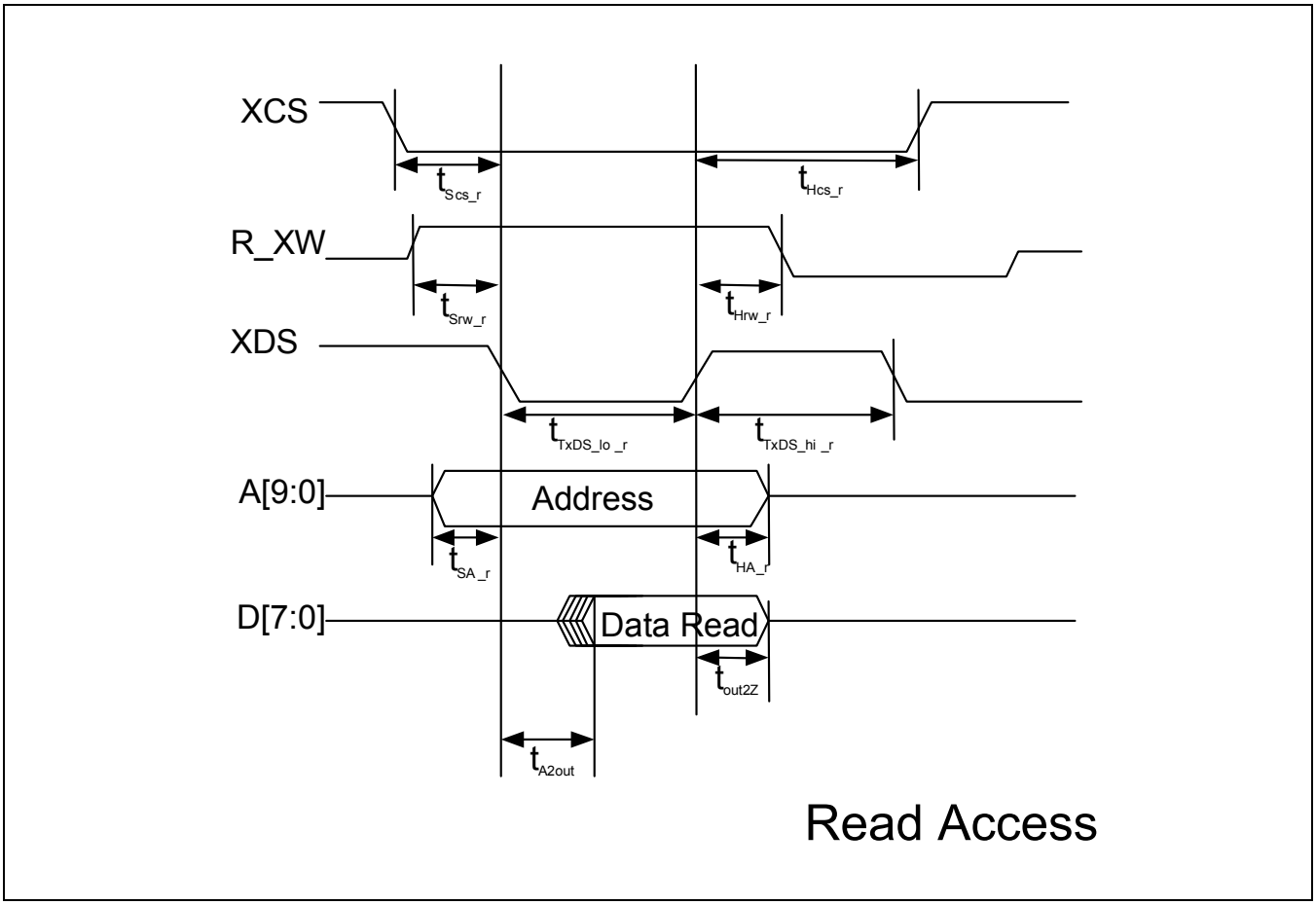


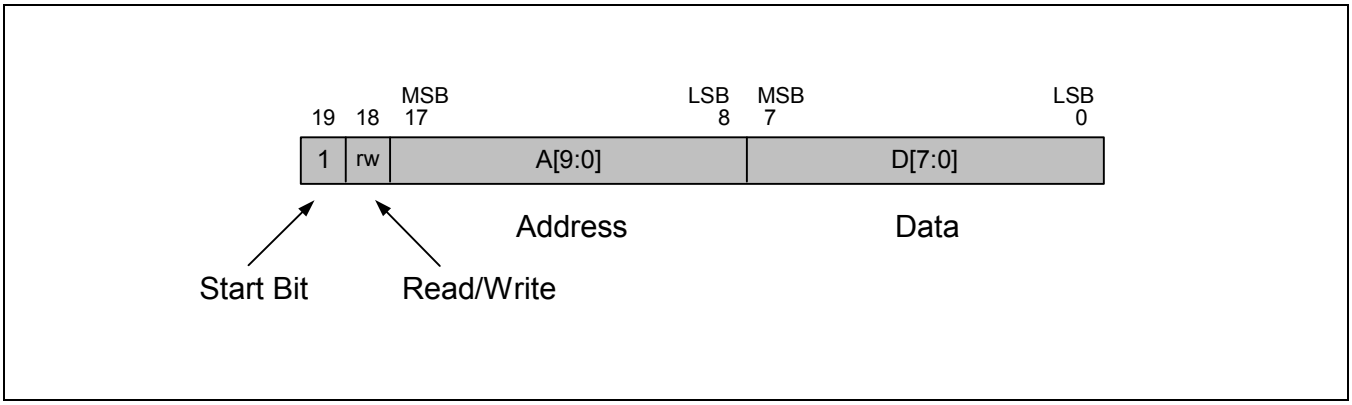
Table 4-2. Parallel I/O Read Timing

Parameter	Description	Minimum	Typical	Maximum
t_{Scs_r}	XCS Falling Edge before XDS Falling Edge	5 ns	—	—
t_{Hcs_r}	XCS Hold after Rising Edge of XDS	0 ns	—	—
t_{Hrw_r}	R/XW Hold after Rising Edge of XDS	0 ns	—	—
t_{Srw_r}	R/XW Setup before Falling Edge of XDS	5 ns	—	—
t_{TxDSl_r}	XDS Low Period	50 ns	—	—
t_{TxDSh_r}	XDS High Period	50 ns	—	—
t_{SA_r}	Address Setup before Falling Edge of XDS	9 ns	—	—
t_{HA_r}	Address Hold after Rising Edge of XDS	2 ns	—	—
t_{a2out}	Address Valid to Data Valid (on Read)	—	—	24 ns
t_{out2Z}	XDS Rising Edge to Data High Z	1 ns	—	8 ns

4.3.3 Serial I/O Overview

The serial I/O operation is gated by chip select signal XCS (on input terminal XCS). Data is shifted in on terminal SDI on the falling edge of the serial I/O clock input (terminal SCLK), and shifted out on the serial data output (terminal SDO) on the rising edge of SCLK. Addressing a register consists of the following, as shown in Figure 4-7: A 12-bit input, consisting of the first bit (start bit, SB = 1), the second bit (operation bit: OP = 1 for read, OP = 0 for write), followed by the 10-bit address (most significant bit (MSB) first).

Figure 4-7. Serial Word Format



4.3.3.1 Timing Diagram Clock Set and Program Modes

To initiate a write sequence, as shown in Figure 4-8, terminal XCS goes low before the falling edge of SCLK. On each falling edge of serial I/O clock (SCLK) the 20-bit word consisting of SB = 1, OP = 0, address, and data, are latched into the input shift register. The rising edge of signal XCS must occur before the falling edge of SCLK for the last bit. Upon receipt of the last bit, one additional cycle of SCLK is necessary before the input data transfers from the input shift register to the addressed register.

If consecutive read/write cycles are being performed, it is not necessary to insert an extra clock cycle between read/write cycles, however one extra clock cycle is needed after the last data bit of the final read/write cycle to complete the operation. On a write cycle, only the first 18 bits after SB and OP are used and all bits that follow are ignored.

Figure 4-9 illustrates the serial read mode timing diagram. To initiate a read sequence, the signal on terminal XCS goes low before the falling edge of SCLK. On each falling edge of SCLK, the 12 bits consisting of SB = 1, OP = 1, and the10-bit address are written to the serial input shift register of the M21131/M21151. On the first rising edge following the address LSB, the SB and eight bits of the data are shifted out on SDO. The first bit output on SDO for a read operation is always 0.

In a read cycle, all extra clock cycles will result in invalid data. For invalid SB/OP, the operation is undefined. The falling edge of XCS always resets the serial operation for a new read/write cycle.

Table 4-3 contains the timing specifications for the serial programming interface.

Figure 4-8. Serial Write Mode

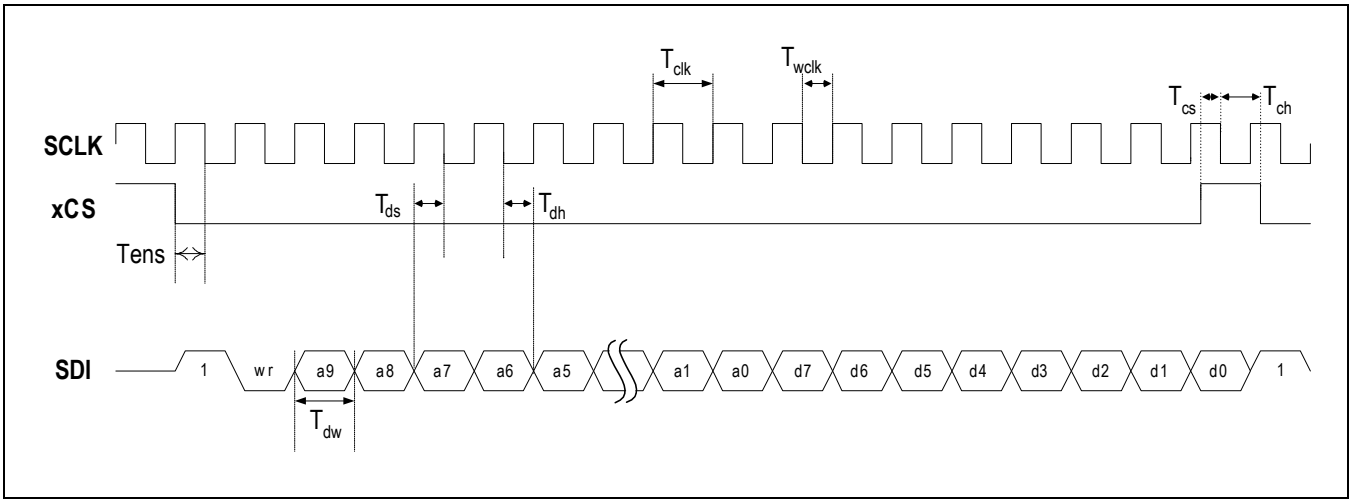


Figure 4-9. Serial Read Mode

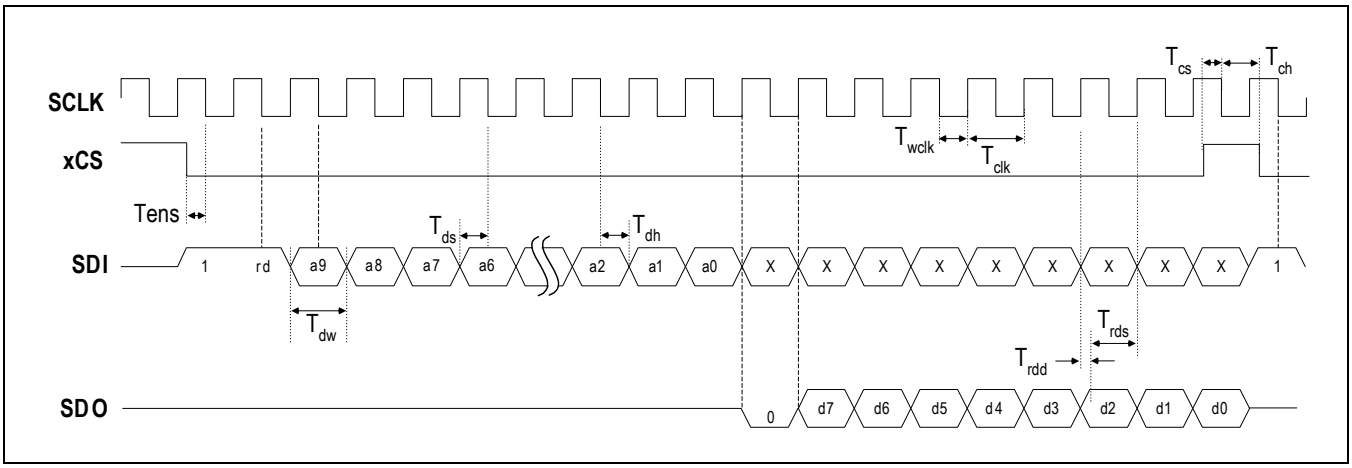


Table 4-3. Serial Interface Timing—Specified at Recommended Operating Conditions

Symbol	Item	Notes	Minimum	Typical	Maximum	Units
t_{dw}	Data width	—	14	—	—	ns
t_{dh}	Data hold time	—	5	—	—	ns
t_{ds}	Data setup time	—	5	—	—	ns
t_{ens}	Enable setup time	—	5	—	—	ns
t_{cs}	Chip select setup time	—	2	—	T_{clk} - 2	ns
t_{ch}	Chip select hold time	—	2	—	—	ns
t_{rDD}	Read data output delay	—	1	—	14	ns
t_{rds}	Read data valid	—	9	—	—	ns
t_{clk}	SCLK period width	—	40	—	—	ns
t_{wclk}	SCLK minimum low duration	—	5	—	T_{clk} - 5	ns
t_r	Output rise time	1	1	—	4	ns
t_f	Output fall time	1	1	—	4	ns

NOTES:

1. Edge rate in the high edge-rate mode.

4.3.4 Switch Setting

Crosspoint functions and options are accessed through hardware terminals, or software via the serial/parallel interface. In some cases, both software and hardware can access the same function. This section describes these functions in detail and Table 3-1 lists register functions.

The setting parameters are summarized in Table 3-1, which contains the allowable addresses for the M21131/M21151 crosspoint switch. The INCHSEL#n register controls the crosspoint connectivity. Its register address, INCHSEL#n, is mapped to the output channel number and its associated data is the input connected to the output N. Output channels 0 through 71/0 through 143 are mapped to register addresses = 00h through 37h/00h through 8Fh with the output N = address.

For example, if register address = 05h and DATA = 02h (5h = 02h), then output #5 gets input #2. Any output can be routed to the internal PRBS receiver input and the internal PRBS transmitter output can be routed to any of the inputs. To Read the current switch state (CSS) of the ACL, the selected channel is specified by register address and the resulting data is the input channel number routed to the selected output. The Next Switch State (NSS) in the ICL, if different from the ACL, cannot be read back. The default state after power on is channel 0 broadcast to all outputs (all registers cleared).

4.3.5 Input/Output Enable and Output Logic Swing

The inputs and outputs have both a hardware global enable and a software global enable as well as individual I/O software controls.

Terminals XINDIS and XOUTDIS control the inputs and outputs, and are active low (disabled) with internal pull-downs (100 KΩ). When terminals XINDIS = L and/or XOUTDIS = L all inputs and/or outputs are globally disabled, respectively (default). Hardware disable has priority over all software controls. If the I/Os are not disabled via the hardware terminals, XINDIS and/or XOUTDIS = H, then the IOENABLE register selects the control status. With IOENABLE[4] = 0 (default), the software global enable/disable bits (IOENABLE[1:0] for global input) and

(IOENABLE[3:2] for global output) are selected. The individual global input and output register values default to disable.

With IOENABLE[4] = *1*, the 72/144 CHANCFG#n registers control the enable/disable status of each channel input and output buffer. The CHANCFG#n address is computed with N+100h, with the variable N mapped to both the input and output channel. Consequently, CHANCFG#n[3:2] controls the enable/disable status of output N, and CHANCFG#n[1:0] controls the enable/disable status of input N. With IOENABLE[4] = 1, IOENABLE[3:2] and IOENABLE[1:0] have no meaning.

For both inputs and outputs, a disabled state implies turning off the current sources of the I/O buffer to save power. With the built-in pull-up resistors, both “p” and “n” nodes of the differential output will default to the high logic state when disabled; however, the logic levels of the “p” and “n” inputs to the switch core are undetermined.

An additional input signal inhibit function is included in the IN_CHAN_CTRL[3] registers (200h–237h/200h–28Fh) of the M21131/M21151. With IN_CHAN_CTRL[3] = 1, the “p” inputs to the switch core are clamped to a logic low and the “n” inputs are clamped to a logic high.

The output drive level is programmable on either a global or individual basis. With IOENABLE[4] = 0 (default), IOENABLE[3:2] = 00b selects a global default 500 mVp–p differential output level, and IOENABLE[3:2] = 01b selects a global default 900 mVp–p differential output level. With IOENABLE[3:2] = 10b a global 1200 mV differential output level is selected (1200 mV should not be used at AV_{DD}_IO = 2.5 V). With IOENABLE[3:2] = 11b (default) all outputs are disabled. A 500 mVp–p differential output implies a 250 mVp–p single-ended output. With IOENABLE[4] = 1, CHANCFG#n[3:2] selects the output level of each channel individually.

The global enable, disable, and output swing level registers minimize the software setup overhead of the crosspoint switch after resetting; however, individual control of enable/disable and output swing level is provided for maximum flexibility in some applications.

4.3.6 Programmable Input Equalization

In order to compensate for lossy external interconnects, the input buffers include a programmable equalization function. Register CHANCFG#n[6:5] as listed in Table 4-4, controls channel equalization for each input independently.

Table 4-4. Equalization Control Bits

CHANCFG#n[6:5]	Description
00	Minimum EQ (≈ 9 dB)
01	Small EQ (≈ 12 dB) (default)
10	Medium EQ (≈ 15 dB)
11	Large EQ (≈ 18 dB)

4.3.7 Programmable Output De-Emphasis

Similar to input equalization, each output buffer and PRBS transmitter has a programmable output de-emphasis (PE) function included. When enabled, the PE will provide a high frequency boost to the output signal, such that the data eye will be improved (more open) after a long external interconnect.

With IOENABLE[4] = 0 (address BAh), CORECTRL[2] (address BBh) globally enables/disables the PE for all outputs. CORECTRL[2] defaults to 0, PE off. The PE for PRBS transmitters are not dependant on IOENABLE[4], i.e., PRBSTXCTRL2_N[5:3] always control PE for the PRBS transmitters. With IOENABLE[4] = 0 and CORECTRL[2] = 1, PE is globally enabled and CORECTRL[4:3] (address BBh) globally control the PE amplitude and duration for all outputs. The default PE amplitude and duration settings are CORECTRL[4] = 0 and

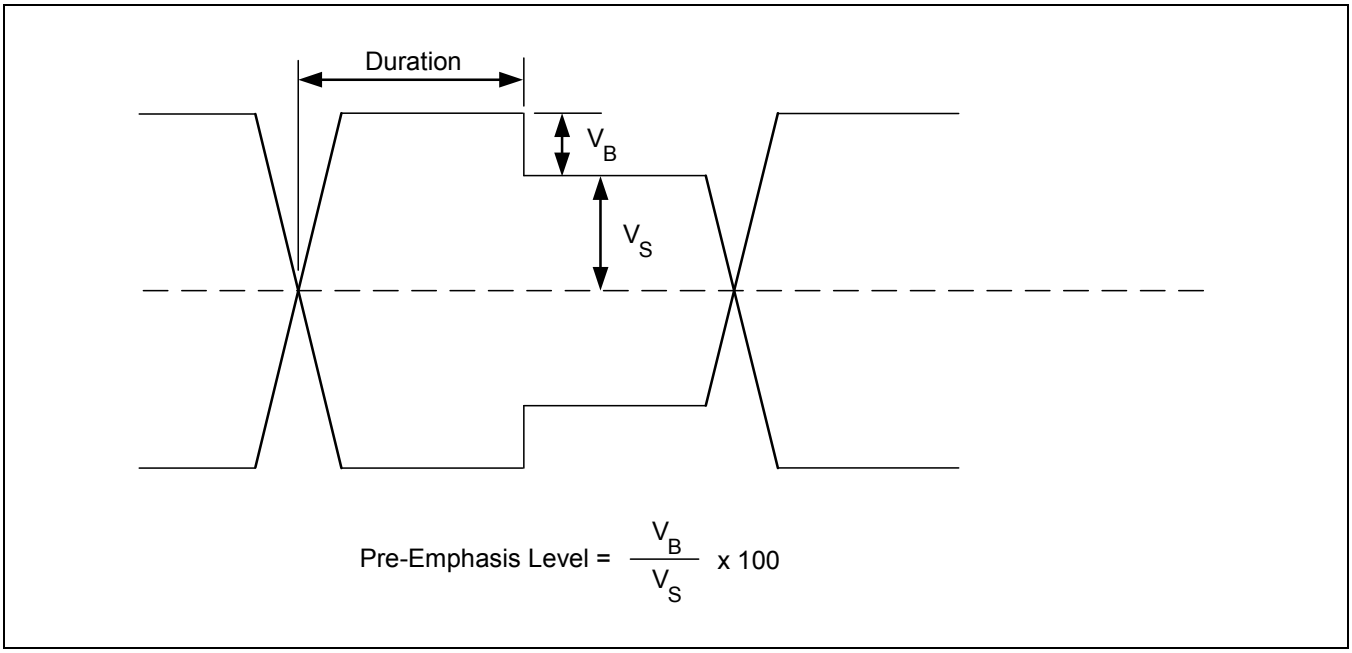
CORECTRL[3] = 1 which globally enable a PE of 50% for a duration of approximately 600 ps (see Figure 4-10). For example, if the output drive level is set for 1200 mV, when there is a data transition (1-to-0 or 0-to-1) the beginning of each pulse will start at 1200 mV and decay to 600 mV in approximately 600 ps. Setting CORECTRL[4] = 1 (PRBSTXCTRL2_N[5] = 1) enables a higher boost of 67%. For example, if the output drive level is set for 1200 mV, the beginning of each pulse will start at 1200 mV and decay to 400 mV. CORECTRL[3] = 0 and PRBSTXCTRL2_N[3] = 0 (default is 1) enable a longer decay time of approximately 1200 ps, corresponding to lower frequency boost. This is for interconnects which exhibit attenuation at lower frequencies.

Table 4-5. De-Emphasis Control Bits

Register BBh[4:3]	Description
00	50% Amplitude, 1200 ps duration.
01	50% Amplitude, 600 ps duration (default).
10	67% Amplitude, 1200 ps duration.
11	67% Amplitude, 600 ps duration.

With IOENABLE[4] = 1 (address BAh), PE on each output is individually enabled/disabled by CHANCFG#n[4]. CHANCFG#n[4] defaults to 0, PE off. The amplitude and duration of the PE on all of outputs are still controlled by CORECTRL[4:3]. The amplitude and duration of the PE on PRBS transmitters are controlled by PRBSTXCTRL2_N[5, 3].

Figure 4-10. Definition of De-Emphasis Levels and Duration



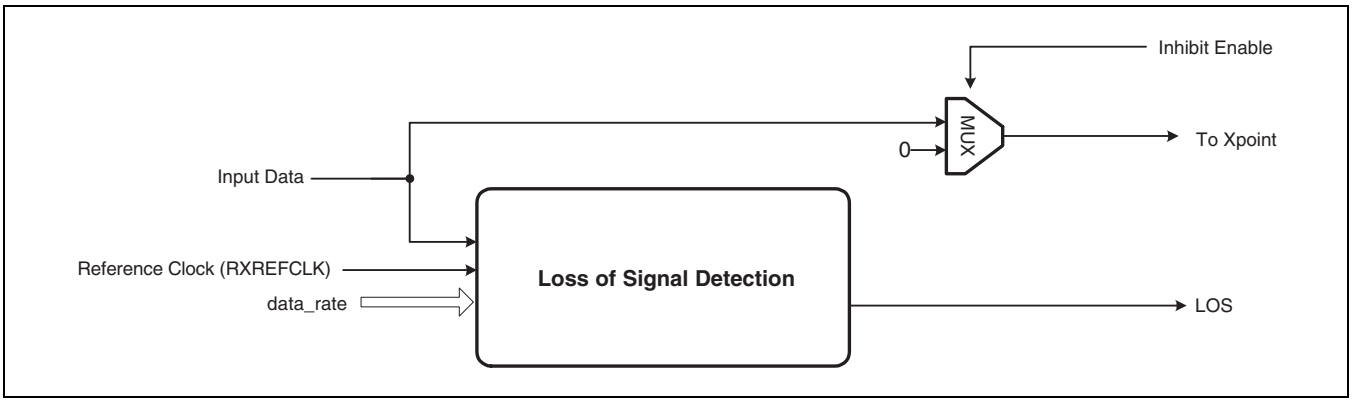
4.3.8 Duty Cycle Distortion (Offset) Circuit on Inputs to Switch

Each input channel has an offset circuit that can be enabled to correct for DC offset. This circuit is designed to correct duty cycle distortion (DCD) that may be present on either a single ended or differential signal at the input of the switch. It also compensates for common mode drift of the input stage over temperature and power supply variation for single ended inputs. When enabled, the offset feature removes DCD thus improving the quality of the data eye pattern. CHANCFG#n[7] at addresses 100h–137h/100h–18Fh enables the offset function.

4.3.9 Input Signal Activity Monitor

For operation at data rates of 1.0 Gbps to 1.6 Gbps and 2.0 Gbps to 3.2 Gbps, a loss of signal (LOS) circuit is included on each input and detects whether valid data is present. The 19.44 MHz RXREFCLK clock must be provided to the M21131/M21151 and the data rate of the signal must be programmed for the LOS feature to function properly. LOS acts as an alarm and can be used to inhibit the signal into the switch core when the data to the input terminal is lost. If the input signal is clamped high or low, or if the difference between the input data rate and the programmed data rate is greater than approximately ±100 Mbps, the LOS alarm will be activated. Whenever valid data is present at the input, the LOS alarm is deactivated. The LOS circuit is disabled if register IN_CHAN_CTRL#[1] = 0 (default 1) (addresses 200h–237h/200h–28Fh). The data rate range is selected using LOS_DR_SEL#n[6] and the data rate is programmed using LOS_DR_SEL#n[5:0] (addresses 300h–337h/300h–38Fh). When register IN_CHAN_CTRL#[3] = 1 (default) a LOS alarm issues an inhibit signal which forces the switch input to a low state. This minimizes any noise propagating to the switch in the LOS condition.

Figure 4-11. LOS Architecture



4.3.9.1 LOS Data Rate Programming

The LOS circuit for each input channel operates independently and employs an external 19.44 MHz clock reference, RXREFCLK. The LOS circuit can be programmed to any rate between 2.0 GHz and 3.2 GHz or between 1.0 GHz and 1.6 GHz using register LOS_DR_SEL#n[6:0] (300h–337h/300h–38Fh). To select a desired rate, it is necessary to set LOS_DR_SEL#n[6:0] to the value closest to the desired rate. For example if 2.64 GHz is the desired rate: LOS_DR_SEL#n[6] = 0 and the code to be selected (LOS_DR_SEL#n[5:0]) is 100010 (136d), which corresponds to 2.6438 GHz. The programmed frequency is exactly equal to the reference frequency multiplied by the decimal equivalent of the binary value programmed in register LOS_DR_SEL#n[5:0] + 102d. For 1.0 Gbps to 1.6 Gbps operation, the dr_range bit, LOS_DR_SEL#n[6] must be set to 1. This bit causes the multiplier set by LOS_DR_SEL#n[5:0] to be divided by two.

Table 4-6. Allowed Data Rates with 19.44 MHz External Reference

RXCDR_CTRLB_N[5:0]	Notes	Bit Rate in Gbps	Multiplier
000000	1	1.983	102
000001	1	2.002	103
000010		2.022	104
…		…	…
011010		2.488	128
…		…	…
111111	1	3.208	165

NOTE:

1. For decimal multiplier values which are not 104, 112, 120, 128, 136, 144, 152, or 160, more programming steps are required and are outlined in the “Settings for Non-Standard Rates” section and Table 4-7.

4.3.9.2 LOS Signal Busing

Although each input channel has an individual LOS alarm, the alarms for all of the channels are wired OR on chip to create the global LOS alarm; therefore, an active LOS from one or more channels will generate a logic high on the global LOS terminal and set an alarm bit. The alarm bit can be immediately read from los_statn[7:0]. Toggling register GLOBAL_CTRL[0] from 0 to 1 then back to 0 will clear all alarm bits (unless a particular alarm persists, in which case this bit will remain high).

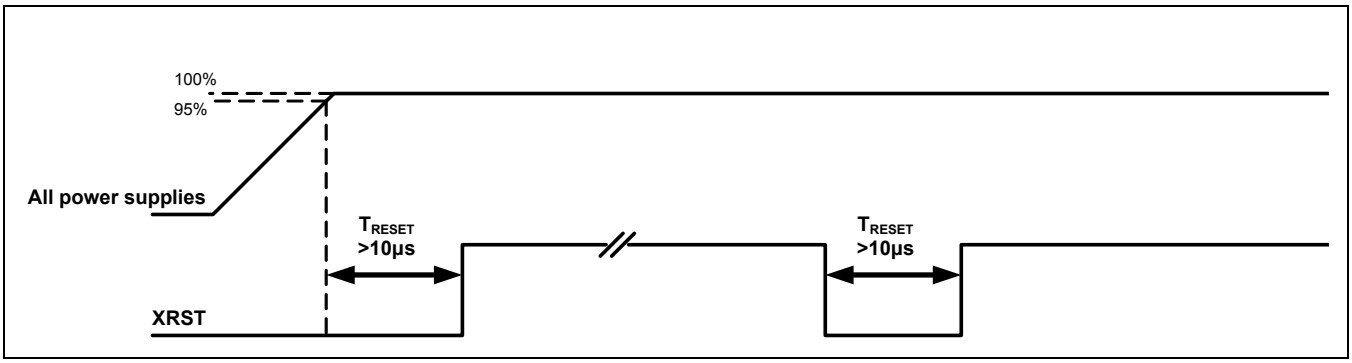
4.3.10 Power-Up Sequence and Device Reset

There are no power supplies sequence requirements for the M21131/M21151. Proper hardware reset assertion will ensure that the device will operate properly regardless of power supply sequence.

The XRST terminal is a hardware reset to be used after power-up or as a general reset. Before and during power-up, XRST must be set LOW.

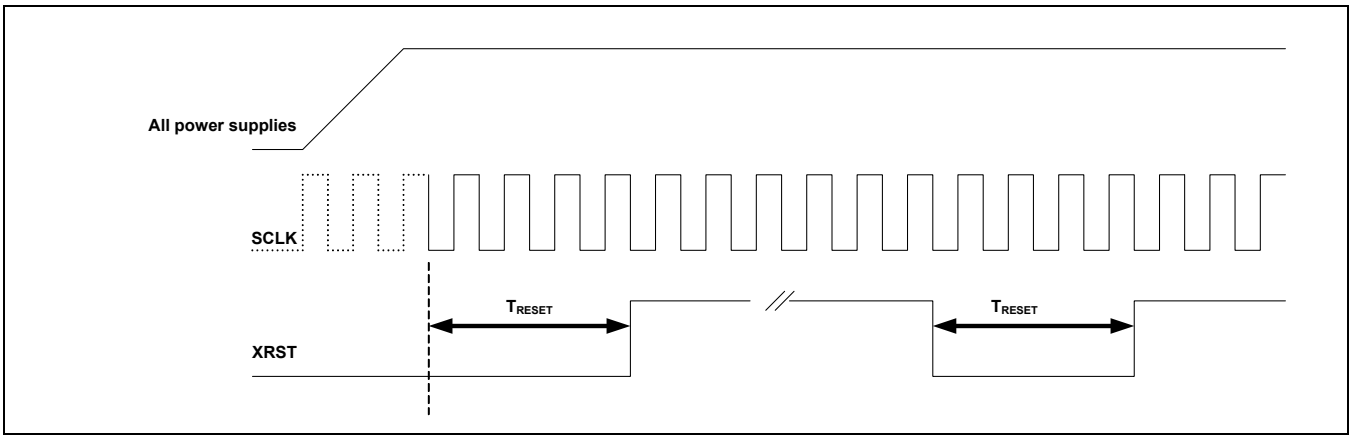
If the device is configured to use the parallel interface for programming the registers, then upon device power-up, the XRST terminal must be held LOW for a minimum of T_{RESET} = 10 µs after all power supplies have reached the expected voltage level. Once XRST is set HIGH following T_{RESET}, the device reset is complete. Any hardware reset of the device after power-up can be achieved by setting terminal XRST LOW for T_{RESET} > 10 µs and returning it to HIGH.

Figure 4-12. Reset Timing in Parallel Programming Mode



If the device is configured to use the serial interface for programming the registers (SPI), then a valid SPI clock (SCLK) must be present at the time of reset. The XRST terminal must be held LOW for a minimum of T_{RESET} >= 4 SCLK cycles, after a valid clock signal is applied. Once XRST is set HIGH following T_{RESET}, the device reset is complete. Any hardware reset of the device after power up can be achieved by setting terminal XRST LOW for at least T_{RESET} > 4 SCLK cycles and returning it to HIGH.

Figure 4-13. Reset Timing in Serial Programming Mode



Following reset, the device will be in the following condition:

- All registers will be set to the default values.
- A software global disables of all input and output channels will be asserted (through the I/O enable register).
- Input channel 0 will be broadcast to all outputs (the ICL and ACL are cleared).
- The PRBS TX and RX will be disabled.
- All error flags will be cleared

If XTEST = L after reset, all inputs and outputs are globally enabled and the switch is set with channel 0 broadcast to all outputs. Mindspeed uses these features for internal die testing, but for normal operation, terminals XTEST = H and XRST = H. To enable a software reset, two consecutive writes to the SOFTRESET register (address, BFh) value (AAh) are required. If the second write is not to the SOFTRESET register, the register will be cleared and two additional consecutive writes of (AAh) will be needed to enable a software reset. Hardware reset has priority over software reset. A third write of any value is required to bring the switch out of reset.

4.3.11 Product and Revision Codes

A read to the read-only PRODCODE register causes a readback of the M21131/M21151 product code number. A read to the read-only CHIPREV register causes a readback of the version number of the chip. The contents of these registers can be used by software drivers to determine the appropriate driver routine to be used. See Section 3.1.3 for details.

4.3.12 Core Power Saving

The CORECTRL register enables the core power-saving modes. Register CORECTRL[1] = 0 powers down the switch core and the PRBS TX/RX (default power on).

Register CORECTRL[0] = 1 enables the SmartPower™ core control (default).

SmartPower automatically disables portions of the core mux circuitry that are not active for certain switch configurations. This results in a significant power savings compared to operations when the core mux is fully powered. The actual power savings will vary across configurations.

Enabling SmartPower will slightly increase the settling time of the device when a new switch core configuration is implemented, so for applications where the minimum configuration time of the switch is desired, SmartPower should be disabled. Most applications will use the M21131/M21151 with SmartPower enabled.

4.3.13 PRBS Transmitter and Receiver

Internally, the switch core input terminals (INP and INN) and output terminals (OUTP and OUTN) are grouped into odd and even sections, as shown in the PRBS TX and RX Functional Block Diagram, Figure 4-14. Likewise, there are two PRBS transmitter (TX) and receiver (RX) sections:

An odd (1) section which operates with the odd numbered Inputs (INP1, 3, 5, etc. and INN1, 3, 5, etc.) and Outputs (OUTP1, 3. 5, etc. and OUTN1, 3, 5, etc.)

An even (0) section which operates with the even numbered Inputs (INP0, 2, 4, etc. and INN0, 2, 4, etc.) and Outputs (OUTP0, 2, 4, etc. and OUTN0, 2, 4, etc.).

As a result, there are two sets of PRBS control terminals, interface terminals and control registers. See Table 3-1, Register Summary, (addresses A0 – B7) for additional information.

The references to PRBS control registers in this section apply to either the odd or even PRBS registers. As an example:

Terminal DOTXP/N[1] is the PRBS TX output of the odd (1) section and can only be routed to the odd numbered inputs. If an even numbered input is selected for PRBSTXCHSEL_ODD[7:0], the PRBS TX output will not be connected to any odd numbered input (to connect a PRBS signal to an even numbered input, the even (0) PRBS TX section must be enabled and the PRBSTXCHSEL_EVEN[7:0] register must be properly programmed).

Similarly, the even (0) PRBS RX section can only accept even numbered outputs (OUTP0, 2. 4, etc.). If an odd numbered output is selected for the even (0) PRBS RX, no PRBS output signal will be connected to the even (0) PRBS RX block (invalid output).

Also, note that since the RX and TX functions are completely duplicated, they can be used simultaneously in parallel. For instance, PRBS signals can be simultaneously routed into input 1 and input 71/input 1 and input 143. These two PRBS signals can then be switched to any even and any odd outputs, respectively. The respective odd and even outputs that were selected can be connected to the PRBS RX blocks. The PRBS TX and RX sections operate from 1.0 Gbps to 1.6 Gbps and 2.0 Gbps to 3.2 Gbps.

4.3.13.1 PRBS TX Pattern Generation

The 2^{23}-1 PRBS TX (with polynomial D23+D18+1) provides a NRZ PRBS pattern. The PRBS TX is enabled with register PRBSTXCTRL1[3] = 1 (default 0) or with terminal XENTX = L (CMOS level, internal pull-up). An asynchronous reset can be performed by setting PRBSTXCTRL1[4] = 1 and then bringing it low again. The data rate is determined by the external clock on terminal CLKTXP/N (PCML), by an external reference clock CLKTXREF (~19.44MHz, CMOS level) or by the recovered clock from the PRBS RX block, which is derived from its preceding CDR).

Register PRBSTXCTRL1[6:5] = 10b (default) selects the high-speed clock input, PRBSTXCTRL1[6:5] = 00b selects the low-frequency reference clock input and PRBSTXCTRL1[6:5] = 01b selects the recovered PRBS RX clock. For the case where an external low frequency clock is provided, register PRBSTXCTRL1[1] = 0 enables the TX PLL and PLL_CTRLB[6:0] sets the actual internal clock frequency into the PRBS TX. For a 19.44 MHz

reference input, the PLL output frequency programming is described in "PRBS CDR Control Parameters" on page 59. Register PLL_CTRLB[7] provides a PLL software reset if required.

4.3.13.2 Additional Test Patterns

The PRBS TX can also output a 0101 or a 0011 pattern. By setting register PRBSTXCTRL2[1] = 1 (default 0) this mode is selected. If PRBSTXCTRL2[2] = 1 then a 0011 pattern is generated otherwise a 0101 pattern is created (default).

4.3.13.3 PRBS Output Data

The output data is updated with each rising edge of CLKTXP. The output terminal Trig (CLKTXP/N divided by 16) is used as a scope trigger to observe the 2^{23}-1 pattern and can be disabled with Register PRBSTXCTRL2[0 = 0 (default). It is a single ended PCML output with 50Ω on chip source termination and 450 mVp–p single ended swing into an external 50Ω load.

The PRBS TX data can be observed at terminals DOTXP and DOTXN (PCML output with 50Ω on chip source termination and 900 mVp–p differential swing into an external 50Ω load) and can be routed internally to any of the inputs. When routing PRBSTX through the crosspoint core, DOTXP/N needs to be terminated with 50Ω load.

Register PRBSTXCTRL1[2] = 0 disables the PRBS TX output to be routed to any input; with PRBSTXCTRL1[2] = 1 (default).

Register PRBSTXCHSEL[7:0] selects the input to which the PRBS TX will be routed. Input channel N is selected by setting PRBSTXCHSEL[7:0] = Nh. If an invalid input is selected (N>71/143), then the PRBS TX will not be routed to any input.

Note that the PRBS TX signal will be forced into the input terminals (the on-chip PRBS buffers are operating in current mode); a portion of the PRBS signal will egress from the input terminal to which the PRBS transmitter is connected. The device normally connected to these terminals may need to be powered down (it is acceptable to have the 50Ω source termination still present) or temporarily disconnected during PRBS operation.

4.3.13.4 PRBS RX Control Parameters

A 2^{23}-1 PRBS RX takes in a NRZ PRBS pattern (with polynomial D23+D18+1) and checks for any bit errors. The PRBS RX includes an integrated CDR which uses RXREFCLK as a low-speed reference clock.

The PRBS RX will be enabled with register PRBSRXCTRL[3] = 1 (default 0) or with terminal XENRX = L (CMOS level, internal pull-up). When enabled, the PRBS RX takes its input directly from any of the odd or even core outputs as enabled by PRBSRXCTRL[5] = 0, or from external inputs DIRXP/N enabled by PRBSRXCTRL[5] = 1 (default).

Register PRBSRXCTRL[2] = 0 prevents any of the core outputs from being connected to the PRBS RX. If register PRBSRXCTRL[2] = 1 (default), then PRBSRXCHSEL[7:0] selects which core output channel goes to the PRBS RX. In either case, the input to the PRBS RX is first routed into a dedicated CDR to resample the data and to extract a clock for the PRBS RX. Register PRBSRXCTRL[1] = 0 (default 1) enables the CDR.

4.3.13.5 PRBS CDR Control Parameters

Register CDR: RXCDR_CTRLB[6:0] controls the desired bit rate, and CDR: RXCDR_CTRLB[7] provides a means for a software reset. The CDR must be in lock before valid data can be passed on to the actual PRBS RX circuit. Register RXCDR_ALARMS[1:0] contain the normal CDR alarms; these bits need to be 0 for the PRBS RX to produce valid error counts. For this reason the PRBS RX needs to remain in reset while the CDR is acquiring lock. This can be done by setting register XRSTRX = L (CMOS level, internal pull-up) or with PRBSRXCTRL[4] = 1 (default 0).

The operation of the CDR for the PRBS RX section is controlled through the PRBS RX CDR Control A and Control B registers (addresses A4h, A5h, B0h, and B1h). The CDR for the PRBS RX can be reset through RXCDR_CTRLB[7]. This bit must be set to a 1 and then set back to a 0 to issue a software reset. The LOS circuit for the PRBS RX CDR can be enabled/disabled with RXCDR_CTRLA[1]. Bits 5, 4, 3, 2, and 0 of this register are Mindspeed reserved bits and should not be used. Bits 5, 4, and 3 should be set to 0 and bits 2 and 0 should be set to 1.

4.3.14 PRBS CDR Data Rate Programming

For the CDR to achieve a correct frequency acquisition, a frequency acquisition loop is present. The frequency acquisition loop employs an external clock reference, REFCLK. The external reference clock frequency should be 19.44 MHz ±50 ppm. The CDR is able to lock the VCO to any rate between 2.0 GHz and 3.2 GHz or from between 1.0 GHz and 1.6 GHz using register RXCDR_CTRLB_N[6:0] (A5h and B1h). To select a desired rate, it is necessary to set RXCDR_CTRLB_N[6:0] to the value closest to the desired rate. For example if 2.64 GHz is the desired rate: RXCDR_CTRLB_N[6] = 0 and the code to be selected (RXCDR_CTRLB_N[5:0]) is 100010 (136d), which corresponds to 2.6438 GHz. The programmed frequency is exactly equal to the reference frequency multiplied by the decimal equivalent of the binary value programmed in register RXCDR_CTRLB_N[5:0] + 102d. For 1.0–1.6 GHz operation, the half rate bit, RXCDR_CTRLB_N[6] must be set to 1. This bit causes the multiplier set by RXCDR_CTRLB_N[5:0] to be divided by two.

The Frequency Acquisition Loop is activated if the frequency difference between VCO (divided down) and the external reference clock is more than a certain value called Frequency Window. More precisely, if ***LOL*** = H this value is called Narrow Frequency Window (NFW) and when ***LOL*** = L it is called Wide Frequency Window (WFW) (WIN_INLCK_LOL[7:0]/WIN_OUTLCK_LOL[7:0]) (addresses C3h/C4h). The WFW is typically larger then NFW to provide hysteresis for the locking process. With CDRX_CTRLA[3] = 1 (default) a LOL alarm issues the CDR inhibit which forces the CDR output to a low-logic state. When ***LOL*** = L the frequency acquisition loop is turned off to reduce jitter generation and to optimize phase lock. A Frequency Window Detector determines whether the VCO frequency is inside or outside the Narrow/Wide Frequency Window.

The Narrow Frequency Window and Wide Frequency Window are calculated as follows:

$$NFW = f_{refclk} \cdot \left\{ \frac{1}{(1 \pm \alpha)} - 1 \right\}, \quad with \quad \alpha = \frac{w\_inlk}{ref\_strt}$$

$$WFW = f_{refclk} \cdot \left\{ \frac{1}{(1 \pm \alpha)} - 1 \right\}, \quad with \quad \alpha = \frac{w\_inlk}{ref\_strt}$$

The default values for the narrow and wide window are 03h and 1Eh, which corresponds to 100 ppm and 1000 ppm frequency windows. The frequency acquisition time is about 1.65 ms and is limited by the 100 ppm accuracy.

4.3.14.1 Settings for Non-Standard Rates

If a data rate is selected, which does not correspond to a multiplier of 104, 112, 120, 128, 136, 144, 152, or 160, then an additional write sequence is required for proper operation:

1. The VCO counter needs to have a start value different from the default value (00h). To accomplish this, the appropriate value for diff_start from Table 4-7 should be written into RXCDR_CTRLB_N[7:0].
2. RXCDR_CTRLA_N[7:6] should be changed to 11b, i.e., CFh should be written to RXCDR_CTRLA_N[7:0] (initial value can be 00, 01, or 10); this latches the contents of RXCDR_CTRLB_N into a dedicated register.

3. RXCDR_CTRLB_N can be used as defined in the register map in Table 4-6.
4. RXCDR_CTRLA_N[7:6] should be reset back to 00, 01, or 10.

An individual channel soft reset will not clear the results of the diff_start register but this write sequence must be repeated after a hardware reset or power down.

For example, for a data rate of 2.605 Gbps for the even PRBS receive CDR, the multiplier would be 134 and the following register commands would be required:

1. Write data 5Fh into register address A5h
2. Write data CFh into register address A4h
3. Write data 20h into register address A5h
4. Write data 0Fh into register address A4h

The diff_start values as a function of the multiplier ratio are shown in Table 4-7.

Table 4-7. Diff_start Values as a Function of the Multiplier (1 of 3)

Multiplier	Bit Rate in Gbps	RXCDR_CTRLB[7:0] = diff_start[7:0]
102	1.983	7Fh
103	2.002	7Fh
104	2.022	00h (default)
105	2.041	13h
106	2.061	27h
107	2.080	3Bh
108	2.099	4Eh
109	2.119	62h
110	2.138	75h
111	2.158	7Fh
112	2.177	00h (default)
113	2.197	12h
114	2.216	24h
115	2.236	36h
116	2.255	49h
117	2.274	5Bh
118	2.294	6Dh
119	2.313	7Fh
120	2.333	00h (default)
121	2.352	11h
122	2.372	22h
123	2.391	33h
124	2.411	44h
125	2.430	55h

Table 4-7. Diff_start Values as a Function of the Multiplier (2 of 3)

Multiplier	Bit Rate in Gbps	RXCDR_CTRLB[7:0] = diff_start[7:0]
126	2.449	66h
127	2.469	77h
128	2.488	00h (default)
129	2.508	10h
130	2.527	20h
131	2.547	30h
132	2.566	40h
133	2.586	4Fh
134	2.605	5Fh
135	2.624	6Fh
136	2.644	00h (default)
137	2.663	0Fh
138	2.683	1Eh
139	2.702	2Dh
140	2.722	3Ch
141	2.741	4Bh
142	2.760	5Ah
143	2.780	69h
144	2.799	00h (default)
145	2.819	0Eh
146	2.838	1Ch
147	2.858	2Ah
148	2.877	38h
149	2.897	47h
150	2.916	55h
151	2.935	36h
152	2.955	00h (default)
153	2.974	0Dh
154	2.994	1Bh
155	3.013	28h
156	3.033	35h
157	3.052	43h
158	3.072	50h
159	3.091	5Eh
160	3.110	00h (default)
161	3.130	0Ch

Table 4-7. Diff_start Values as a Function of the Multiplier (3 of 3)

Multiplier	Bit Rate in Gbps	RXCDR_CTRLB[7:0] = diff_start[7:0]
162	3.149	19h
163	3.169	26h
164	3.188	33h
165	3.208	3Fh

Because of finite resolution in the diff_start values, the value for WIN_OUTLCK_LOL[7:0] should be changed to at least 0Ah (default is 03h).

If rates are required which correspond to a non-integer multiplier (in between 2 consecutive multipliers), the CDRs can still lock to this input, as long as the closest integer multiplier is selected, and the narrow and wide frequency windows are changed to wider settings. For this purpose, each CDR has 2 individual large frequency window settings (lolwinctrl[1:0]): RXCDR_CTRLA_N[7:6] = 01 selects 2200/2600 ppm for the narrow and wide window of CDRx; RXCDR_CTRLA_N[7:6] = 10 selects 4400/5200 ppm. RXCDR_CTRLA_N[7:6] = 00 (default) selects the global frequency window settings of 100 ppm/1000 ppm (default).

NOTE: If these wide window settings are not selected, a CDR with a data rate in between, for instance 2.488 Gbps and 2.508 Gbps, will never go out of frequency acquisition, since the frequency acquisition loop pulls the VCO to either 2.488 GHz or 2.508 GHz (depending on which multiplier was chosen) and the phase loop will pull the VCO to the exact data rate which is seen as an LOL condition (if the data rate is more than 1000 ppm away from 2.488 Gbps or 2.508 Gbps).

4.3.14.2 PRBS Error Detection

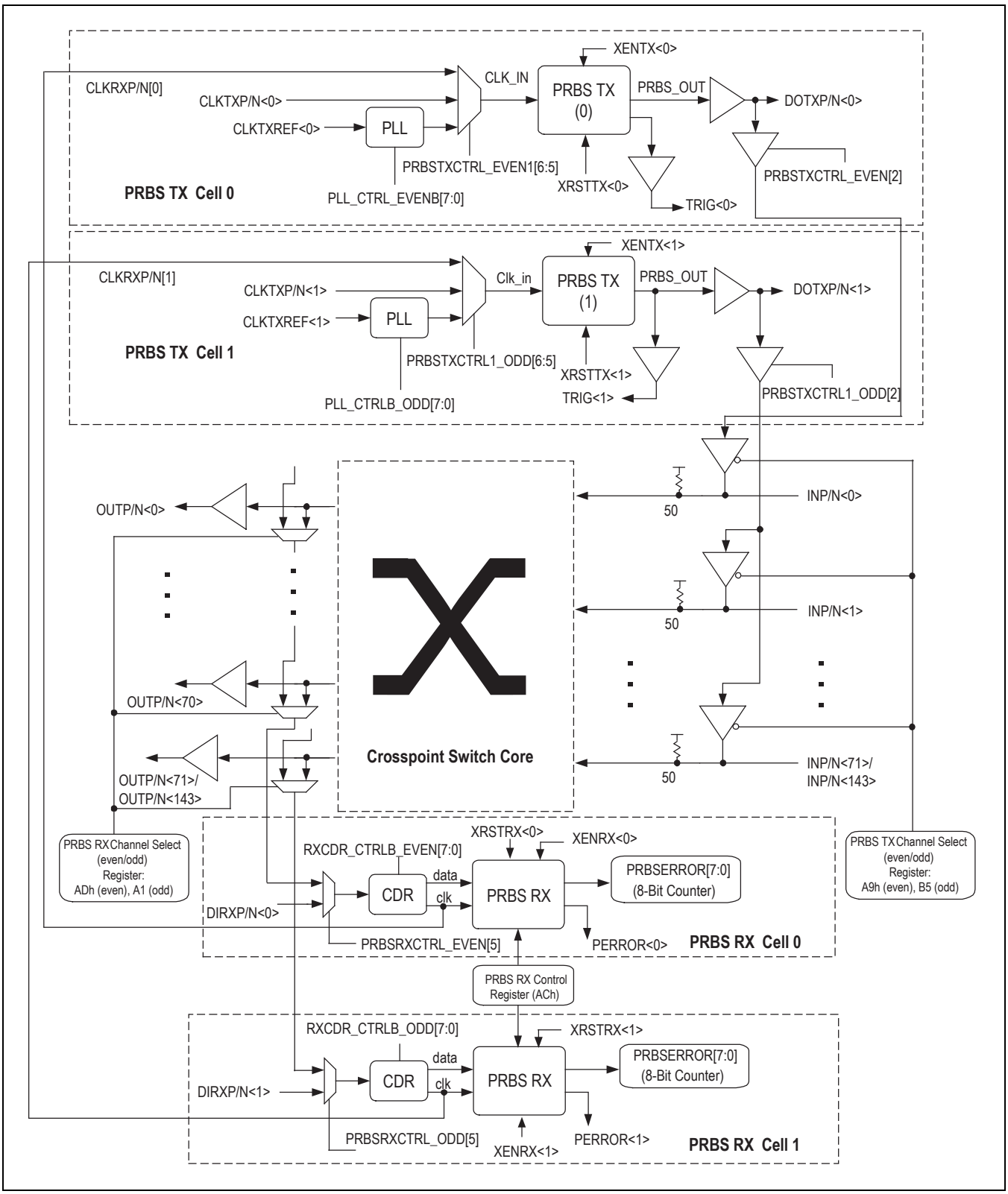
When the PRBS RX detects an error, terminal PERROR will go high. The first and every additional error increments an internal 8-bit counter (PRBSERROR[7:0]). If the number of errors exceeds 255 (counter overflow), the counter will remain at 255 until a hardware or software reset (powering down and then powering up) occurs. Reading the receiver error counter register requires a write of any value to copy the current contents of the error register into the PRBS error register. Subsequently, a read will yield the current error count as of the last write.

While the counter value is being read out, no additional errors will be counted. Upon PRBS reset, the PRBS receiver error counter is cleared and PERROR is reset. Register PRBSERROR[7:0] will always contain the current number of error counts The value divided by the time of the test can be used to calculate a first order estimate of the bit error rate. If there have been more than 255 errors, the PRBSERROR register will always read FFh until cleared.

NOTE: The PERROR terminal is gated with the RXCDR alarms, so that if no stable data is presented to the PRBS receiver (LOS or LOL alarm is high), this terminal will go high and will stay high until all the alarms are cleared and the PRBS receiver error counter is cleared. This enables the PRBS receiver to detect the all zeros case as an error condition.

The PRBS RX can also be configured to detect all patterns that the PRBS TX can generate. Register PRBSRXCTRL[7] = 1 (default 0) selects this mode. The input data has to be a 0101 or a 0011 repeating pattern. If it does not correspond to one of them, errors will be counted.

Figure 4-14. PRBS TX and RX Functional Block Diagram



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