M21050

Duplex Quad (Octal) Multi-Rate CDR (1.0 Gbps - 3.2 Gbps)

The M21050 is a high-performance duplex quad (octal) multi-rate clock and data recovery (CDR) array, optimized for multi-lane datacom applications. Each CDR operates independently at data rates between 1.0 Gbps to 3.2 Gbps, allowing maximum flexibility in system design.

Signal conditioning features include input equalization and output pre-emphasis, allowing robust reception and transmission of signals to other devices up to 60" away.

User-selectable input/output interface types allow coupling to/from CML and InfiniBand. Frequency acquisition is accomplished with an external reference clock. The built-in frequency synthesizer allows multi-rate operation, while operating with a single reference clock.

The device can be controlled either through hardwired pins or an I^2C-compatible interface. The hardwired mode eliminates the need for an external micro-controller, while allowing control of the key features of the device. The I^2C-compatible interface allows complete control of the device features.

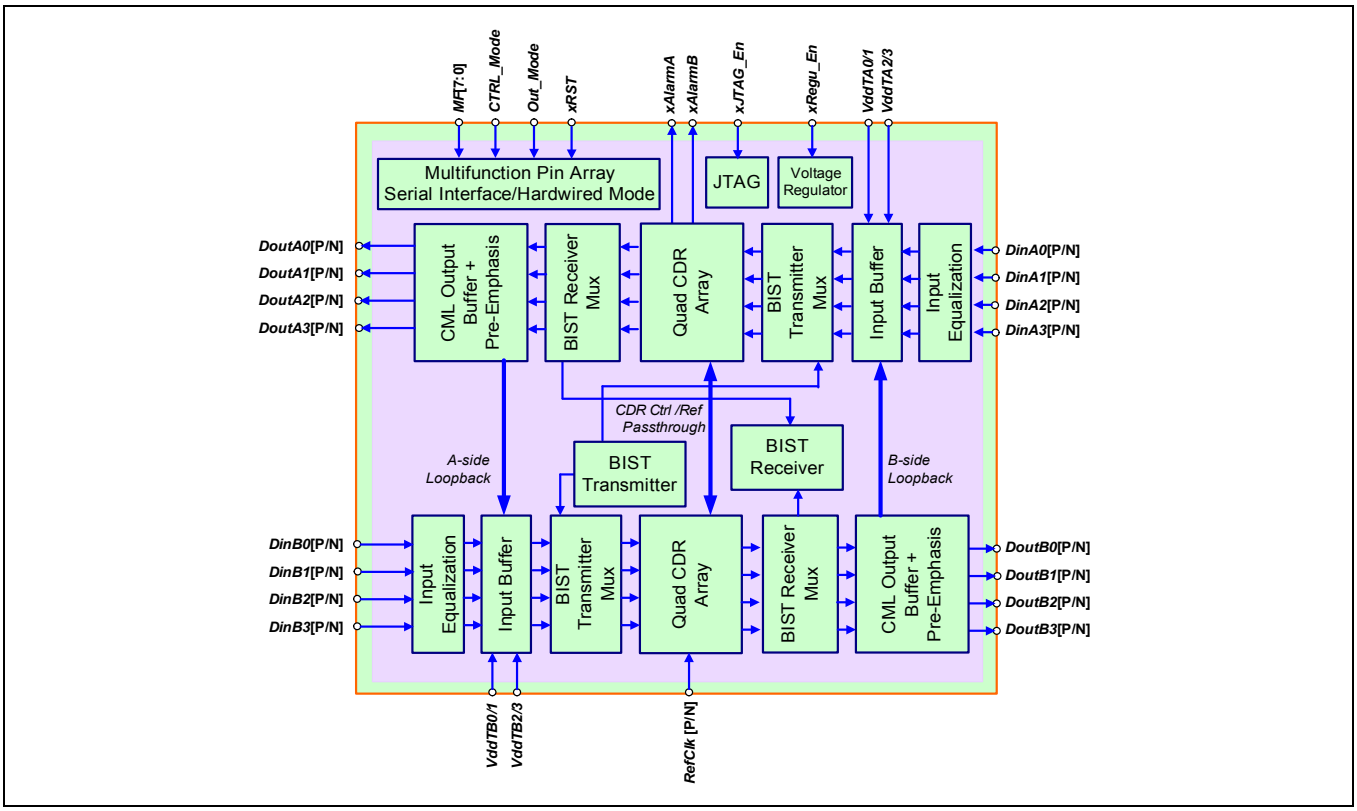
Applications

- Fibre Channel systems
- Gigabit Ethernet systems
- 10GBASE-CX4 systems & modules
- Backplane reach extension
- 1.5 Gbps and 3 Gbps Serial-ATA Systems
- Port Bypass
- Clock Synthesizer
- PCI Express
- InfiniBand systems and modules

Features

- Eight independent CDRs in a duplex quad configuration
- Signal conditioning features on inputs and outputs for trace lengths of up to 60", and cable lengths up to 25m
- Jitter Tolerance 0.625 UI typical
- Interface to CML and InfiniBand
- I^2C-compatible or hardwired control interfaces
- Power consumption as low as 800 mW
- Built-in pattern generator and receiver for module and system testing
- Optimized for PRBS, 8b/10b or similar data patterns

Functional Block Diagram



Ordering Information

Part Number	Package	Operating Data Rate	Operating Temperature
M21050-14	72-terminal, 10mm x 10mm, MLF	1 Gbps - 3.2 Gbps	–40 °C to 85 °C
M21050G-14	72-terminal, 10mm x 10mm, MLF (RoHS compliant)	1 Gbps - 3.2 Gbps	–40 °C to 85 °C

NOTES:

1. The letter "G" designator after the part number indicates that the device is RoHS-compliant. Refer to www.mindspeed.com for additional information.
2. M21050 is the base device number, and -14 is the device revision number.
3. These devices are shipped in trays.

Revision History

Revision	Level	Date	Description
F	Release	September 2006	Updated Table 3-6: V_{OL}, V_{OH}, V_{OD} for all swing levels. Updated Table 3-4: I_{OL}, I_{OH}, t_r, t_f
E	Release	June 2005	Added RoHS compliant model numbers to the ordering information.
D	Release	April 2005	Incorporated all topics/items discussed in product bulletin 21050-PDB-003-A: • FDA mode no longer supported • Changed table of recommended reference clock frequencies • Updated LOA detector window Updated specifications tables with results from electrical characterization: • Included specifications for latency, output data duty cycle, and channel to channel output data skew • Input differential voltage minimum spec increased from 50 mV to 125 mV • Input common-mode voltage minimum spec increased from ***Vss*** to 800 mV • Decreased jitter tolerance specification from 0.65 UI to 0.625 UI • Updated ESD specifications • Updated R_{IN} and R_{OUT} maximum values from 55Ω to 65Ω • Increased DC power dissipation specifications • Increased I_{OL} specifications for two-wire interface • Output data deterministic jitter increased from 115 mUI to 150 mUI • Output data total jitter increased from 215 mUI to 250 mUI Other topics discussed: • Included support of adaptive input equalization • Provided details about programmable input hysteresis (new feature) • Renamed pin ***Out_Mode0*** as ***Out_Mode*** and set ***Out_Mode1*** as N/C • Updated phase loop bandwidth settings
C	Preliminary	December 2003	New document format, major rewrite to incorporate design changes and add content.
B	Preliminary	July 2003	Change temperature range from 0° to 85°C to -40° to 85°C
A	Preliminary	December 2002	Preliminary release

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1.0 Functional Description

1.1 Detailed Feature Descriptions

1.1.1 Conventions

Throughout this data sheet, physical pins will be denoted in ***bold italic*** print. An array of pins can be called by each individual pin name (e.g. ***MF0***, ***MF1***, ***MF2***, ***MF3***, and ***MF6***) or as an array (e.g. ***MF*** [6,3:0]). The M21050 control is accessed through registers that employ an 8-bit address and an 8-bit data scheme. Registers are denoted in italic print, e.g. *TestRegister* and individual bits within the register will be called out as *TestRegister* [4:3] to denote the 4th and 3rd bit where bit 0 is the LSB and bit 7 is the MSB. Many features are bit mapped within a register; if the status of the other bits are uncertain, it is recommended that the user reads the value from the register before writing, to assure only the desired bits change. Writing in the same value to the bits within a register does not cause glitches to the unchanged features. The address for the register as well as its functions can be found in detail in Section 2.0. The purpose of the text description is to highlight the features of the register. For redundant items, such as the channel number, the registers will have a nomenclature of *TestReg*_0 for channel 0, *TestReg*_1 for channel 1. For general reference, the text will denote such registers as *TestReg*_N where N can vary from 0 to 7.

1.1.2 Reset

Upon application of power, the M21050 automatically generates a master reset. At any time, forcing ***xRST*** = L causes the M21050 to enter the master reset state. A master reset can also be initiated through the registers in the two-wire interface control mode by writing AAh to *Mastreset*. Once a master reset is initiated, all registers are returned to the default values, the internal state machines cleared, and all CDR/BIST reset to the out-of-lock condition. After a reset, the register *Mastreset* will automatically return to the default value of 00h.

Each individual CDR can be soft reset by setting *CDR_ctrlA*_N[7] = 1 where N = 0 for CDR A0, N = 1 for CDR A1,…,N = 4 for CDR B0,...,N = 7 for CDR B3. The bit should be returned to 0b for normal operation. In this case, the registers that determine the CDR operation options such as data-rate, window sizes, etc., remain unchanged and only the CDR state-machine is reset, resulting in an out-of lock condition.

1.1.3 Internal Voltage Regulator

The digital and analog core are designed to run at 1.2V, however, for operation from 1.8 to 2.5V, an internal linear voltage regulator is provided. ***xRegu_En*** = L enables the voltage regulator which uses ***AVdd_I/O*** and ***DVdd_I/O*** to generate the required 1.2V for ***AVdd_Core*** and ***DVdd_Core***. In this mode, the ***AVdd_Core*** and ***DVdd_Core*** pins should be connected to a floating DC low inductance PCB plane, and AC bypassed to ***Vss*** using standard decoupling techniques. If desired, ***AVdd_Core*** and ***DVdd_Core*** can be separated into individual planes. If 1.2V is available, it can be connected directly to ***AVdd_Core*** and ***DVdd_Core,*** to save power, by bypassing the internal linear regulator with ***xRegu_En*** = H. In this case, it is recommended that the ***AVdd_Core*** and ***DVdd_Core*** pins be tied together to a common PCB plane, and bypassed to ***Vss*** with standard decoupling techniques.

1.1.4 High-Speed Input/Output Pins

The high-speed input data interface can support PCML and InfiniBand (AC-coupled). The high-speed serial differential data (1 Gbps to 3.2 Gbps) enters the CDR via ***Din*** [B3:A0,P/N]. Inputs A0 and A1 (B0 and B1) are internally terminated with 50Ω to ***VddTA0/1 (VddTB0/1)*** and inputs A2 and A3 (B2 and B3) are terminated with 50Ω to ***VddTA2/3 (VddTB2/3)***. ***VddT*** must be tied to ***Vdd_Core*** and decoupled to ground with high frequency capacitors. ***VddT*** must be a low-impedance node since it is shared between inputs, which requires either a low impedance plane or bypass capacitors.

The M21050 supports the following high-speed output modes: DC-coupled PCML, and AC-coupled InfiniBand. The output modes are selectable with a hardwired pin only, ***Out_Mode***, and the output can be globally enabled or disabled with ***MF7*** as shown in Table 1-1. In the two-wire interface mode, the *Out_ctrl*_N[7:6] register is used to set the data level, and ***Out_Mode*** is used to set the interface type. In the two-wire interface mode, the data output can be enabled with *Out_ctrl*_N[2] = 1b (default), and the output data polarity can be flipped by setting *Out_ctrl*_N[3] = 1b (default: no inversion). Note that N goes from 0 to 7 to map I/O for A0...A3, B0...B3. Output data polarity flip is an internal function that would have the same effect as switching the P and N terminals. In addition to software control via the two-wire interface, the output data polarity can also be flipped by pulling the pins ***MF*** [6:5] low, as shown in Table 1-4. The recommended ***AVdd_I/O*** for the different outputs is shown in Table 1-2.

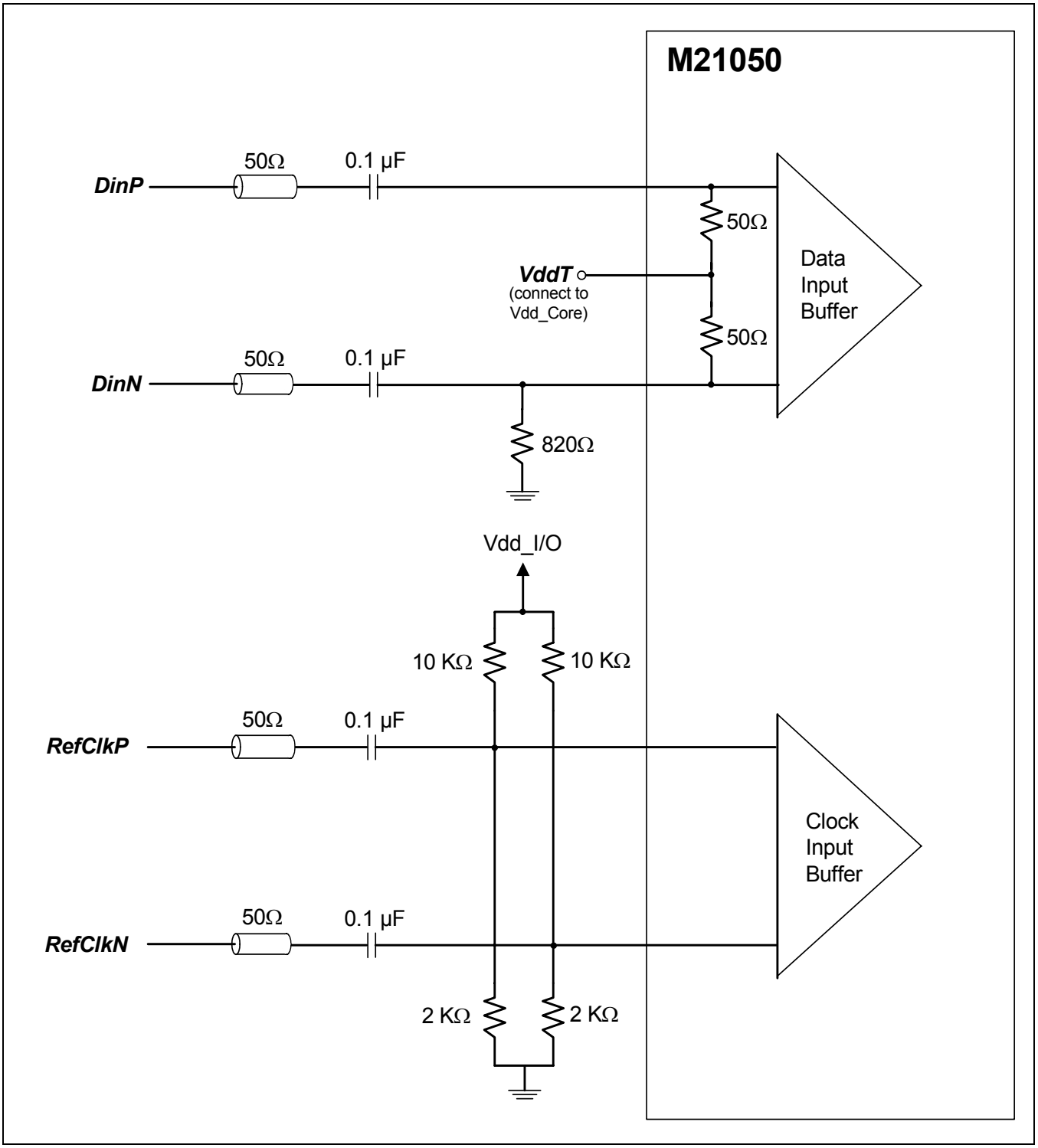
Table 1-1. Output Interface and Level Mapping

Multifunction Pin ***MF7***	**PCML Mode** ***Out_Mode*** **= 0b**	**InfiniBand Mode** ***Out_Mode*** **= 1b**
0b	Off	Off
1b	1000 mV	1600 mV

Table 1-2. Output Interface and Recommended AVdd_I/O Range

Output Logic	***AVdd_I/O*** **Range (V)**
Off	1.8 - 2.5
PCML 600 mV	1.8 - 2.5
PCML 1000 mV	1.8 - 2.5
PCML 1300 mV	1.8 - 2.5
InfiniBand 1600 mV	1.8 - 2.5

Figure 1-1. Recommended Data and Reference Clock Input Coupling Circuitry



1.1.5 CDR Reference Frequency

The CDR frequency acquisition requires the use of an external reference clock. An external reference clock is applied to ***RefClk*** [P/N] to enable frequency reference acquisition (FRA) in the CDR. PCML, LVTTL, CMOS are examples of the wide variety of interfaces supported for the reference clock. The inputs contain a DC-coupled 100Ω differential termination between ***RefClkP*** and ***RefClkN*** along with a 100 kΩ pull-down on each terminal to ***Vss***. After this termination/pull-down block, the inputs are AC coupled internally. The common-mode and allowable voltage swings are specified in Table 3-11. The ***RefClk*** common-mode must be above 250 mV, which may require external pull-ups, in the case of external AC-coupling.

1.1.6 Multifunction Pins Overview

The M21050 is designed to be an extremely versatile device, with many user-selectable options in the CDR and I/O to optimize performance. All of these options can be accessed and controlled through the serial interface. The serial interface is a two-wire interface that is compatible with industry standard I^2C, and shall be referred to as the two-wire interface. When selected, the two-wire interface I/O pins and address pins are mapped to the multifunction pins ***MF***[7:0]. A subset of the key features for most applications, such as standard data-rates, I/O level, etc., can be selected through ***MF***[7:0] in the hardwired option, which does not require use of any serial interface. In this mode, upon power up (auto reset on power up), the M21050 function is determined by the status of the physical hardwired pins. During operation, the hardwired pins can change states, which would cause the CDR to follow with the appropriate action. Another feature of the multifunction pins is to support JTAG testing of this device during PCB manufacturing.

The various control and test modes of this device are selected with two pins: ***CTRL_Mode,*** and ***xJTAG_En***. ***xJTAG_En*** = L overrides ***CTRL_Mode,*** and puts the device in JTAG test mode, while ***xJTAG_En*** = H allows ***CTRL_Mode*** to determine the M21050 control method, as summarized in Table 1-3.

Table 1-3. Mode Select Pins

Pin	JTAG Test Mode	Hardwired Mode	2-Wire Serial
xJTAG_En	L	H	H
CTRL_Mode	no effect	1b	0b

1.1.7 Multifunction Pins Defined for Hardwired Mode

A subset of options in the M21050 can be accessed with hardwired pins, as defined in Table 1-4. The hardwired data-rates, along with the default reference frequency, are shown in Table 1-5.

Table 1-4. Multifunction Pins for Hardwired Mode

Pin	Function	Description
MF0	Data-Rate 0	CDR Rate Select (See Table 1-5 for description)
MF1	Data-Rate 1	CDR Rate Select (See Table 1-5 for description)
MF2	Data-Rate 2	CDR Rate Select (See Table 1-5 for description)
MF3	A-side equalization and B-side pre-emphasis enable	H = Disabled L = A-side input equalization enabled, and B-side output pre-emphasis enabled
MF4	B-side equalization and A-side pre-emphasis enable	H = Disabled L = B-side input equalization enabled, and A-side output pre-emphasis enabled
MF5	A-side polarity flip	H = Normal data polarity L = Inverted polarity
MF6	B-side polarity flip	H = Normal data polarity L = Inverted polarity
MF7	Output Level	L = All outputs powered down H = All outputs on: nominal output level. Output type selected with ***Out_Mode***

Table 1-5. Hardwired Data-Rates and Associated Reference Clock Frequencies

Pins ***MF*** [2:0]	Application	Signal Data-rate (Gbps)	Reference Frequency (MHz)
000	10x Fibre Channel - XAUI	3.1875	159.375
001	10 Gigabit Ethernet - XAUI	3.125	156.25
010	InfiniBand	2.5	62.5
011	STS-48	2.48832	19.44
100	InfiniBand	2.5	250
101	2x Fibre Channel	2.125	106.25
110	Gigabit Ethernet	1.250	125
111	1x Fibre Channel	1.0625	106.25

1.1.8 Two-Wire Serial Interface

The two-wire interface is compatible with the I^{2}C standard. The M21050 supports the read/write slave-only mode; 7-bit device address field width (3 MSB fixed to 001b and 4 LSBs set with ***MF*** [3:0]), and supports the standard data rate of 100 kbps, fast mode of 400 kbps, and high-speed mode of 3.4 Mbps. SDA (***MF5***) and SCL (***MF4***) can drive a maximum of 500 pF each at the maximum data-rate. During the write mode from the master to the M21050, data is latched into the internal M21050 registers on the rising edge of SCL, during the acknowledge phase (ACK) of communication. Table 1-6 summarizes the multifunction pins for the two-wire interface. For further information on timing, please see the I ^{2}C bus specification standard.

Table 1-6. Multifunction Pins for Two-Wire Interface

Pin	Function	Description
MF0	Address bit 0	7-bit device address; address bit 0 is LSB, address bit 6 is MSB
MF1	Address bit 1	
MF2	Address bit 2	
MF3	Address bit 3	
MF4	SCL	Clock input
MF5	SDA	Data input/output (open drain)

1.1.9 JTAG

The M21050 supports JTAG external boundary scan only, which includes all of the high-speed I/O, as well as the digital I/O.

Table 1-7. Multifunction Pins for JTAG

Pin	Function	Description
MF4	TCLK	Test clock
MF5	TDO	Test data output
MF6	TDI	Test data input
MF7	TMS	Test select

1.1.10 Input Deterministic Jitter Attenuators

Each of the eight input channels contains an independent input equalizer (IE). For the IE, the address N is mapped to the input channel. In the hardwired mode, there is the option to set equalization on or off. In the two-wire serial interface control mode, the default state allows for configurable input equalization settings using *Ineq_ctrl*_N[3, 1:0], for which the setting of 100b is optimized for trace-lengths between 10 - 46 inches and twinaxial cable lengths between 5 - 15m.

The input equalization settings have been optimized for a variety of connectivity applications, such as board traces and cables. For PCB, the input equalization settings have been specified to operate up to 60” at 3.1875 Gbps on FR4, and up to 72” on FR4 at 2.125 Gbps. The equalizer has similar high performance on Nelco-13, Arlon 25, Rogers 3003, 4003C, 4340, GeTek PCB materials, and twinaxial cables.

Another component of input deterministic jitter is ISI due to DC offsets. By default, a DC servo-like circuit is enabled to correct for this type of deterministic jitter, and can be disabled by setting *Ineq_ctrl*_N[4] = 0b. The DC servo can also be used to track changes in the common mode for single-ended operation. When the CDR, DC servo, and IE are all enabled, the jitter tolerance should be greater than 1 UI.

In certain datacom applications, such as blade server to blade server connectivity, there arises the need to support twinaxial cable lengths ranging from 1m to 15m and/or PCB trace-lengths ranging from 10 in to 60 in. While an optimal IE setting may be found for a fixed connectivity configuration, if the configuration were to change it may be necessary to select new IE settings. An example of this would be changing the cable length on the port-side of the card from 1m to 15m, and/or plugging the card into a different slot in the chassis effectively changing the PCB trace-length on the host-side of the card from 10 in to 60 in. If the M21050 IE settings cannot be changed when the connectivity configuration is altered, it may be necessary to enable adaptive input equalization (AIE). AIE is enabled by setting register *Ineq_ctrl*_N[2] = 1b. The configurable IE has a wide dynamic range, and should be chosen over AIE whenever possible. Electrical characterization has shown that the performance or AIE is not consistent from device to device, whereas the configurable IE has shown minimal variation in performance. AIE is disabled by setting *Ineq_ctrl*_N[2] = 0b (default), and the optimal configurable IE setting is selected with *Ineq_ctrl*_N[3, 1:0].

Figure 1-2. 2.5 Gbps waveform after transmission through 25m of twinaxial cable (input to M21050)

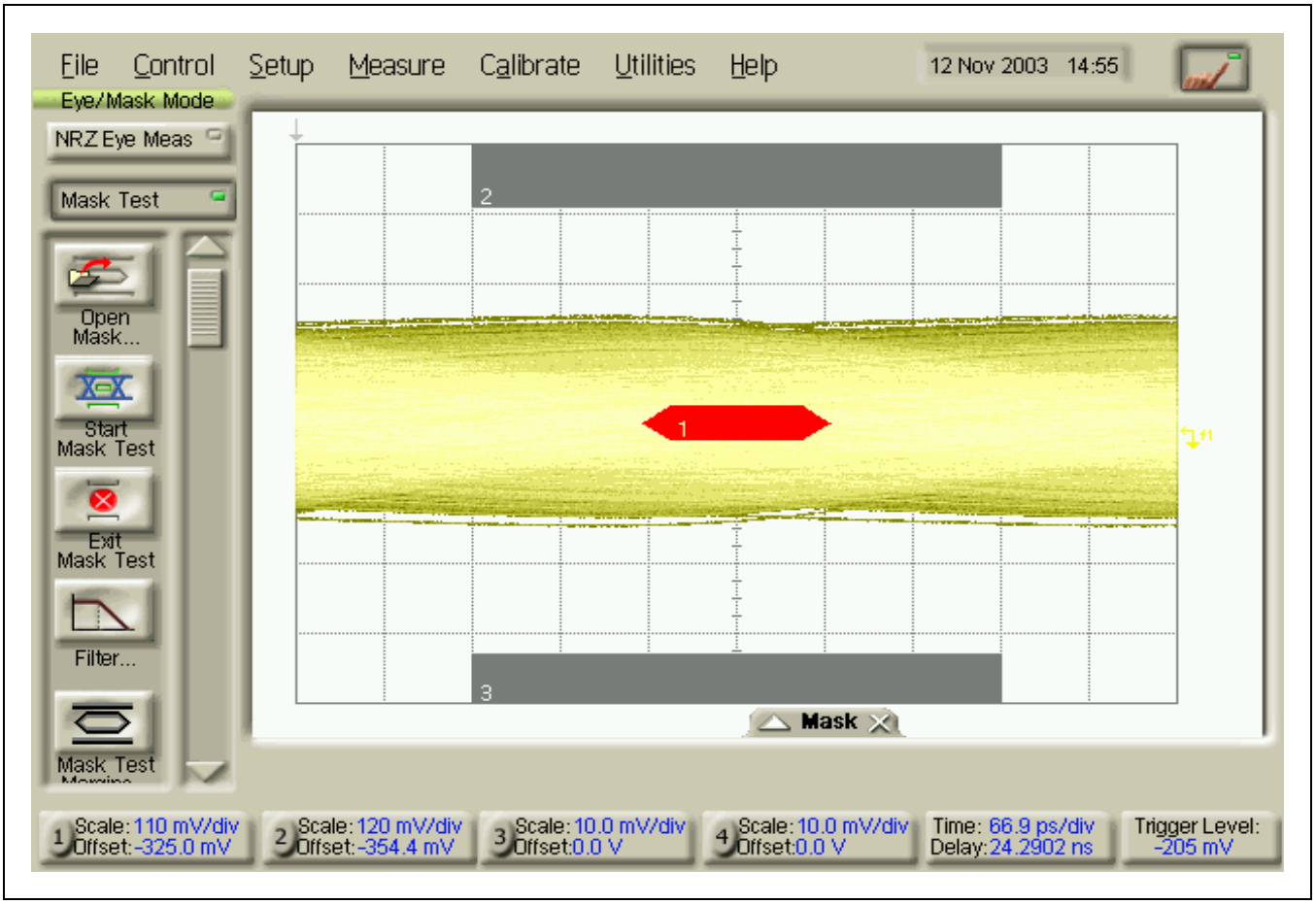
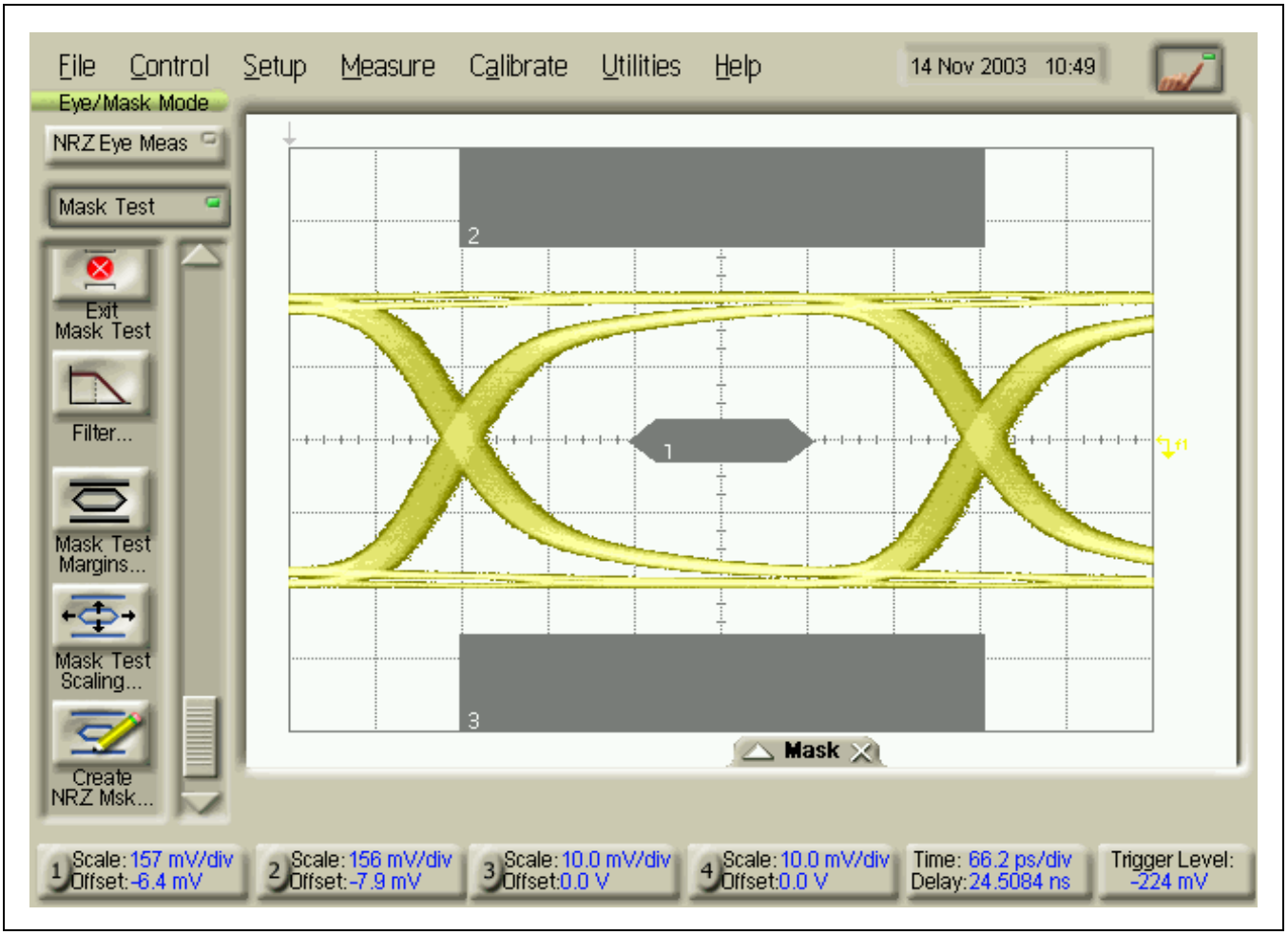


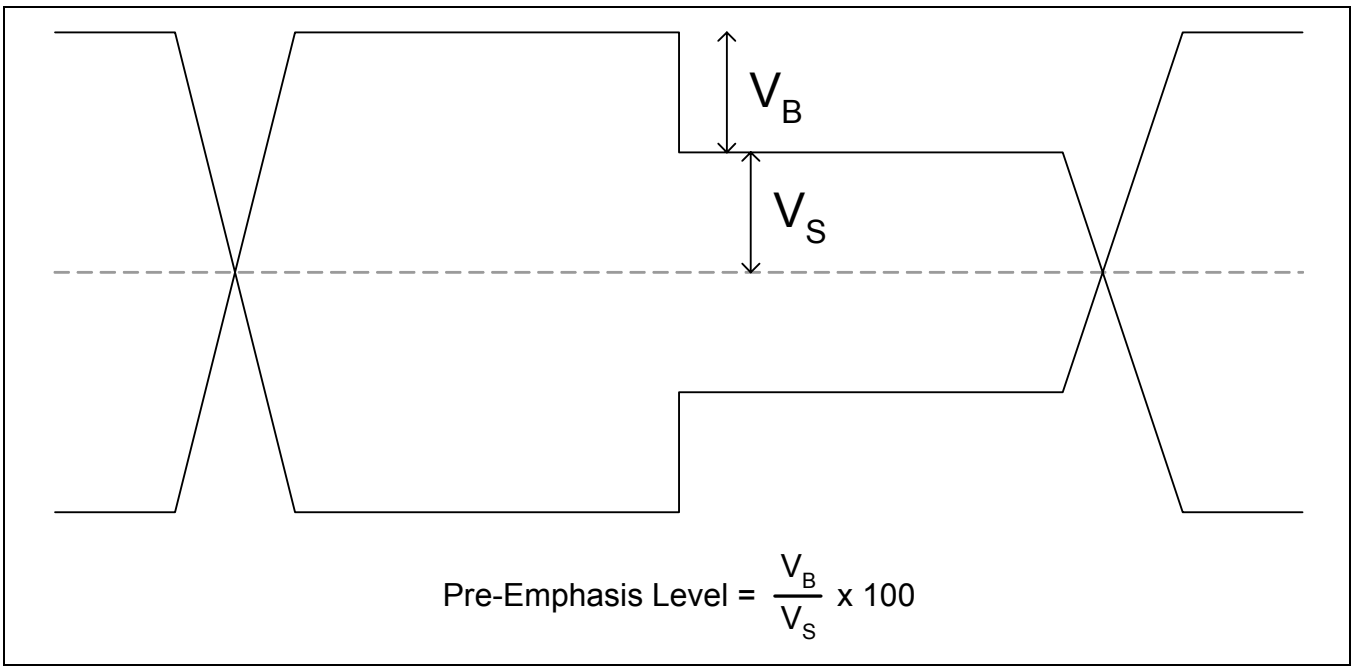
Figure 1-3. 2.5 Gbps waveform at M21050 output with input shown in Figure 1-2 (CDR enabled and IE at maximum setting)



1.1.11 Output Pre-Emphasis

Each of the eight output channels contains an independent output pre-emphasis circuit that can be used to select the optimal pre-emphasis level. The pre-emphasis settings have been optimized for a variety of connectivity applications such as board traces and cables. For the PCB, the settings have been specified to operate up to 40” at 3.1875 Gbps on FR4, and up to 60” on FR4 at 2.125 Gbps. Like the input equalizer settings, the output pre-emphasis has similar high performance on Nelco-13, Arlon 25, Rogers 3003, 4003C, 4340, GeTek PCB materials, and twinaxial cables. The digital pre-emphasis level is selected, for each output channel, with *Preemp_ctrl*_N[2:0], and the default value of 000b corresponds to pre-emphasis disabled.

Figure 1-4. Definition of Pre-Emphasis Levels



1.1.12 Dual 4x4 Loopback

The M21050 Octal CDR is designed to operate in groups of four CDRs, for applications where four channels are used for transmit, and four channels are used for receive. Two loopbacks (A-side and B-side) are provided to loopback the two groups of four CDRs. The A-side loopback, enabled by setting *Loopback* [0] = 1b, connects ***DoutA0*** to ***DinB0***, ***DoutA1*** to ***DinB1***, ***DoutA2*** to ***DinB2***, and ***DoutA3*** to ***DinB3***. In addition, the A-side loopback can have the order reversed, by setting *Loopback* [1] = 1b, which connects ***DoutA0*** to ***DinB3***, ***DoutA1*** to ***DinB2***, ***DoutA2*** to ***DinB1***, and ***DoutA3*** to ***DinB0.*** The B-side loopback, enabled by setting *Loopback* [2] = 1b, connects ***DoutB0*** to ***DinA0***, ***DoutB1*** to ***DinA1***, ***DoutB2*** to ***DinA2***, and ***DoutB3*** to ***DinA3***. In addition, the B-side loopback can have the order reversed, by setting *Loopback* [3] = 1b, which connects ***DoutB0*** to ***DinA3***, ***DoutB1*** to ***DinA2***, ***DoutB2*** to ***DinA1***, and ***DoutB3*** to ***DinA0.*** The default is 0000b, which disables loopback for all eight channels. Refer to the front cover functional block diagram for an illustration of the A-side and B-side loopbacks. This feature is not available in the hardwired mode.

1.1.13 CDR Features

The M21050 contains eight multi-rate CDRs, that can each operate at independent data-rates. When the CDR achieves phase lock onto the incoming data stream, the CDR removes the incoming random jitter above its loop bandwidth, as well as any deterministic jitter remaining from the two input deterministic jitter attenuators (IE & DC servo). The M21050 output data has low jitter, due to retiming with a low jitter generation CDR. The output pre-emphasis option allows for compensation of interconnect deterministic jitter, generated up to the next downstream device.

Each CDR is capable of multi-rate operation which is achieved by a combination of built in VCO frequency dividers (VCD), Data Rate Dividers (DRD), and a wide VCO tuning range (F_{min} = 2.0 GHz, F_{max} = 3.2 GHz). As a result, the allowed input data range is F_{min} / DRD_{max} to F_{max} / DRD_{min}. Although the ranges are not continuous, the ranges are deliberately chosen to cover all typical applications.

By default, the loop bandwidth is set at an approximate bandwidth of 8 MHz, with DRD = 1 and F_{vco} = 2.5 GHz. Within a given VCO frequency range, the bandwidth will scale proportionately. For example, if the loop bandwidth (F_{LBW}) is 8 MHz at 2.5 GHz, then at 3.125 GHz the F_{LBW} will be 10 MHz. When DRD is not equal to 1, the bandwidth at DRD = 1 scales by the DRD divide ratio. For example, if the F_{LBW} is 8 MHz at F_{vco} = 2.5 GHz with DRD = 1, then if DRD = 2, F_{vco} = 1.25 GHz and the F_{LBW} will be 4 MHz. In the hardwired mode, the F_{LBW} will be properly set for the hardwired data-rates. In the two-wire interface mode, the default bandwidth scales automatically with the input data-rate, and the bandwidth can be tuned through the registers.

The CDR needs to achieve frequency lock before it can achieve phase lock and re-time the input data. Frequency reference acquisition (FRA) requires an external frequency source to be connected to the ***RefClk*** [P/N] pins.

Frequency acquisition is accomplished with two key sections. The first section is a secondary frequency lock loop (FLL) that drives the VCO towards the desired frequency. The second section is the loss-of-lock circuitry (LOLCir), that turns on or off the secondary FLL. In general, both LOL and LOA have register bits (*Alarm_LOA* and *Alarm_LOL*) which are active high, and pins (***xAlarmA*** and ***xAlarmB***) which are active low. The pin ***xAlarmA*** (***xAlarmB***) is an internal wired OR of the four LOL and four LOA alarms associated with the four CDRs in block A(B). ***xAlarmA*** and ***xAlarmB*** can be wired OR externally. In the general context, they will be referred to as LOL or LOA which is active H. Frequency acquisition takes place when the LOLCir determines an out of lock condition (LOL = H) for each CDR, when the VCO frequency exceeds a given range (window). LOLCir enables the secondary FLL to drive the VCO close to the desired frequency (typically the signal data-rate). When the VCO falls within a given frequency range where the CDR loop can acquire phase lock, LOLCir turns off the secondary FLL and sets LOL = L, allowing the CDR to achieve phase lock. During this time, LOLCir continues to monitor the frequency difference and will signal a LOL = H, to start the acquisition routine again, if the frequency falls out of range. The LOLCir range is fixed in the hardwired mode, and programmable in the two-wire interface mode. The frequency threshold (window) for LOL = H-to-L and LOL = L-to-H are different, to prevent LOL from toggling when the frequency is near one of the windows. These registers also control the frequency acquisition time. Suggested values are given in this document for general robust operation, and are used as register defaults, however, the programmability of the registers allow for optimization based on a given application (e.g. faster lock times).

Each CDR contains an independent loss of activity (LOA) detector that determines if there is valid data, by looking at the transition density of the reference clock. Fixed window detectors compare the data transition density with the reference clock. If the data transition density falls outside of the window, a loss of activity condition is signaled. When LOA goes high, it also (just like LOL) forces the FLL to turn on, so that the VCO will be forced to the desired frequency range. When LOA goes low again, phase lock will occur.

All of the CDRs are reset upon ***xRST*** = L, *Mastreset* = AAh, or upon power up. A soft reset through *CDR_ctrlA*_N[7] = 1b resets the individual CDR state machine, and presets the CDR to an out-of-lock condition, however, the register contents that are related to CDR setup are unchanged. It is required to force a soft reset if the data-rate is dynamically changed. The soft reset register bit needs to be cleared for proper operation. A reset during operation will cause bit errors, until the CDR achieves phase lock.

By default, all of the CDRs are active and powered up for normal operation. By setting *CDR_ctrlB*_N[7:6] = 11b, a CDR can be bypassed and powered down, to allow for non-standard data-rates, or to save power when the CDR is not required at lower data-rates. When *CDR_ctrlB*_N[7:6] = 01b, the CDR is bypassed so the output data is not retimed but active (VCO locked to the input data). In the last mode with *CDR_ctrlB*_N[7:6] = 10b, the CDR is powered down, and all signals along the input and output paths are also powered down, to save power. In this case, the input data does not reach the output.

The internal loop filter automatically scales with the VCO data rate divider selection. For operation with the VCO tuning range for a fixed DRD setting, the loop bandwidth scales proportionally for the new data-rate. The loop bandwidth can be selected with *Phadj_ctrl*_N[5:4], and the 400% setting with *Phadj_ctrl*_N[5:4] = 10b is the default.

To prevent the propagation of noise in the case where there is a LOL/LOA condition, the CDR contains an auto-inhibit feature, which is enabled by default. When either LOA or LOL is active, the output of the CDR is fixed at a logic high state (***DoutP*** = H, ***DoutN*** = L). This feature can be disabled by setting *CDR_ctrlA*_N[3] = 0b, which allows *CDR_ctrlA*_N[5] to either force an inhibit (1b) or to never inhibit (0b).

In some optical module and back-plane applications, the optimal data sampling point is not in the middle of the data eye. By default, the CDR achieves phase lock very near the center of the eye. For optimal performance (jitter tolerance), the actual sampling point can be adjusted with *Phadj_ctrl*_N[3:0]. The adjustment range is from –122.5 mUI to +122.5 mUI with 17.5 mUI steps.

1.1.14 Multi-Rate CDR Data-Rate Selection

For multi-rate operation, the first step is to determine the desired data-rate range. The input data range must be bracketed by $DF_{min} = F_{vco,min}/DRD_{max}$ to $DF_{max} = F_{vco,max}/DRD_{min}$. $DF_{max/min}$ are the maximum/minimum data input frequencies, $DRD_{max/min}$ is the data rate divider setting with *CDR_ctrlB*_N[3:0], and $F_{vco,min}/F_{vco,max}$ are the minimum/maximum VCO frequencies, which are 2.0 GHz and 3.2 GHz respectively. The valid data rates are shown in Table 1-8.

Table 1-8. Valid Input Data Range

Parameter	DF_{min}	DF_{max}	Units
Data-rate divider (DRD = 1): *CDR_ctrlB*_N[3:0] = 0000b	2.0	3.2	GHz
Data-rate divider (DRD = 2): *CDR_ctrlB*_N[3:0] = 0001b	1.0	1.6	GHz

It is important to note the difference between the VCO frequency (F_{vco}), and the data rate frequency (DF). F_{vco} is always between 2 GHz to 3.2 GHz, while DF is the divided down F_{vco} that matches the input data rate.

1.1.15 Frequency Reference Acquisition (FRA)

When an external reference is applied to ***RefClk*** [P/N], the FRA mode is enabled in either the hardwired or two-wire serial interface mode. Frequency acquisition is enabled by the LOLCir when LOL = H (*Alarm_LOL* [N] = 1b). With FRA enabled, a secondary FLL attempts to lock the VCO to a frequency derived from the external reference. When the frequency is close to the desired frequency, LOLCir sets LOL = L and disables the secondary FLL, thus, the main CDR PLL is free to phase lock to the incoming data. Although the main CDR can achieve frequency lock, the VCO frequency tuning range typically exceeds the CDR's inherent acquisition range, which implies at a minimum, the FRA needs to get the VCO within the CDR range. The loss of lock circuitry (LOLCir) is used to determine when the secondary FLL is active. The LOLCir consists of window detectors that constantly compare a scaled VCO frequency, to a frequency related to the external reference. When LOL = H the loop is out of lock, FRA is activated until the frequency difference is within the narrow reference window (NRW). When LOL = L, FRA is not engaged until the frequency exceeds the wide reference window (WRW). If a signal is not present, the circuit will drive the VCO frequency to the NRW and turn-off. Without data present, the CDR will then drift until the frequency difference exceeds the WRW, and repeat this cycle. To prevent this, by default, FRA is activated with LOL = H, or LOA = H and FRA is not de-activated unless both LOL = L and LOA = L.

Figure 1-5. Block Diagram of FRA Mode

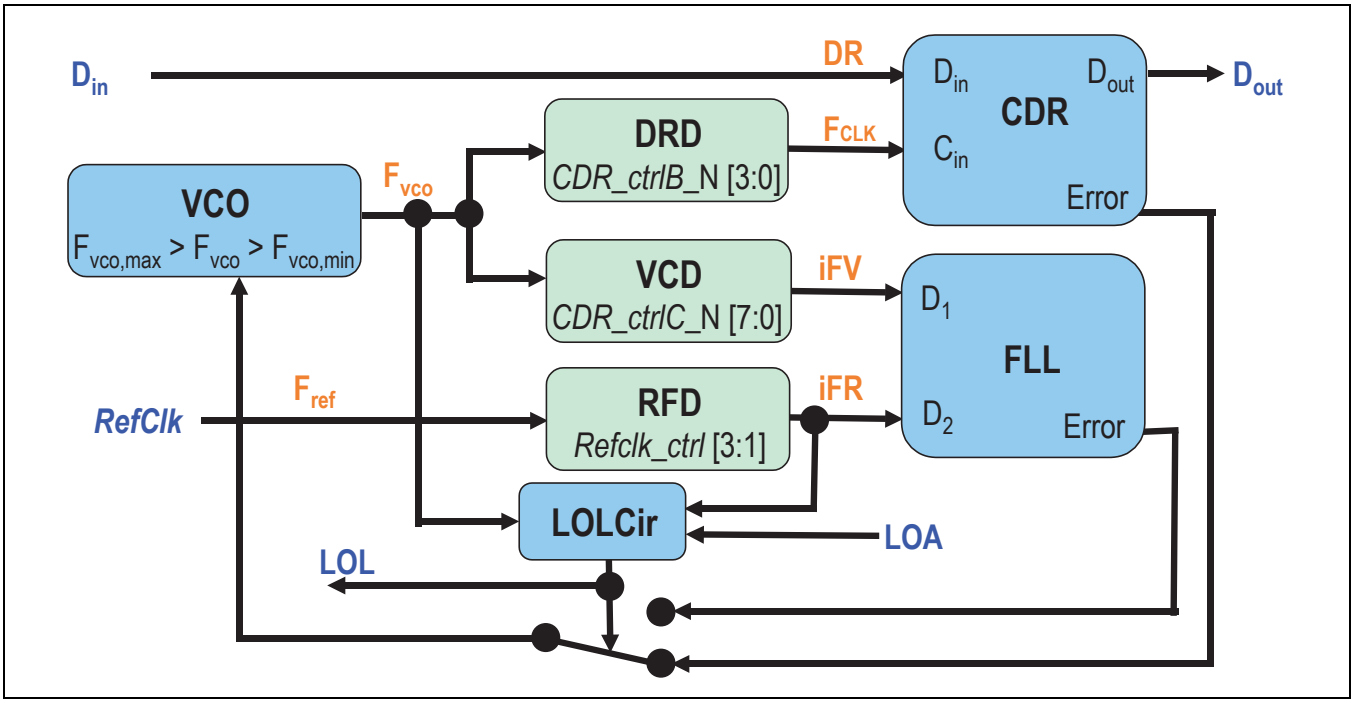


Figure 1-5 shows a block diagram of the FRA mode. The secondary FLL for FRA compares a scaled version of the internal VCO frequency (iFV) with a scaled version of the input reference frequency (iFR), and iFR and iFV are limited to between 10 MHz and 25 MHz. The external reference frequency (F_{ref}) is applied to the ***RefClk*** [P/N] terminals. This reference frequency is scaled to the iFR by the Reference Frequency Divider (RFD) [*Refclk_ctrl* [3:1]], which allows for the external reference to vary on the order of 10 MHz to 800 MHz. The RFD level is a globally set value that applies to all CDRs. Table 1-9 gives the divider ratio, along with the minimum and maximum F_{ref} values.

Table 1-9. Reference Clock Frequency Ranges

RFD Value	Minimum F_{ref} (MHz)	Maximum F_{ref} (MHz)
RFD (*Refclk_ctrl* [3:1] = 000b): divide by 1	10	25
RFD (*Refclk_ctrl* [3:1] = 001b): divide by 2	20	50
RFD (*Refclk_ctrl* [3:1] = 010b): divide by 4	40	100
RFD (*Refclk_ctrl* [3:1] = 011b): divide by 8	80	200
RFD (*Refclk_ctrl* [3:1] = 100b): divide by 12	120	300
RFD (*Refclk_ctrl* [3:1] = 101b): divide by 16	160	400
RFD (*Refclk_ctrl* [3:1] = 110b): divide by 32	320	800

The VCO frequency is scaled to the iFV by the VCO Comparison Divider (VCD) [*CDR_ctrlC*_N[7:0]]. The external reference clock frequency must be an integer multiple of the input signal data-rate. Table 1-10 provides DRD, RFD, and VCD values for common applications. DRD is the data-rate divider set with register *CDR_ctrlB*_N[3:0], RFD is the reference frequency divider set with register *Refclk_ctrl* [3:1], and VCD is the VCO comparison divider set with register *CDR_ctrlC*_N[7:0]. For applications not listed in Table 1-10, please contact the Mindspeed applications engineering group.

Table 1-10. DRD/RFD/VCD Settings for Different Data-Rates and Reference Frequencies

Application	DR (Mbps)	Fref (MHz)	DRD	RFD	VCD	Notes
10GE - XAUI	**3125**	**156.25**	**1**	**8**	**160**	**1**
10GE-XAUI	3125	25	1	2	250	
10GFC - XAUI	**3187.5**	**159.375**	**1**	**8**	**160**	**1**
InfiniBand	**2500**	**250**	**1**	**16**	**160**	**1**
InfiniBand	2500	125	1	8	160	
InfiniBand	**2500**	**62.5**	**1**	**4**	**160**	**1**
STS-48	**2488.32**	**155.52**	**1**	**8**	**128**	**1**
STS-48	2488.32	19.44	1	1	128	
2GFC	**2125**	**106.25**	**1**	**8**	**160**	**1**
2GFC	2125	25	1	2	170	
GE	**1250**	**125**	**2**	**8**	**160**	**1**
GE	1250	25	2	2	200	
FC	**1062.5**	**106.25**	**2**	**8**	**160**	**1**

NOTE:
1. Bold text denotes data-rates selectable in the hardwired control mode.

The FLL drives iFV to iFR, and it is the primary function of LOLCir to determine when to turn off the FLL, so the CDR can achieve phase lock. LOLCir uses the frequency difference between iFV and iFR to switch LOL, which turns on and off the secondary FLL. The thresholds where LOL makes a transition are defined as windows, which are fixed in the hardwired mode, and programmable in the two-wire interface mode. To prevent LOL from toggling at the threshold, two windows are used for hysteresis. When LOL = L and the frequency difference exceeds the larger window (WRW), LOL L-to-H occurs to signal an out of lock case. When LOL = H (and LOA = L), the frequency difference is brought within the narrow (NRW) window, after which LOL makes a H-to-L transition signaling in-lock. If LOA = H when LOL = H, the FLL remains on to keep the VCO locked to the reference, until a signal is present. N_{acq} is defined with *LOL_ctrl*_N[7:5], N_{narrow} is defined with *LOL_ctrl*_N[4:1], and N_{wide} is defined with *LOL_ctrl*_N[0]. The LOLCir averages a large number of transitions before making an LOL decision. This averaging time is referred to as the LOL decision time or DT_{LOL}.

Table 1-11 shows various window sizes for different applications, including the default value in both the hardwired and serial interface modes.

Table 1-11. LOL Window Size and Decision Time Examples

Condition	N_{acq}	N_{narrow}	N_{wide}	Narrow Window (ppm)	Wide Window (ppm)	Decision Time (µs)
Hardwired mode	101b	0011b	0b	±1465	±1955	420
Two-wire serial interface mode	101b	0011b	0b	±1465	±1955	420
iFV = iFR	111b	0010b	1b	±245	±975	1685
Fast lock	010b	0001b	0b	±5860	±7800	56

Notes:
1. Decision time is calculated with iFR = 19.44 MHz; will scale proportionally with iFR range from 10 to 25 MHz.
2. Above are examples showing ability to tailor windows for data-rates, reference frequencies, and acquisition times.

1.1.16 Loss of Activity

By default, the LOA detector is enabled and can be disabled by setting *CDR_ctrlA*_N[1] = 0b, where N is mapped to the CDR (number). Loss of activity measures the transition density of data to determine if the data is valid. During small time intervals, variations are due to data content, packet headers, stress patterns, etc., which is taken into account by averaging over a larger time period. In some applications, when data is not present, noise produces rail-to-rail transitions that cause problems with level based detectors. These applications include cascaded CDRs, high-gain crosspoints, as well as modules with optical amplifiers. As a result, the transition density LOA can separate data from random noise, determine false lock at the wrong integer and non-integer data-rate, signal stuck high/low conditions, and determine false lock to re-timed noise. Unlike level based detectors, it cannot determine false lock onto low amplitude data, which is a condition that does not typically occur with backplane applications, and can be handled by the limiting amplifier or pre-amplifier in modules. The LOA window is fixed at 25% to 100%.

1.1.17 Built-in Self Test (BIST) Overview

The M21050 contains a single BIST test pattern generator as well as a test pattern receiver. Both the BIST transmitter (BIST Tx), and BIST receiver (BIST Rx) are designed to operate with fixed patterns. PRBS 2^7-1, 2^{15}-1, 2^{23}-1, and 2^{31}-1 test patterns are provided. For 8b/10b testing, the fibre channel CRPAT and CJTPAT standard patterns are supported. In addition, an 8b/10b countdown pattern is also provided; this is the 8b/10b representation of a binary count from 255 to 0, while maintaining 8b/10b running disparity requirements. User programmable 16 bit and 20 bit patterns are also provided; they are typically used to generate short patterns for debug, such as 1100b, as well as 8b/10b idle or control characters. The BIST is designed to reduce system development time, as well as product test costs, and can be used by both the equipment provider as well as the equipment end user.

When enabled, the BIST Rx allows one input from the CDR to enter the BIST receiver. The desired channel to monitor is selected through a control register. The BIST Rx uses the recovered clock and data from the selected CDR to drive the pattern checker. Every time a bit error is received, the error register is incremented. The maximum number of errors is FFh, and all subsequent errors will not be counted. At any time, the error register can be cleared. By keeping track of the time between clear and read, a rough BER number can be obtained.

When enabled, the BIST Tx can broadcast the output test pattern to any of the CDR outputs (the BIST Tx and Rx can be used at the same time). The BIST Tx contains an internal clock multiplier (PLL), that can take its input from either the external reference frequency, or from the same CDR that is driving the BIST Rx (only in full rate mode, DRD = 1).

1.1.18 BIST Test Patterns

The test pattern is selected with *BISTtx_ctrl* [5:2] for the transmitter, and *BISTrx_ctrl* [5:2] for the receiver.

The PRBS patterns generated by the unit are ITU-T 0.151 compliant, and summarized in Table 1-12.

Table 1-12. BIST PRBS Patterns

BISTtx_ctrl **[5:2]** / *BISTrx_ctrl* **[5:2]**	**Pattern**	**Polynomial**
0000b	PRBS 2^7-1	2^7+2^6+1
0001b	PRBS 2^{15}-1	$2^{15}+2^{14}+1$
0010b	PRBS 2^{23}-1	$2^{23}+2^{18}+1$
0011b	PRBS 2^{31}-1	$2^{31}+2^{28}+1$

For 8b/10b based applications, three patterns are available. The CJTPAT and CRPAT comply with the Fibre Channel T11.2/Project 1230/Rev10 specifications.

Table 1-13. BIST 8b/10b Patterns

BISTtx_ctrl **[5:2]** / *BISTrx_ctrl* **[5:2]**	**Pattern**
0100b	CJTPAT
0101b	CRPAT
0110b	Countdown

Two user programmable patterns that are 16 bits long (*BISTtx_ctrl* [5:2] = *BISTrx_ctrl* [5:2] = 0111b) and 20 bits long (*BISTtx_ctrl* [5:2] = *BISTrx_ctrl* [5:2] = 1000b) are determined with *BIST_pattern0...BIST_pattern2*. Note that the contents of these registers are used by both the BIST Tx and the BIST Rx, if they are setup in this mode.

1.1.19 BIST Receiver (BIST Rx) Operation

The BIST Rx is powered up and enabled by setting *BISTrx_ctrl* [1] = 1b (off by default), resetting the BIST Rx block with *BISTrx_ctrl* [0] = 1b (default), and selecting a pattern with *BISTrx_ctrl* [5:2]. The signal to the BIST Rx is routed from the output of the CDR, and the BIST Rx can only check one channel at a time. The desired channel to monitor is selected with *BISTrx_chsel* [2:0]. The BIST Rx uses the recovered clock from the CDR to drive the BIST state-machine, thus the CDR must be enabled and locked to data for proper operation. When the data is valid, *BISTrx_ctrl* [6] = 1b is used to clear the error register, and all subsequent errors can be read back through *BISTrx_error*. The BIST Rx automatically synchronizes the input data with the pattern.

1.1.20 BIST Transmitter (BIST Tx) Operation

The BIST Tx is powered up and enabled by setting *BISTtx_ctrl* [1] = 1b (off by default), resetting the BIST Tx block with *BISTtx_ctrl* [0] = 1b (default), and selecting a pattern with *BISTtx_ctrl* [5:2]. The BIST Tx can multicast the test pattern to any channels selected with *BISTtx_chsel* [7:0]. The high-speed clock of the BIST Tx is generated from its own frequency multiplier PLL, that uses a selectable frequency reference determined by *BISTtx_ctrl* [6]. With *BISTtx_ctrl* [6] = 0b (default), the external reference clock is used and typically gives the lowest jitter output, however, it is not typically synchronized with the data rate. With *BISTtx_ctrl* [6] = 1b, the reference clock is derived from the same CDR used to drive the BIST Rx, which gives an output synchronized with the data rate (this feature only works with DRD = 1 for that CDR), however, it contains the low-frequency jitter from the input data. In this mode, the BIST Tx output is synchronous with the CDR used in the BIST Rx. In either case, the BIST Tx PLL needs to be

configured for the proper data-rate. When the PLL is properly configured and locked to the reference, the LOL flag should be low (*BISTtx_alarm* [7]). A bit error can be intentionally inserted into the BIST Tx output, by providing a 0b, 1b, 0b sequence to *BISTtx_ctrl* [7].

The BIST Tx PLL setup is similar to the CDR, thus, the description of similar registers for the CDR also applies and will not be repeated here. The desired output data rate is set with the DRD register (*BISTtx_PLL_ctrlB* [3:0]) and with the VCD register (*BISTtx_PLL_ctrlC* [7:0]). The input reference frequency iFR is the same as for the main CDRs, since the same external reference and reference dividers are used. In the internal CDR case, iFR is $F_{vco,rxcdr}/128$, where $F_{vco,rxcdr}$ is the VCO frequency of the CDR selected by *BISTrx_chsel* [2:0]. Like the CDRs, if the output data-rate of the Tx needs to be changed, the Tx requires a soft reset.

1.1.21 Junction Temperature Monitor

An internal junction temperature monitor with a range of –40°C to 130°C is integrated into the M21050. On the low end, the temperature monitor (Tmon) is set to measure –40°C to 10°C in six 10°C steps, and on the high end, 80°C to 130°C in six 10°C steps. The typical temperature resolution is 3°C. The temperature monitor is enabled with *Temp_mon* [1] = 1b. When enabled, the temperature measurement cycle is achieved by providing a rising edge for *Temp_mon* [0]. Afterwards, the correct temperature can be read from *Temp_value* [3:0]. Table 1-14 shows the mapping of the temperature to *Temp_value* [3:0]. Enabling and strobing the temperature in the same write cycle will not yield reliable results.

Table 1-14. Junction Temperature Monitor

Junction Temperature	*Temp_value* [3:0]	Condition
Tc ≥ 130°C	1100b	High-alarm
130°C > Tc ≥ 120°C	1011b	High-alarm
120°C > Tc ≥ 110°C	1010b	High-warning
110°C > Tc ≥ 100°C	1001b	Normal
100°C > Tc ≥ 90°C	1000b	Normal
90°C > Tc ≥ 80°C	0111b	Normal
80°C > Tc ≥ 10°C	0110b	Normal
10°C > Tc ≥ 0°C	0101b	Low-warning
0°C > Tc ≥ -10°C	0100b	Low-alarm
-10°C > Tc ≥ -20°C	0011b	Low-alarm
-20°C > Tc ≥ -30°C	0010b	Low-alarm
-30°C > Tc ≥ -40°C	0001b	Low-alarm
-40°C > Tc	0000b	Low-alarm

1.1.22 IC Identification / Revision Code

The IC identification can be read back from *Chipcode,* and the revision of the device can be read back from *Revcode*. The assigned IC identification for the M21050 is 19h and the revision code is 20h.

1.2 Pin Definitions

Table 1-15. Power Pins

Pin Name	Function	Type
Vss	Device ground	Power
AVdd_I/O	Analog I/O positive supply	Power
AVdd_Core	Analog core positive supply	Power
DVdd_I/O	Digital I/O positive supply	Power
DVdd_Core	Digital core positive supply	Power

Notes:
1. If internal regulator is enabled, connect all of the ***AVdd_Core*** and/or ***DVdd_Core*** pins together to a common floating plane and bypass to ***Vss***.
2. If internal regulator is NOT enabled, it is recommended that all ***AVdd_Core*** pins be tied to a plane at 1.2V, that is bypassed to ground. ***DVdd_Core*** can be tied to this plane or separately decoupled.
3. Device ground (***Vss***) is established by contact with exposed pad on underside of package; there are no ***Vss*** pins.

Table 1-16. High-Speed Signal Pins (1 of 2)

Pin Name	Function	Termination	Type
DinA0P	Serial positive data input for channel 0	50Ω pull up to ***VddTA0/1***	Input
DinA0N	Serial negative data input for channel 0	50Ω pull up to ***VddTA0/1***	Input
DinA1P	Serial positive data input for channel 1	50Ω pull up to ***VddTA0/1***	Input
DinA1N	Serial negative data input for channel 1	50Ω pull up to ***VddTA0/1***	Input
DinA2P	Serial positive data input for channel 2	50Ω pull up to ***VddTA2/3***	Input
DinA2N	Serial negative data input for channel 2	50Ω pull up to ***VddTA2/3***	Input
DinA3P	Serial positive data input for channel 3	50Ω pull up to ***VddTA2/3***	Input
DinA3N	Serial negative data input for channel 3	50Ω pull up to ***VddTA2/3***	Input
VddTA0/1	Termination Pin for ***DinA*** [1:0]	Terminate to ***AVdd_Core***	Input Termination
VddTA2/3	Termination Pin for ***DinA*** [3:2]	Terminate to ***AVdd_Core***	Input Termination
DoutA0P	Serial positive data output for channel 0	50Ω pull up ***AVdd_I/O***	Output
DoutA0N	Serial negative data output for channel 0	50Ω pull up ***AVdd_I/O***	Output
DoutA1P	Serial positive data output for channel 1	50Ω pull up ***AVdd_I/O***	Output
DoutA1N	Serial negative data output for channel 1	50Ω pull up ***AVdd_I/O***	Output
DoutA2P	Serial positive data output for channel 2	50Ω pull up ***AVdd_I/O***	Output
DoutA2N	Serial negative data output for channel 2	50Ω pull up ***AVdd_I/O***	Output
DoutA3P	Serial positive data output for channel 3	50Ω pull up ***AVdd_I/O***	Output
DoutA3N	Serial negative data output for channel 3	50Ω pull up ***AVdd_I/O***	Output
DinB0P	Serial positive data input for channel 0	50Ω pull up to ***VddTB0/1***	Input
DinB0N	Serial negative data input for channel 0	50Ω pull up to ***VddTB0/1***	Input
DinB1P	Serial positive data input for channel 1	50Ω pull up to ***VddTB0/1***	Input
DinB1N	Serial negative data input for channel 1	50Ω pull up to ***VddTB0/1***	Input

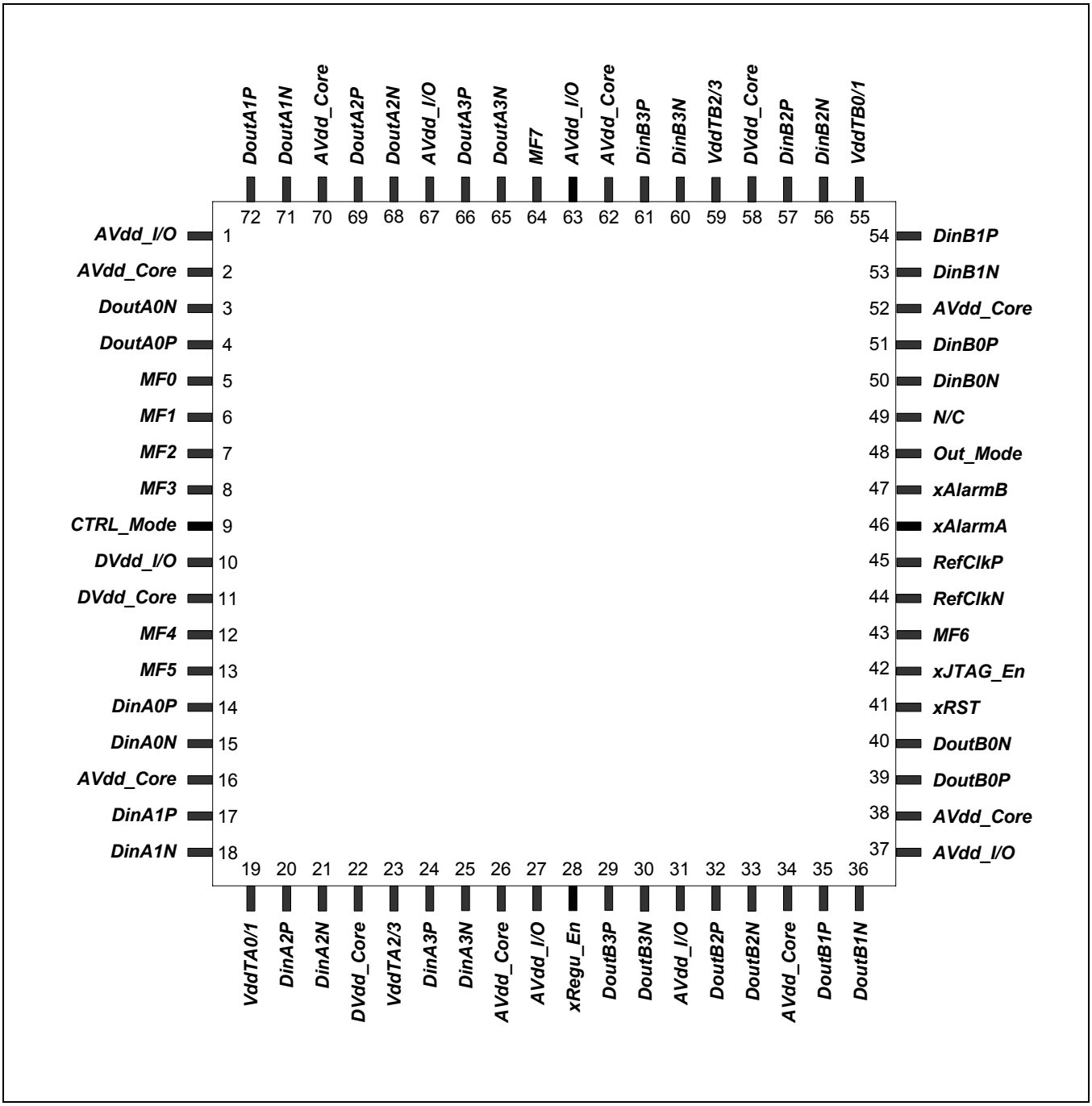
Table 1-16. High-Speed Signal Pins (2 of 2)

Pin Name	Function	Termination	Type
DinB2P	Serial positive data input for channel 2	50Ω pull up to ***VddTB2/3***	Input
DinB2N	Serial negative data input for channel 2	50Ω pull up to ***VddTB2/3***	Input
DinB3P	Serial positive data input for channel 3	50Ω pull up to ***VddTB2/3***	Input
DinB3N	Serial negative data input for channel 3	50Ω pull up to ***VddTB2/3***	Input
VddTB0/1	Termination pin for ***DinB*** [1:0]	Terminate to ***AVdd_Core***	Input Termination
VddTB2/3	Termination pin for ***DinB*** [3:2]	Terminate to ***AVdd_Core***	Input Termination
DoutB0P	Serial positive data output for channel 0	50Ω pull up ***AVdd_I/O***	Output
DoutB0N	Serial negative data output for channel 0	50Ω pull up ***AVdd_I/O***	Output
DoutB1P	Serial positive data output for channel 1	50Ω pull up ***AVdd_I/O***	Output
DoutB1N	Serial negative data output for channel 1	50Ω pull up ***AVdd_I/O***	Output
DoutB2P	Serial positive data output for channel 2	50Ω pull up ***AVdd_I/O***	Output
DoutB2N	Serial negative data output for channel 2	50Ω pull up ***AVdd_I/O***	Output
DoutB3P	Serial positive data output for channel 3	50Ω pull up ***AVdd_I/O***	Output
DoutB3N	Serial negative data output for channel 3	50Ω pull up ***AVdd_I/O***	Output

Table 1-17. Control, Interface, and Alarm Pins

Pin Name	Function	Default	Type
MF0	Multifunction pin for hardwired mode, and two-wire interface	Internal pull up	CMOS
MF1	Multifunction pin for hardwired mode, and two-wire interface	Internal pull up	CMOS
MF2	Multifunction pin for hardwired mode, and two-wire interface	Internal pull up	CMOS
MF3	Multifunction pin for hardwired mode, and two-wire interface	Internal pull up	CMOS
MF4	Multifunction pin for hardwired mode, two-wire interface, and JTAG	Internal pull up	CMOS
MF5	Multifunction pin for hardwired mode, two-wire interface, and JTAG	Internal pull up	CMOS
MF6	Multifunction pin for hardwired mode, and JTAG	Internal pull up	CMOS
MF7	Multifunction pin for hardwired mode, and JTAG	Internal pull up	CMOS
CTRL_Mode	Enable hardwired mode or two-wire interface (1b = hardwired)	Internal pull up	CMOS
Out_Mode	Selects output data format (0b = PCML)	Internal pull down	CMOS
xRST	Reset pin (L = reset)	Internal pull up	CMOS
xJTAG_En	JTAG testing control pin (L = enable)	Internal pull down	CMOS
xRegu_En	Internal voltage regulator control pin (L = enable)	Internal pull up	CMOS
RefClkP	Reference clock positive input	Internal pull down	I - AC coupled
RefClkN	Reference clock negative input	Internal pull down	I - AC coupled
xAlarmA	A-side loss of activity/lock alarm	No internal pull up/down	O - open drain
xAlarmB	B-side loss of activity/lock alarm	No internal pull up/down	O - open drain

Figure 1-6. M21050 Pinout Diagram (Top View)



2.0 Registers

Table 2-1. Register Table Summary

Addr	Register Name	d7: MSB	d6	d5	d4	d3	d2	d1	d0: LSB
Common Registers									
00h	*Globctrl*	powerup	MSPD int	MSPD int	MSPD int	MSPD int	MSPD int	reserved	clear_alm
03h	*Loopback*	reserved	reserved	reserved	reserved	loopback[3]	loopback[2]	loopback[1]	loopback[0]
04h	*Refclk_ctrl*	reserved	reserved	reserved	reserved	ref_divr[2]	ref_divr[1]	ref_divr[0]	MSPD int
05h	*Mastreset*	rst	rst	rst	rst	rst	rst	rst	rst
06h	*Chipcode*	chipcode[7]	chipcode[6]	chipcode[5]	chipcode[4]	chipcode[3]	chipcode[2]	chipcode[1]	chipcode[0]
07h	*Revcode*	revcode[7]	revcode[6]	revcode[5]	revcode[4]	revcode[3]	revcode[2]	revcode[1]	revcode[0]
08h	*Input_hys*	reserved	reserved	en_hys	reserved	reserved	reserved	reserved	reserved
10h	*BISTrx_chsel*					reserved	chan[2]	chan[1]	chan[0]
11h	*BISTrx_ctrl*	MSPD int	rx_ctrclr	rx_patt[3]	rx_patt[2]	rx_patt[1]	rx_patt[0]	en_rx	rx_rst
12h	*BISTrx_error*	err[7]	err[6]	err[5]	err[4]	err[3]	err[2]	err[1]	err[0]
14h	*BISTtx_chsel*	tx_chan_7	tx_chan_6	tx_chan_5	tx_chan_4	tx_chan_3	tx_chan_2	tx_chan_1	tx_chan_0
15h	*BISTtx_ctrl*	err_insert	rx2txclk	tx_patt[3]	tx_patt[2]	tx_patt[1]	tx_patt[0]	en_tx	tx_rst
17h	*BISTtx_LOLctrl*	tacq_LOL[2]	tacq_LOL[1]	tacq_LOL[0]	narwin_LOL[3]	narwin_LOL[2]	narwin_LOL[1]	narwin_LOL[0]	widwin_LOL[0]
18h	*BISTtx_PLL_ctrlA*	softreset	MSPD int	reserved	MSPD int	reserved	MSPD int	reserved	MSPD int
19h	*BISTtx_PLL_ctrlB*	PLLmode[1]	PLLmode[0]	MSPD int	MSPD int	data_rate[3]	data_rate[2]	data_rate[1]	data_rate[0]
1Ah	*BISTtx_PLL_ctrlC*	VCO_divr[7]	VCO_divr[6]	VCO_divr[5]	VCO_divr[4]	VCO_divr[3]	VCO_divr[2]	VCO_divr[1]	VCO_divr[0]
1Bh	*BIST_pattern0*					pattern[19]	pattern[18]	pattern[17]	pattern[16]
1Ch	*BIST_pattern1*	pattern[15]	pattern[14]	pattern[13]	pattern[12]	pattern[11]	pattern[10]	pattern[9]	pattern[8]
1Dh	*BIST_pattern2*	pattern[7]	pattern[6]	pattern[5]	pattern[4]	pattern[3]	pattern[2]	pattern[1]	pattern[0]
1Fh	*BISTtx_alarm*	tx_LOL	reserved	reserved	MSPD int	MSPD int	MSPD int	MSPD int	MSPD int
20h	*Temp_mon*					reserved	reserved	en_temp_mon	strobe_temp
21h	*Temp_value*					temp[3]	temp[2]	temp[1]	temp[0]
30h	*Alarm_LOL*	LOL_7	LOL_6	LOL_5	LOL_4	LOL_3	LOL_2	LOL_1	LOL_0
31h	*Alarm_LOA*	LOA_7	LOA_6	LOA_5	LOA_4	LOA_3	LOA_2	LOA_1	LOA_0
Per channel registers (N = channel/CDR#, M = N+4)									
M0h	*CDR_ctrlA*_N	softreset	MSPD int	inh_force	MSPD int	autoinh_en	MSPD int	LOA_en	MSPD int
M1h	*CDR_ctrlB*_N	CDRmode[1]	CDRmode[0]	MSPD int	reserved	data_rate[3]	data_rate[2]	data_rate[1]	data_rate[0]
M2h	*CDR_ctrlC*_N	VCO_divr[7]	VCO_divr[6]	VCO_divr[5]	VCO_divr[4]	VCO_divr[3]	VCO_divr[2]	VCO_divr[1]	VCO_divr[0]
M3h	*Out_ctrl*_N	outlvl[1]	outlvl[0]	reserved	reserved	data_pol_flip	dataout_en	MSPD int	MSPD int
M4h	*Preemp_ctrl*_N	reserved	MSPD int	MSPD int	MSPD int	MSPD int	preemph[2]	preemph[1]	preemph[0]
M5h	*Ineq_ctrl*_N	reserved	MSPD int	MSPD int	en_DCservo	in_eq[2]	en_ad_eq	in_eq[1]	in_eq[0]
M6h	*Phadj_ctrl*_N	i_trim[1]	i_trim[0]	r_sel[1]	r_sel[0]	phase_adj[3]	phase_adj[2]	phase_adj[1]	phase_adj[0]
M9h	*LOL_ctrl*_N	tacq_LOL[2]	tacq_LOL[1]	tacq_LOL[0]	narwin_LOL[3]	narwin_LOL[2]	narwin_LOL[1]	narwin_LOL[0]	widwin_LOL[0]
MAh	*Jitter_reduc*_N	MSPD int	MSPD int	lowjitter	MSPD int	MSPD int	MSPD int	MSPD int	MSPD int

Notes:
1. N = 0 for channel/CDR A0, N = 1 for channel/CDR A1,..., N = 7 for channel/CDR B3.
2. M = 4h for channel/CDR A0, M = 5h for channel/CDR A1,..., M = Bh for channel/CDR B3. For example channel/CDR A0 starts at address 40h, channel/CDR A1 at 50h, channel/CDR A2 at 60h, channel/CDR A3 at 70h, channel/CDR B0 at 80h, channel/CDR B1 at 90h, channel/CDR B2 at A0h, channel/CDR B3 at B0h.

2.1 Global Control Registers

2.1.1 Global Control Registers Nomenclature

1. Reserved bits: bits that exist and reserved for future use by Mindspeed.
2. Bits not defined and not reserved do not exist.
3. Do not write to reserved or undefined bits – operation not guaranteed.
4. MSPD internal: defines an internal function. Must always write the default value to MSPD internal bits. When in doubt, read back default value after reset.

2.1.2 Global Control

Table 2-2. Global Control (*Globctrl*: Address 00h)

Bits	Type	Default	Label	Description
7	R/W	1b	powerup	Powers up the IC by enabling the current references 1b: Power up the IC (device powerup) 0b: Power down the IC
6:2	R/W	00000b	MSPD internal	N/A
1	R/W	0b	Reserved	N/A
0	R/W	0b	clear_alm	Clears the *Alarm_LOA*, *Alarm_LOL* alarm registers (write only) 1b: Clear alarms 0b: Normal operation - latch alarm bits **Note**: Upon writing a 1b to this bit, it clears the registers, and user needs to write a 0b to enable the normal state.

2.1.3 Loopback Control

Table 2-3. Loopback Control (*Loopback*: Address 03h)

Bits	Type	Default	Label	Description
7:4	R/W	0000b	Reserved	N/A
3:0	R/W	0000b	loopback	A-side and B-side loopback configuration 1b: Enable loopback 0b: Disable loopback [3]: B-side loopback with order reversed [2]: B-side loopback [1]: A-side loopback with order reversed [0]: A-side loopback **Note:** No more than 1 of these 4 bits should be set to 1b at any time.

2.1.4 External Reference Frequency Divider Control (RFD)

Table 2-4. External Reference Frequency Divider Control (RFD) (*Refclk_ctrl****: Address 04h)***

Bits	Type	Default	Label	Description
7:4	R/W	0000b	Reserved	N/A
3:1	R/W	000b	ref_divr	Sets the divider ratio to scale down ***RefClk*** to the internal rate for FRA/LOA 000b: RFD = 1 001b: RFD = 2 010b: RFD = 4 011b: RFD = 8 100b: RFD = 12 101b: RFD = 16 110b: RFD = 32
0	R/W	0b	MSPD internal	N/A

2.1.5 Master Chip Reset

Table 2-5. Master Chip Reset (*Mastreset:* ***Address 05h)***

Bits	Type	Default	Label	Description
7:0	R/W	00000000b	rst	Same feature as hardware ***xRST***. Resets the entire IC AAh: Reset upon write to this register with AAh 00h: Normal operation **Note**: All other values are ignored.

2.1.6 IC Electronic Identification

Table 2-6. IC Electronic ID (*Chipcode****: Address 06h)***

Bits	Type	Default	Label	Description
7:0	R	19h	chipcode	This register contains the chipcode of this IC.

2.1.7 IC Revision Code

Table 2-7. IC Revision Code (*Revcode****: Address 07h)***

Bits	Type	Default	Label	Description
7:0	R	20h	revcode	This register contains the revision of the IC.

2.1.8 Input Hysteresis

Table 2-8. Input Hysteresis (*Input_hys*: Address 08h)

Bits	Type	Default	Label	Description
7:6	R/W	00b	Reserved	N/A
5	R/W	0b	en_hys	When enabled, 25 mV of hysteresis will be applied to all inputs. Useful in preventing noise from toggling inputs during quiescent periods of input patterns, such as seen in the InfiniBand polling pattern. 0b: Disable input hysteresis 1b: Enable input hysteresis
4:0	R/W	00000b	Reserved	N/A

2.1.9 Built In Self-Test (BIST) Receiver Channel Select

Table 2-9. Receiver Channel Select (*BISTrx_chsel*: Address 10h)

Bits	Type	Default	Label	Description
3	R/W	0b	Reserved	N/A
2:0	R/W	000b	chan	Selects which CDR to route into the BIST receiver (active when *BISTrx_ctrl* [1]=1) 000b: Output A0 to BIST 001b: Output A1 to BIST 010b: Output A2 to BIST 011b: Output A3 to BIST 100b: Output B0 to BIST 101b: Output B1 to BIST 110b: Output B2 to BIST 111b: Output B3 to BIST

2.1.10 Built In Self-Test (BIST) Receiver Main Control Register

Table 2-10. Built In Self-Test (BIST) Receiver Main Control Register (*BISTrx_ctrl*: Address 11h)

Bits	Type	Default	Label	Description
7	R/W	0b	MSPD internal	N/A
6	R/W	0b	rx_ctrclr	Clear the BIST Rx error count register, *BISTrx_error* (active when *BISTrx_ctrl* [1] = 1) 0b: Normal operation 1b: Clear register
5:2	R/W	0000b	rx_patt	Selects the BIST Rx test pattern (active when *BISTrx_ctrl* [1] = 1) 0000b: PRBS 2^7-1 0001b: PRBS 2^{15}-1 0010b: PRBS 2^{23}-1 0011b: PRBS 2^{31}-1 0100b: Fibre channel CJTPAT 0101b: Fibre channel CRPAT 0110b: 8b/10b countdown pattern 0111b: 16 bit user programmable pattern 1000b: 20 bit user programmable pattern
1	R/W	0b	en_rx	Powers up the BIST Rx 0b: Power down 1b: Power up and enable
0	R/W	1b	rx_rst	Resets the BIST Rx (recommended after powerup/enable, active when *BISTrx_ctrl* [1] = 1) 0b: Normal BIST Rx operation 1b: Reset of BIST Rx

2.1.11 Built In Self-Test (BIST) Receiver Bit Error Counter

Table 2-11. Built In Self-Test (BIST) Receiver Bit Error Counter (*BISTrx_error*: Address 12h)

Bits	Type	Default	Label	Description
7:0	R/W	00000000b	err	Bit error count (active when *BISTrx_ctrl* [1] = 1). This register is set to 00h upon reset, and is incremented for every bit error the BIST Rx receives, up to FFh. At FFh, the register will stay at this level until cleared.

2.1.12 Built In Self-Test (BIST) Transmitter Channel Select

Table 2-12. Built In Self-Test (BIST) Transmitter Channel Select (*BISTtx_chsel****: Address 14h)***

Bits	Type	Default	Label	Description
7:0	R/W	00000000b	tx_chan	Selects which output channel the BIST Tx outputs the test pattern on (active when *BISTtx_ctrl* [1] = 1) Bit map: 1b = BIST Tx on, 0b = BIST Tx off [7]: Output to CDR B3 [6]: Output to CDR B2 [5]: Output to CDR B1 [4]: Output to CDR B0 [3]: Output to CDR A3 [2]: Output to CDR A2 [1]: Output to CDR A1 [0]: Output to CDR A0 **Note**: Registers are set up to allow for multicasting BIST Tx output.

2.1.13 Built In Self-Test (BIST) Transmitter Main Control Register

Table 2-13. Built In Self-Test (BIST) Transmitter Main Control Register (*BISTtx_ctrl*: Address 15h)

Bits	Type	Default	Label	Description
7	R/W	0b	err_insert	Inserts a single bit error into the PRBS Tx 1b: Insert error 0b: Normal operation **Note:** Setting the register high allows one error to be inserted into the data stream. To insert another error, the user needs to clear, then set this register bit.
6	R/W	0b	rx2txclk	Selects the source of the clock for the BIST Tx PLL (active when *BISTtx_ctrl* [1] = 1) 0b: External reference frequency 1b: Recovered clock from BIST Rx **Note:** For the recovered clock option, the BIST Rx must be enabled with *BISTrx_ctrl* [1] = 1, and use the recovered clock from the same CDR selected by BIST Rx. This option only works for the full-rate case (DRD = 1).
5:2	R/W	0000b	tx_patt	Selects the BIST Tx test pattern (active when *BISTtx_ctrl* [1] = 1) 0000b: PRBS 2^7-1 0001b: PRBS 2^{15}-1 0010b: PRBS 2^{23}-1 0011b: PRBS 2^{31}-1 0100b: Fibre channel CJTPAT 0101b: Fibre channel CRPAT 0110b: 8b/10b countdown pattern 0111b: 16 bit user programmable pattern 1000b: 20 bit user programmable pattern
1	R/W	0b	en_tx	Powers up the BIST Tx and PLL 0b: Power down 1b: Power up and enable
0	R/W	1b	tx_rst	Resets the BIST Tx (recommended after powerup/enable; active when *BISTtx_ctrl* [1] = 1) 0b: Normal BIST Tx operation 1b: Reset of BIST Tx

2.1.14 Built In Self-Test (BIST) Transmitter PLL Loss of Lock Register

Table 2-14. Built In Self-Test (BIST) Transmitter PLL Loss of Lock Register (*BISTtx_LOLctrl *Address 17h)

Bits	Type	Default	Label	Description
7:5	R/W	101b	tacq_LOL	Sets the value for the LOL reference window **Code** **Value** 000b 128 001b 256 010b 512 011b 1024 100b 2048 101b 4096 110b 8192 111b 16384

Table 2-14. Built In Self-Test (BIST) Transmitter PLL Loss of Lock Register (BISTtx_LOLctrl Address 17h)

Bits	Type	Default	Label	Description
4:1	R/W	0011b	narwin_LOL	Sets the narrow LOL window for the LOL = H to LOL = L transition (transition to in lock threshold) **Code** **Value** 0000b 2 0001b 3 0010b 4 0011b 6 0100b 8 0101b 12 0110b 16 0111b 24 1000b 9 1001b 10 1010b 11 1011b 12 1100b 13 1101b 14 1110b 15 1111b 32
0	R/W	0b	widwin_LOL	Sets the wide LOL window for the LOL = L to LOL = H transition (transition to out of lock threshold) **Narrow Code** **Wide Code 0b** **Wide Code 1b** 0000b 3 8 0001b 4 12 0010b 6 16 0011b 8 24 0100b 12 32 0101b 16 32 0110b 24 32 0111b 32 32 1000b 12 32 1001b 12 32 1010b 12 32 1011b 16 32 1100b 16 32 1101b 16 32 1110b 16 32 1111b 32 32

2.1.15 Built In Self-Test (BIST) Transmitter PLL Control Register A

Table 2-15. Built In Self-Test (BIST) Transmitter PLL Control Register A (*BISTtx_PLL_ctrlA*: Address 18h)

Bits	Type	Default	Label	Description
7	R/W	0b	softreset	Resets the BIST transmitter PLL (assuming *BISTtx_ctrl* [1] = 1b) 0b: Normal operation 1b: Reset PLL only
6	R/W	0b	MSPD internal	N/A
5	R/W	0b	Reserved	N/A
4	R/W	0b	MSPD internal	N/A
3	R/W	0b	Reserved	N/A
2	R/W	1b	MSPD internal	N/A
1	R/W	0b	Reserved	N/A
0	R/W	1b	MSPD internal	N/A

2.1.16 Built In Self-Test (BIST) Transmitter PLL Control Register B

Table 2-16. Built In Self-Test (BIST) Transmitter PLL Control Register B (*BISTtx_PLL_ctrlB*: Address 19h)

Bits	Type	Default	Label	Description
7:6	R/W	11b	PLLmode	Determines state of the PLL. Must be enabled in addition to the BIST Tx (*BISTtx_ctrl* [1] = 1b) 00b: Channel active, PLL powered up 11b: Channel active, PLL powered down
5:4	R/W	01b	MSPD internal	N/A
3:0	R/W	0000b	data_rate	Data-rate divider (DRD): this divides down the VCO frequency to the desired data-rate 0000b: DRD = 1 0001b: DRD = 2 **Note**: Please consult $F_{vco,max}$ and $F_{vco,min}$ to determine the frequency range of each DRD ratio.

2.1.17 Built In Self-Test (BIST) Transmitter PLL Control Register C

Table 2-17. Built In Self-Test (BIST) Transmitter PLL Control Register C (*BISTtx_PLL_ctrlC*: Address 1Ah)

Bits	Type	Default	Label	Description
7:0	R/W	10000000b	VCO_divr	VCO comparison divider (VCD): this divider divides down the VCO to compare it with the divided down reference frequency. Binary value reflects the divider ratio 01h: Minimum value (VCD = 1) . . . FFh: Maximum value (VCO = 255)

2.1.18 Built In Self-Test (BIST) Transmitter 20 bit User Programmable Pattern

Table 2-18. Built In Self-Test (BIST) Transmitter 20 bit User Programmable Pattern (BIST_pattern0: Address 1Bh)

Bits	Type	Default	Label	Description
3:0	R/W	1100b	pattern	Sets the 20 bit user programmable pattern used in the BIST [3] MSB : Pattern bit#19 [2] : Pattern bit#18 [1] : Pattern bit#17 [0] LSB : Pattern bit#16

2.1.19 Built In Self-Test (BIST) Transmitter 16/20-bit User Programmable Pattern

Table 2-19. Built In Self-Test (BIST) Transmitter 16/20 bit User Programmable Pattern (BIST_pattern1: Address 1Ch)

Bits	Type	Default	Label	Description
7:0	R/W	11001100b	pattern	Sets the 16/20 bit user programmable pattern used in the BIST [7] MSB : Pattern bit#15 [6] : Pattern bit#14 [5] : Pattern bit#13 [4] : Pattern bit#12 [3] : Pattern bit#11 [2] : Pattern bit#10 [1] : Pattern bit#9 [0] LSB : Pattern bit#8

2.1.20 Built In Self-Test (BIST) Transmitter 16/20-bit User Programmable Pattern

Table 2-20. Built In Self-Test (BIST) Transmitter 16/20 bit User Programmable Pattern (BIST_pattern2: Address 1Dh)

Bits	Type	Default	Label	Description
7:0	R/W	11001100b	pattern	Sets the 16/20 bit user programmable pattern used in the BIST [7] MSB : Pattern bit#7 [6] : Pattern bit#6 [5] : Pattern bit#5 [4] : Pattern bit#4 [3] : Pattern bit#3 [2] : Pattern bit#2 [1] : Pattern bit#1 [0] LSB : Pattern bit#0

2.1.21 Built In Self-Test (BIST) Transmitter Alarm

Table 2-21. Built In Self-Test (BIST) Transmitter Alarm (*BISTtx_alarm*: Address 1Fh)

Bits	Type	Default	Label	Description
7	R	0b	tx_LOL	Loss of lock for the BIST Tx PLL (active when *BISTtx_ctrl* [1] = 1) 0b: Normal operation 1b: Loss of lock
6:5	R/W	00b	Reserved	N/A
4:0	R/W	00000b	MSPD internal	N/A

2.1.22 Internal Junction Temperature Monitor

Table 2-22. Internal Junction Temperature Monitor (*Temp_mon*: Address 20h)

Bits	Type	Default	Label	Description
3:2	R/W	00b	Reserved	N/A
1	R/W	0b	en_temp_mon	Power up and enable the temperature monitor 1b: Power up and enable temperature monitor 0b: Disable temperature monitor
0	R/W	0b	strobe_temp	Strobes ADC for temperature measurement 1b: Read temperature 0b: Ok to read temperature **Note**: To strobe ADC, a rising edge should be provided by writing 1b, then writing 0b to return to default state.

2.1.23 Internal Junction Temperature Value

Table 2-23. Internal Junction Temperature Value (*Temp_value*: Address 21h)

Bits	Type	Default	Label	Description
3:0	R	N/A	temp	A read of these bits returns the temperature from the last write cycle (to strobe_temp)

Junction Temperature	temp	Condition
Tc ≥ 130°C	1100b	High-alarm
130°C > Tc ≥ 120°C	1011b	High-alarm
120°C > Tc ≥ 110°C	1010b	High-warning
110°C > Tc ≥ 100°C	1001b	Normal
100°C > Tc ≥ 90°C	1000b	Normal
90°C > Tc ≥ 80°C	0111b	Normal
80°C > Tc ≥ 10°C	0110b	Normal
10°C > Tc ≥ 0°C	0101b	Low-warning
0°C > Tc ≥ -10°C	0100b	Low-alarm
-10°C > Tc ≥ -20°C	0011b	Low-alarm
-20°C > Tc ≥ -30°C	0010b	Low-alarm
-30°C > Tc ≥ -40°C	0001b	Low-alarm
-40°C > Tc	0000b	Low-alarm

2.1.24 CDR Loss of Lock Register Alarm Status

Table 2-24. CDR Loss of Lock Register Alarm Status (*Alarm_LOL*: Address 30h)

Bits	Type	Default	Label	Description
7:0	R	N/A	LOL	Latched loss of lock alarm status 1b = loss of CDR lock, 0b = normal operation [7]: CDR B3 [6]: CDR B2 [5]: CDR B1 [4]: CDR B0 [3]: CDR A3 [2]: CDR A2 [1]: CDR A1 [0]: CDR A0 **Note:** After a clear (*Globctrl* [0] = 1), this register is cleared and will latch any new alarms that make a L to H transition, and set any pre-existing alarm conditions to H.

2.1.25 Loss of Activity Register Alarm Status

Table 2-25. Loss of Activity Register Alarm Status (*Alarm_LOA*: Address 31h)

Bits	Type	Default	Label	Description
7:0	R	N/A	LOA	Latched loss of activity alarm status 1b = loss of input signal, 0b = normal operation [7]: CDR B3 [6]: CDR B2 [5]: CDR B1 [4]: CDR B0 [3]: CDR A3 [2]: CDR A2 [1]: CDR A1 [0]: CDR A0 **Note:** After a clear (*Globctrl* [0] = 1), this register is cleared and will latch any new alarms that make a L to H transition, and set any pre-existing alarm conditions to H.

2.2 Individual Channel/CDR Control

Multiple Instance Nomenclature

1. N = 0 for channel/CDR A0, N = 1 for channel/CDR A1,..., N = 7 for channel/CDR B3.
2. M = 4h for channel/CDR A0, M = 5h for channel/CDR A1,..., M = Bh for channel/CDR B3. For example channel/CDR A0 starts at address 40h, channel/CDR A1 at 50h, channel/CDR A2 at 60h, channel/CDR A3 at 70h, channel/CDR B0 at 80h, channel/CDR B1 at 90h, channel/CDR B2 at A0h, channel/CDR B3 at B0h.

2.2.1 CDR N Control Register A

Table 2-26. CDR N Control Register A (*CDR_ctrlA_N*: Address M0h)

Bits	Type	Default	Label	Description
7	R/W	0b	softreset	Resets individual CDR N (setup registers remain unchanged; need to softreset after rate change) 0b: Normal operation 1b: Reset single CDR only
6	R/W	0b	MSPD internal	N/A
5	R/W	0b	inh_force	Manual control of the output inhibit if *CDR_ctrlA*_N[3] = 0 0b: Normal operation 1b: Forced inhibit
4	R/W	0b	MSPD internal	N/A
3	R/W	1b	autoinh_en	Auto inhibit of the output (***DoutP*** = H, ***DoutN*** = L) if CDR N has a LOL or LOA condition 0b: Auto inhibit disabled, *CDR_ctrlA*_N[5] determines inhibit force state 1b: Auto inhibit enabled
2	R/W	1b	MSPD internal	N/A
1	R/W	1b	LOA_en	Enables the transition density based loss of activity detector for output N 0b: Disable and power down LOA circuit 1b: Enable LOA circuit
0	R/W	1b	MSPD internal	N/A

2.2.2 CDR N Control Register B

Table 2-27. CDR N Control Register B (CDR_ctrlB_N: Address M1h)

Bits	Type	Default	Label	Description
7:6	R/W	00b	CDRmode	Determines state of the PLL 00b: CDR powered up and active 01b: CDR powered up and bypassed 10b: CDR powered down (no signal through) 11b: CDR powered down and bypassed
5	R/W	0b	MSPD internal	N/A
4	R/W	0b	Reserved	N/A
3:0	R/W	0000b	data_rate	Data-rate divider (DRD): this divides down the VCO frequency to the desired data-rate to match input data-rate 0000b: DRD = 1 0001b: DRD = 2 **Note:** Please consult $F_{vco,max}$ and $F_{vco,min}$ to determine frequency range of each DRD ratio.

2.2.3 CDR N Control Register C

Table 2-28. CDR N Control Register C (CDR_ctrlC_N: Address M2h)

Bits	Type	Default	Label	Description
7:0	R/W	10000000b	VCO_divr	VCO comparison divider (VCD): this divides down the VCO, to compare it with the scaled reference clock, for use in the FRA/LOA mode. Binary value reflects the divider ratio 1h: Minimum value (VCD= 1) . . . FFh: Maximum value (VCD = 255)

2.2.4 Output Buffer Control for CDR N

Table 2-29. Output Buffer Control for CDR N (*Out_ctrl_N*: Address M3h)

Bits	Type	Default	Label	Description
7:6	R/W	10b	outlvl	Determines the output swing of a data buffer for CDR N In PCML mode: 00b: Power down 01b: 600 mV 10b: 1000 mV 11b: 1300 mV For InfiniBand, the output swing is increased to: 00b: Power down 01b: 1000 mV 10b: 1300 mV 11b: 1600 mV
5:4	R/W	00b	Reserved	N/A
3	R/W	0b	data_pol_flip	Flips the polarity of the output data 0b: Normal 1b: Polarity flip
2	R/W	1b	dataout_en	Enables the data output driver N 1b: Data output enabled to level specified in *Out_ctrl*_N[7:6] 0b: Data output disabled and powered down
1:0	R/W	00b	MSPD internal	N/A

2.2.5 Output Buffer Pre-Emphasis Control for Output N

Table 2-30. Output Buffer Pre-Emphasis Control for Output N (*Preemp_ctrl_N*: Address M4h)

Bits	Type	Default	Label	Description
7	R/W	0b	Reserved	Default = 0b
6:3	R/W	1000b	MSPD internal	N/A
2:0	R/W	000b	preemph	Selects the digital pre-emphasis level 111b: 200% 110b: 150% 101b: 100% 100b: 75% 011b: 50% 010b: 37.5% 001b: 25% 000b: Pre-emphasis off

2.2.6 Input Equalization Control for Output N

Table 2-31. Input Equalization Control for Output N (*Ineq_ctrl_*N*: Address M5h)***

Bits	Type	Default	Label	Description
7	R/W	0b	Reserved	N/A
6:5	R/W	00b	MSPD internal	N/A
4	R/W	1b	en_DCservo	Enables DC servo in the input channel to remove offset based deterministic jitter 0b: DC servo D_j attenuator off 1b: DC servo D_j attenuator on
3, 1:0	R/W	000b	in_eq	Selects the input equalization level 111b: Maximum input equalization level . . . 100b: Nominal input equalization level . . . 001b: Minimum input equalization level 000b: Input equalization disabled **Note:** The 100b setting is optimized for PCB trace lengths between 10 - 46 inches, although other settings may be optimal for some applications. Bit 2 must be set to zero.
2	R/W	0b	en_ad_eq	This bit is used to select adaptive input equalization (AIE) over configurable input equalization (IE). When AIE is selected, bits [3, 1:0] have no effect. 0b: Disable AIE 1b: Enable AIE **Note:** Whenever possible, configurable IE should be selected over AIE since configurable IE performance is more consistent across devices.

2.2.7 CDR N Loop Bandwidth and Data Sampling Point Adjust

Table 2-32. CDR N Loop Bandwidth and Data Sampling Point Adjust (*Phadj_ctrl_N*: Address M6h)

Bits	Type	Default	Label	Description
7:6	R/W	10b	i_trim	Adjusts the charge-pump current; the loop bandwidth (F_{LBW}) scales proportionally 00b: 0.65x nominal value 01b: 0.8x nominal value 10b: Nominal 11b: 1.15x nominal value
5:4	R/W	10b	r_sel	Adjusts the resistor of the CDR loop filter; the loop bandwidth (F_{LBW}) scales proportionally 00b: 0.72x nominal value 01b: Nominal 10b: 2.6x nominal value
3:0	R/W	0000b	phase_adj	Adjusts the static phase offset (sampling point) of the data 1111b: -122.5 mUI 1110b: -105 mUI 1101b: -87.5 mUI 1100b: -70 mUI 1011b: -52.5 mUI 1010b: -35.0 mUI 1001b: -17.5 mUI 1000b: 0 mUI 0000b: 0 mUI 0001b: 17.5 mUI 0010b: 35.0 mUI 0011b: 52.5 mUI 0100b: 70.0 mUI 0101b: 87.5 mUI 0110b: 105 mUI 0111b: 122.5 mUI

2.2.8 CDR N FRA LOL Window Control

Table 2-33. CDR N FRA LOL Window Control (*LOL_ctrl_N*: Address M9h)

Bits	Type	Default	Label	Description
7:5	R/W	101b	tacq_LOL	Sets the value for the LOL reference window **Code** **Value** 000b 128 001b 256 010b 512 011b 1024 100b 2048 101b 4096 110b 8192 111b 16384

Table 2-33. CDR N FRA LOL Window Control (*LOL_ctrl_N*: Address M9h)

Bits	Type	Default	Label	Description
4:1	R/W	0011b	narwin_LOL	Sets the narrow LOL window for the LOL = H to LOL = L transition (transition to in lock threshold) **Code** **Value** 0000b 2 0001b 3 0010b 4 0011b 6 0100b 8 0101b 12 0110b 16 0111b 24 1000b 9 1001b 10 1010b 11 1011b 12 1100b 13 1101b 14 1110b 15 1111b 32
0	R/W	0b	widwin_LOL	Sets the wide LOL window for the LOL = L to LOL = H transition (transition to out of lock threshold) **Narrow Code** **Wide Code 0b** **Wide Code 1b** 0000b 3 8 0001b 4 12 0010b 6 16 0011b 8 24 0100b 12 32 0101b 16 32 0110b 24 32 0111b 32 32 1000b 12 32 1001b 12 32 1010b 12 32 1011b 16 32 1100b 16 32 1101b 16 32 1110b 16 32 1111b 32 32

2.2.9 Jitter Reduction Control

Table 2-34. Jitter Reduction Control (*Jitter_reduc_*N***: Address MAh)***

Bits	Type	Default	Label	Description
7:6	R/W	01b	MSPD internal	N/A
5	R/W	0b	lowjitter	When data-rate is in the range (2.45 Gbps - 2.55 Gbps)/DRD, setting this bit to 1b will reduce output jitter (DRD is data-rate divider). 1b: Reduce output jitter 0b: Normal operation **Note:** This bit should be set to 1b for InfiniBand, SONET STS-N, PCI Express, and Gigabit Ethernet applications.
4:0	R/W	N/A	MSPD internal	Any value may be written to this register with no effect on performance.

3.0 Product Specifications

3.1 Absolute Maximum Ratings

These are the absolute maximum ratings at or beyond which the device can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

Table 3-1. Absolute Maximum Ratings

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DVdd_I/O	Digital I/O power		0	1.8/2.5/3.3	3.6	V
AVdd_I/O	Analog I/O power		0	1.8/2.5	2.7	V
AVdd_Core	Analog core power	1	0	1.2	1.5	V
DVdd_Core	Digital core power	1	0	1.2	1.5	V
Tst	Storage temperature		–65	—	+150	°C
ESD	Human body model (low-speed)		2000		—	V
ESD	Human body model (high-speed)		2000		—	V
ESD	Charged device model		500		—	V

Notes:
1. Apply voltage to core pins if internal regulator is disabled. If enabled, pins should be floating with by-pass to ***Vss***.

3.2 Recommended Operating Conditions

Table 3-2. Recommended Operating Conditions

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DVdd_I/O	Digital I/O power	2	—	1.8/2.5/3.3	—	V
AVdd_I/O	Analog I/O power	2	—	1.8/2.5	—	V
AVdd_Core	Analog core power	1, 2	—	1.2	—	V
DVdd_Core	Digital core power	1, 2	—	1.2	—	V
T_a	Ambient temperature	—	- 40	—	85	°C
θ_{ja}	Junction to ambient thermal resistance	3	—	24	—	°C/W

Notes:
1. ***AVdd_Core*** or ***DVdd_Core*** provided from external source (internal regulator disabled ***xRegu_En*** = H).
2. Typical value +/- 5% is acceptable.
3. With forced convection of 1 m/s and 2.5 m/s, θ_{ja} is decreased to 18 °C/W and 16 °C/W respectively.

3.3 Power Dissipation

Table 3-3. DC Power Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
Idd	Case 1: current consumption for output swing = 600 mV CML, internal regulator = on	1, 2	—	640	800	mA
Pdiss	Power dissipation at 1.8V	—	—	1.2	1.5	W
Pdiss	Power dissipation at 2.5V	—	—	1.6	2.1	W
Idd	Case 2: current consumption for output swing = 1000 mV CML, internal regulator = on	1, 2	—	700	870	mA
Pdiss	Power dissipation at 1.8V	—	—	1.3	1.7	W
Pdiss	Power dissipation at 2.5V	—	—	1.8	2.3	W
	Case 3: output swing = 600 mV CML, internal regulator = off	1				
Idd_core	Core current consumption	—	—	510	610	mA
Idd_io	Input/Output buffers current consumption	—		100	120	mA
Pdiss	Power dissipation at 1.2V core, 1.8V I/O	—	—	800	990	mW
Pdiss	Power dissipation at 1.2V core, 2.5V I/O	—	—	910	1100	mW
Idd	Case 4: current consumption for output swing = 1600 mV InfiniBand, internal regulator = on	1, 2	—	770	950	mA
Pdiss	Power dissipation at 1.8V	—	—	1.4	1.8	W
Pdiss	Power dissipation at 2.5V	—	—	1.9	2.5	W
	Case 5: output swing = 1600 mV InfiniBand, internal regulator = off	1, 2				
Idd_core	Core current consumption	—	—	530	620	mA
Idd_io	Input/Output buffers current consumption	—		210	270	mA
Pdiss	Power dissipation at 1.2V core, 1.8V I/O	—	—	1.0	1.3	W
Pdiss	Power dissipation at 1.2V core, 2.5V I/O	—	—	1.2	1.5	W

Notes:
1. Specified at recommended operating conditions – see Table 3-2.
2. Thermal design such as thermal pad vias on PCB must be considered.

3.4 Input/Output Specifications

Table 3-4. Two-Wire Serial Interface CMOS I/O Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
V_{OH}	Output logic high I_{OH} = –3 mA	1, 2	0.8 x ***DVdd_I/O***	***DVdd_I/O***	—	V
V_{OL}	Output logic low I_{OL} = 24 mA	1, 2	—	0.0	0.2 x ***DVdd_I/O***	V
I_{OL}	Output current (logic low)	1	0	—	10	mA
I_{OH}	Output current (logic high)	1	10	—	—	mA
V_{IH}	Input logic high	1	0.75 x ***DVdd_I/O***	—	3.6	V
V_{IL}	Input logic low	1	0	—	0.25 x ***DVdd_I/O***	V
I_{IH}	Input current (logic high)	1	–100	—	100	µA
I_{IL}	Input current (logic low)	1	–100	—	100	µA
t_r	Output rise time (20-80%)	1	—	—	250	ns
t_f	Output fall time (20-80%)	1	—	—	250	ns
C2wire	Input capacitance of ***MF4*** & ***MF5*** in two-wire interface	1, 3	—	—	10	pF

Notes:
1. Specified at recommended operating conditions – see Table 3-2.
2. ***DVdd_I/O*** can be chosen independently from ***AVdd_I/O***.
3. Two-wire serial output mode can drive 500 pF.

Table 3-5. High-Speed Input Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DR_{IN}	Input signal data-rate	1, 3	1	—	3.2	Gbps
V_{ID}	Input differential voltage (P-P)	1, 3, 4	125	—	2000	mV
V_{ICM}	Input common-mode voltage	1	800	—	***AVdd_Core***	mV
R_{IN}	Input termination to ***VddT***	1, 6	45	50	65	Ω
S_{11}	Input return loss (40 MHz to 2.5 GHz)	1	—	–15.0	—	dB
S_{11}	Input return loss (2.5 GHz to 5 GHz)	1	—	–5.0	—	dB
—	Maximum DC input current	1, 5	—	—	25	mA

Notes:
1. Specified at recommended operation conditions – see Table 3-2.
2. Designed for seamless interface to PCML.
3. Example 1200 mV_{pp} differential = 600 mV_{pp} for each single-ended terminal.
4. Minimum input level defined as error free operation at 10^{-12} BER.
5. Computed as the current through 50 ohms from the voltage difference between the input voltage common mode to ***VddT.***
6. See Figure 3-1 for input termination circuit.

Figure 3-1. High-Speed Data Input Internal Circuitry

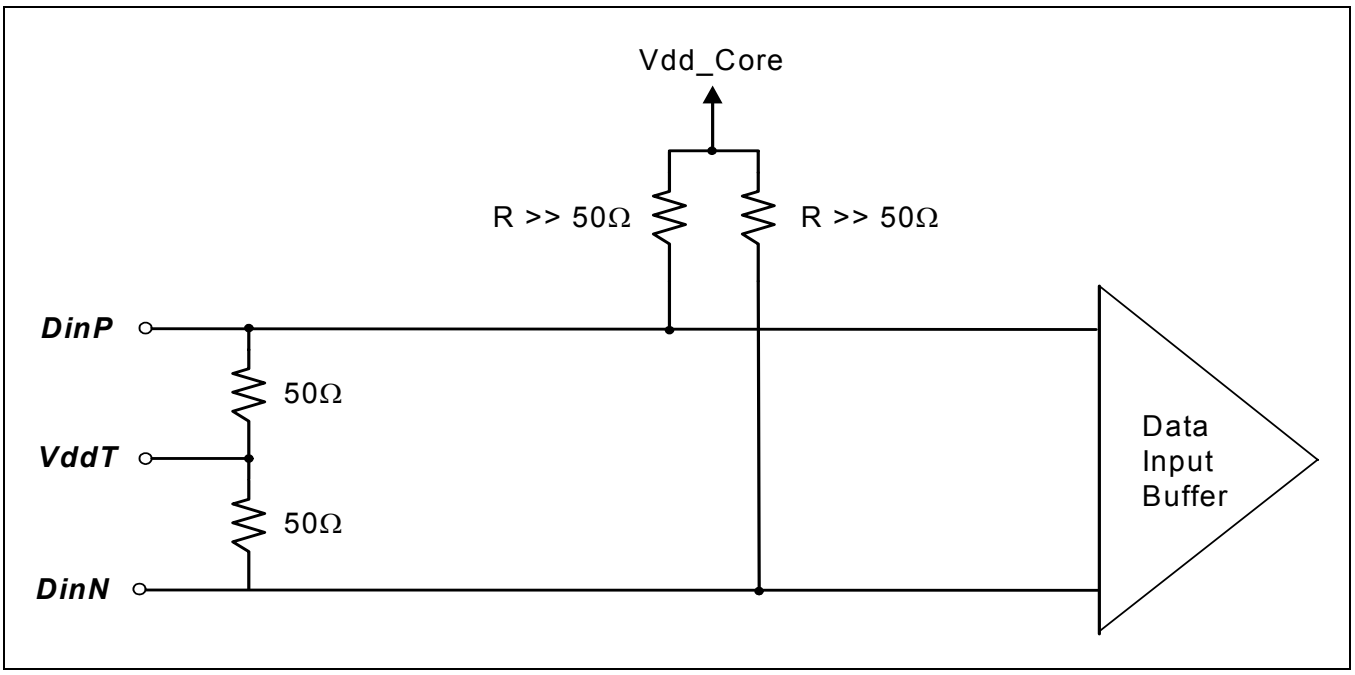


Table 3-6. PCML (Positive Current Mode Logic) Output Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DR_{OUT}	Output signal data-rates	1	1	—	3.2	Gbps
t_r/t_f	Rise/Fall time (20-80%) for all levels	1	—	100	130	ps
V_{OH}	Low Swing: output logic high (single-ended)	1	***AVdd_I/O*** – 65	—	***AVdd_I/O***	mV
V_{OL}	Low Swing: output logic low (single-ended)	1	***AVdd_I/O*** – 370	—	***AVdd_I/O*** – 240	mV
V_{OD}	Low Swing: differential swing	1, 2	400	500	650	mV
V_{OH}	Medium Swing: output logic high (single-ended)	1	***AVdd_I/O*** – 85	—	***AVdd_I/O***	mV
V_{OL}	Medium Swing: output logic low (single-ended)	1	***AVdd_I/O*** – 600	—	***AVdd_I/O*** – 400	mV
V_{OD}	Medium Swing: differential swing	1, 2	700	850	1100	mV
V_{OH}	High Swing: output logic high (single-ended)	1	***AVdd_I/O*** – 100	—	***AVdd_I/O***	mV
V_{OL}	High Swing: output logic low (single-ended)	1	***AVdd_I/O*** – 770	—	***AVdd_I/O*** – 500	mV
V_{OD}	High Swing: differential swing	1, 2	1000	1100	1200	mV
V_{OH}	InfiniBand Swing: output logic high (single-ended)	1	***AVdd_I/O*** – 120	—	***AVdd_I/O***	mV
V_{OL}	InfiniBand Swing: output logic low (single-ended)	1	***AVdd_I/O*** – 1000	—	***AVdd_I/O*** – 600	mV
V_{OD}	InfiniBand Swing: differential swing	1, 2	1050	1500	1900	mV
R_{OUT}	Output termination to ***AVdd_I/O***	1	45	50	65	Ω
S_{22}	Output return loss (40 MHz to 2.5 GHz)	1	—	–15.0	—	dB
S_{22}	Output return loss (2.5 GHz to 5 GHz)	1	—	–5.0	—	dB

Notes:
1. Specified at recommended operating conditions – see Table 3-2.
2. Example 1200 mV $_{P-P}$ differential = 600 mV $_{P-P}$ for each single-ended terminal.
3. All output swings defined with pre-emphasis off.

Table 3-7. Input Equalization Performance Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DR_{IN}	Input signal data-rates	1	1	—	3.2	Gbps
—	Maximum error-free distance at 3.1875 Gbps	1, 2, 3, 5	—	—	60	in
—	Maximum error-free distance at 2.125 Gbps	1, 2, 3, 5	—	—	72	in

Notes:
1. Specified at recommended operating conditions – see Table 3-2.
2. Performance measured on standard FR4 backplane such as standards provided by TYCO for 10GE XAUI.
3. Measured with PCML driver WITHOUT output pre-emphasis at a minimum launch voltage of 1 Vpp output swing at beginning of line.
4. Combined input equalization + output pre-emphasis performance will be better than individual performance, but less than the sum of the two lengths.
5. Default setting optimized for driving 10 - 46 in of PCB trace length. Equalizer can be configured for longer reach using two-wire interface.
6. For applications where input equalization setting cannot be dynamically re-configured, adaptive input equalization may be enabled. See Section 1.1.10 for additional details.

Table 3-8. Output Pre-Emphasis Performance Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DR_{OUT}	Output signal data-rates	1	1	—	3.2	Gbps
—	Maximum error-free distance at 3.1875 Gbps	1, 2	—	—	40	in
—	Maximum error-free distance at 2.125 Gbps	1, 2	—	—	60	in

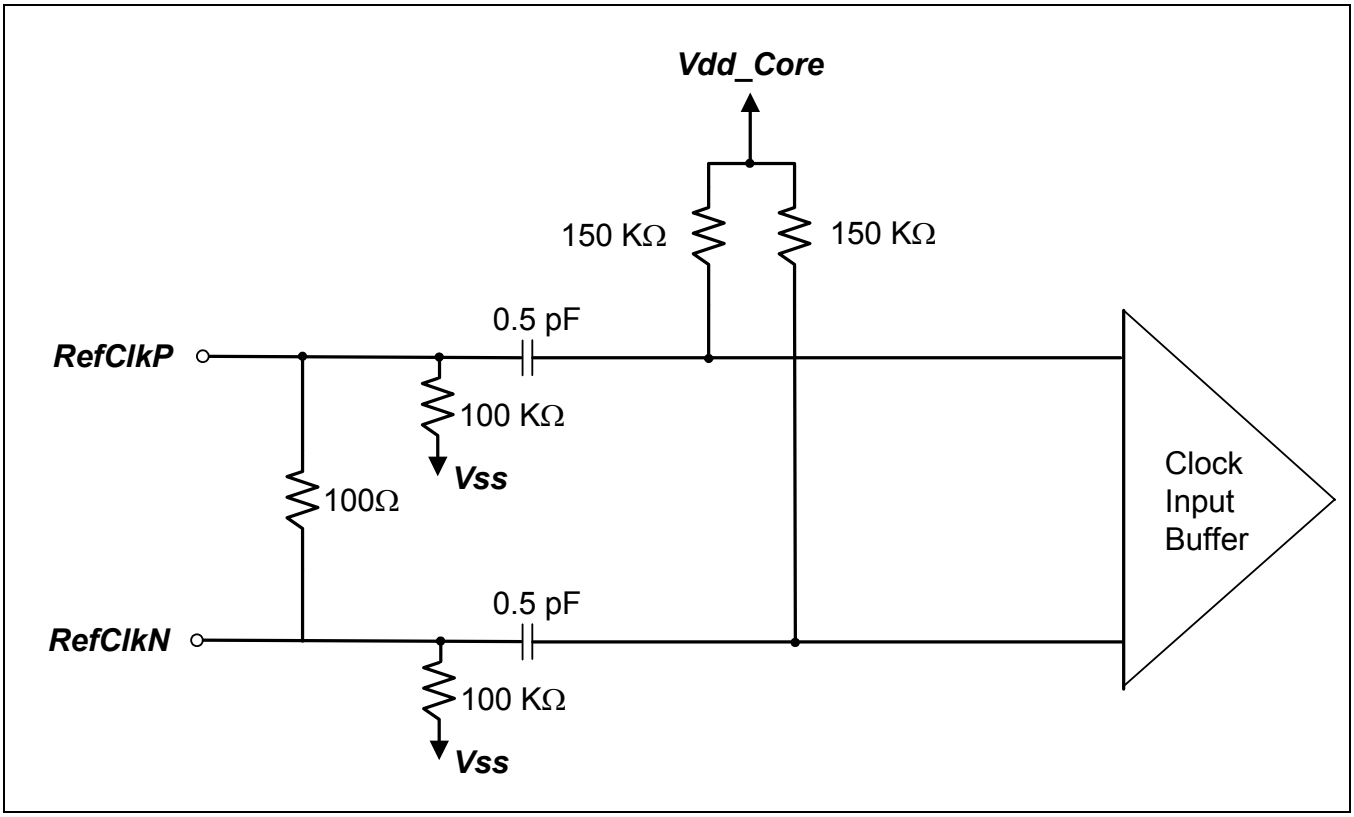
Notes:
1. Specified at recommended operating conditions – see Table 3-2.
2. Performance measured on standard FR4 backplane such as standards provided by TYCO for 10GE XAUI.
3. Measured with PCML receiver without input equalization, using PCML output driver at 1300 mVpp output swing at beginning of line.
4. Combined input equalization + output pre-emphasis performance will be better than individual performance, but less than the sum of the two lengths.

Table 3-9. Reference Clock Input

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
F_{ref}	Input frequency (*Refclk_ctrl* [3:1] = 000b)	1	10	19.44	25	MHz
F_{ref}	Input frequency (*Refclk_ctrl* [3:1] = 001b)	1	20	38.88	50	MHz
F_{ref}	Input frequency (*Refclk_ctrl* [3:1] = 010b)	1	40	62.5	100	MHz
F_{ref}	Input frequency (*Refclk_ctrl* [3:1] = 011b)	1	80	125	200	MHz
F_{ref}	Input frequency (*Refclk_ctrl* [3:1] = 100b)	1	120	250	300	MHz
F_{ref}	Input frequency (*Refclk_ctrl* [3:1] = 101b)	1	160	311.04	400	MHz
F_{ref}	Input frequency (*Refclk_ctrl* [3:1] = 110b)	1	320	622.08	800	MHz
V_{ID}	Input differential voltage (P-P)	1, 2, 3	100	—	1600	mV
V_{ICM}	Input common-mode voltage	1, 3	250	—	***AVdd_I/O***	mV
—	Input duty cycle	1	40	50	60	%
—	Frequency stability	1	—	—	100	ppm
R_{IN}	Differential termination	1, 3	—	100	—	Ω
—	Internal pull-down to ***Vss***	1	—	100	—	kΩ
—	Maximum DC input current	1	—	—	15	mA

Notes:
1. Specified at recommended operation conditions – see Table 3-2.
2. Example 1200 mV_{pp} differential = 600 mV_{pp} for each single-ended terminal.
3. Input can accept a CMOS single-ended clock on differential P terminal when differential N terminal is decoupled to ground with a large enough capacitor. CMOS input will then see an effective 100Ω load.
4. See Figure 3-2 for input termination circuit.

Figure 3-2. Reference Clock Input Internal Circuitry



3.5 CDR Performance Specifications

Table 3-10. CDR High-Speed Performance

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DR_{IN}	Input signal data rate (NRZ data) divider ratio = 1	1	2	—	3.2	Gbps
DR_{IN}	Input signal data rate (NRZ data) divider ratio = 2	1	1	—	1.6	Gbps
J_{TOL}	Jitter tolerance (Figure 3-3)	1, 2	—	0.625	—	UI
R_j	Output data random jitter (pp)	1, 7	—	—	100	mUI
D_j	Output data deterministic jitter (pp)	1, 7	—	—	150	mUI
T_j	Output data total jitter (pp)	1, 7	—	—	250	mUI
J_{pp}	Output data broadband jitter (pp)	1, 8, 10	—	135	230	mUI
J_{rms}	Output data broadband jitter (rms)	1, 8, 10	—	22	40	mUI
D_{DC}	Output data duty cycle	1	45	50	55	%
T_{LAT}	Latency from input to output	1, 10	—	615	800	ps
CH_{SK}	Channel to channel output data skew (utilizing CDR)	1	—	20	65	ps
T_{init}	Initialization time	1, 3, 6		2	—	ms
T_{FRA}	Frequency acquisition time	1, 4		0.4	—	ms
T_{PLL}	Phase lock time with 100 ppm delta F	1, 5			100	ns
T_{PLL}	Phase lock time with 0 ppm delta F	1, 5			50	ns

Notes:
1. Specified at recommended operating conditions – see Table 3-2.
2. Jitter tolerance specified with input equalization and output pre-emphasis disabled, utilizing PRBS 2^{23}-1.
3. Time after power up, reset, or data-rate change.
4. Time from application of valid data to lock within +/-20% of lock phase.
5. Defined as when phase settles to within 20% of lock phase.
6. After reset (master or soft), initialization takes place, then frequency acquisition.
7. R_j, D_j, T_j represent jitter measured to BER of 10^{-12} per T11.2 FC-PI-2 specifications.
8. Broadband jitter defined as jitter measured on sampling oscilloscope without the use of filters.
9. Maximum value specified incorporates asynchronous aggressors.
10. When the CDR is enabled, the latency is the number shown plus 1.5 times the period of the clock. For example, when operating the CDR at 2.5 Gbps, the typical latency is 615 ps + 600 ps = 1.215 ns. When the CDR is bypassed, the latency through the M21050 is the number listed.

Figure 3-3. Jitter Tolerance Specification Mask

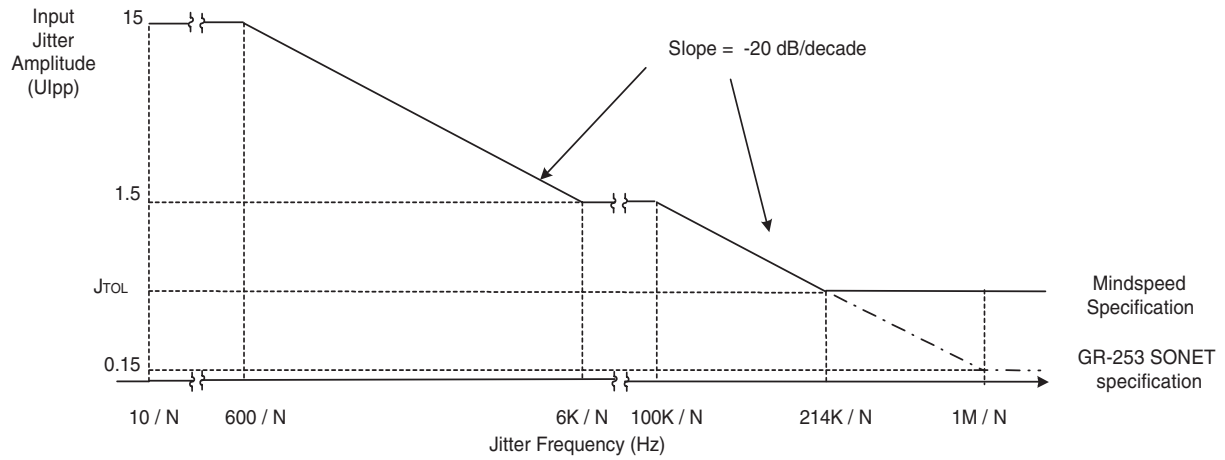


Table 3-11. CDR Alarm Performance

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DT_{LOA}	***xLOA*** decision time	1, 3	—	26	—	µs
TD_{low}	***xLOA*** assertion transition density threshold (***xLOA*** = H to L)	1, 3	0	—	25	%
TD_{high}	***xLOA*** de-assertion transition density threshold (***xLOA*** = L to H)	1, 3	25	—	100	%
DT_{LOL}	***xLOL*** decision time (measurement time)	1, 2	10	420	3275	µs
WRW	***xLOL*** assertion frequency threshold (***xLOL*** = H to L)	1, 2	±185	±1950	±250000	ppm
NRW	***xLOL*** de-assertion frequency threshold (***xLOL*** = L to H)	1, 2	±120	±1450	±250000	ppm

Notes:
1. Specified at recommended operating conditions – see Table 3-2.
2. Actual time is set with LOL window. Typical is the default value. Minimum and maximum indicate dynamic range.
3. Fixed values.

3.6 Package Drawings and Surface Mount Assembly Details

The M21050 is assembled in 72-pin 10 mm x 10 mm MicroLeadFrame (MLF) packages. This is a plastic encapsulated package with a copper leadframe. The MLF is a leadless package with lands on the bottom surface of the package.

The exposed die paddle serves as the IC ground (***Vss***), and the primary means of thermal dissipation. This die paddle should be soldered to the PCB. A cross-section of the MLF package can be found in Figure 3-4.

Figure 3-4. Cross-Section of MLF Package

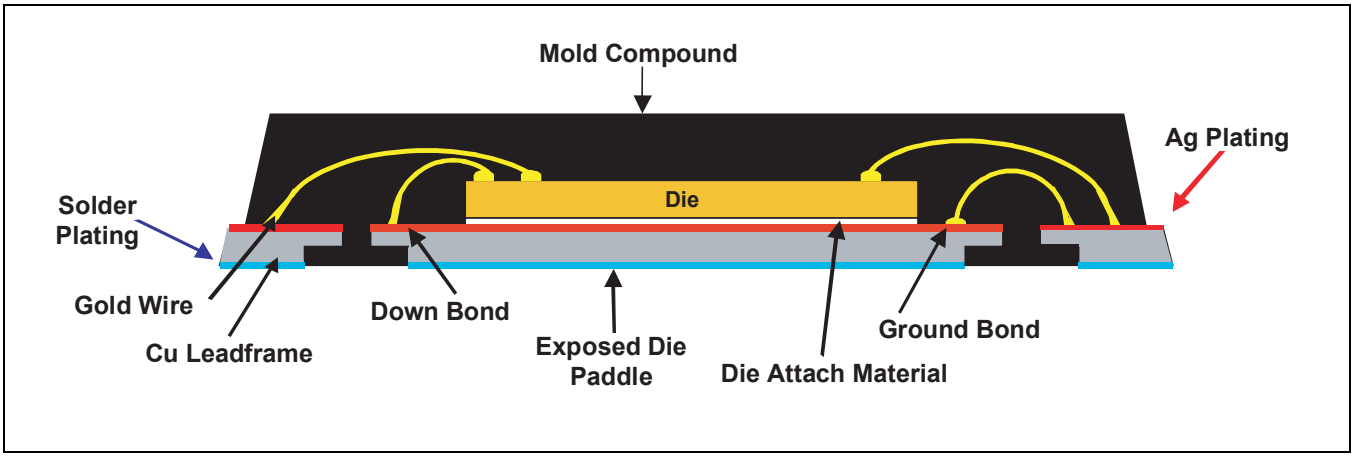
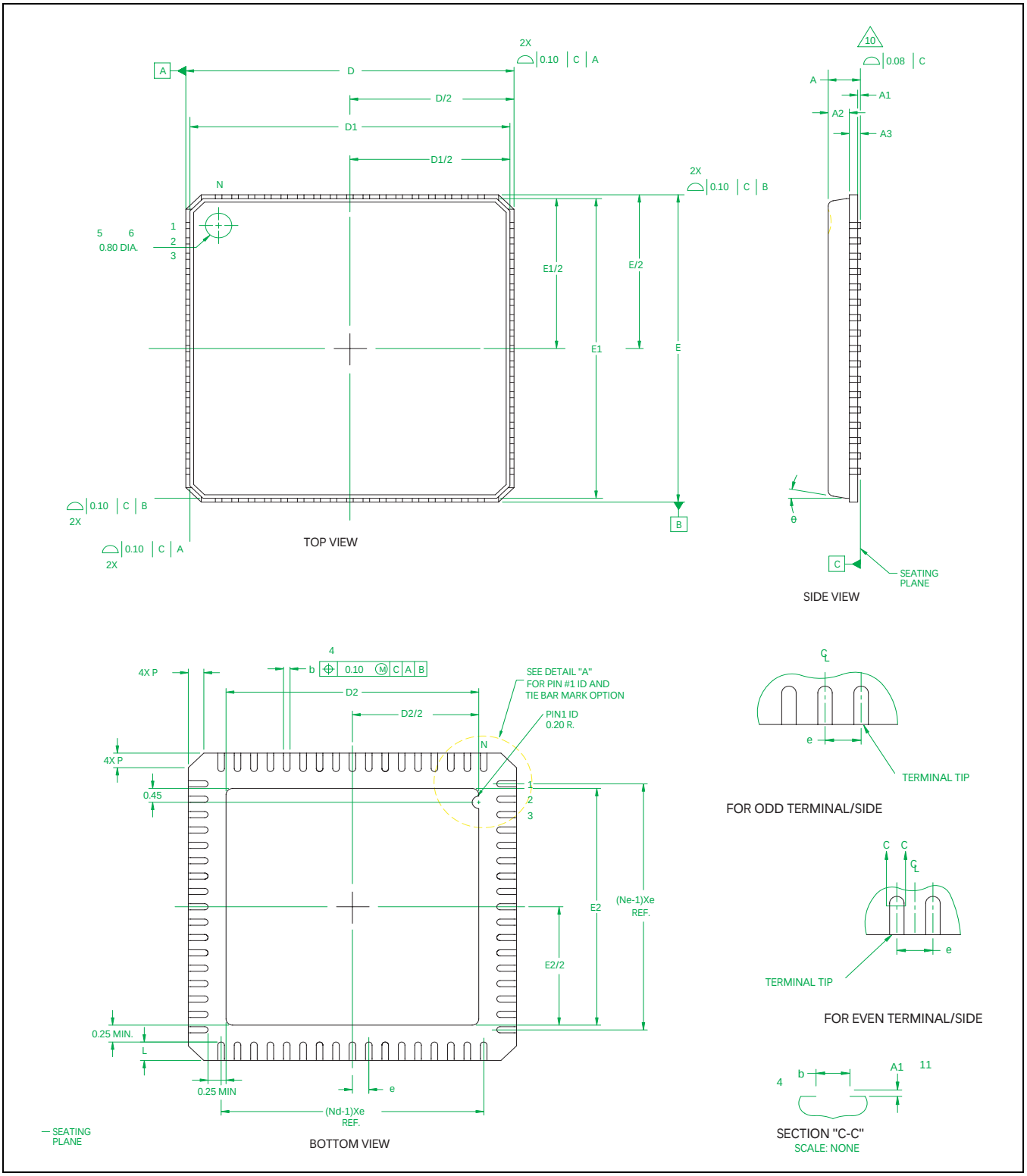


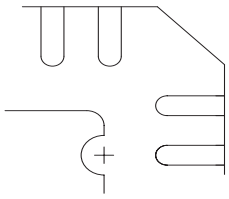
Figure 3-5 shows the package outline drawing for the 68-pin 10 mm x 10 mm MLF package (**Note:** See Figure 3-6 for dimensions of 72-pin package).

Figure 3-5. 68-Pin Package Drawing



The relevant dimensions for the 72-pin version of the package can be found in Figure 3-6.

Figure 3-6. 72-Pin Package Dimensions



STANDARD

DETAIL "A" - PIN #1 ID AND TIE BAR MARK OPTION

SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		72		3
Nd		18		3
Ne		18		3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4
Q	0.00	0.20	0.45	12
D2	SEE EXPOSED PAD VARIATION:C			
E2	SEE EXPOSED PAD VARIATION:C			

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	-	0.85	0.90	
A1	0.00	0.01	0.05	11
A2	-	0.65	0.70	
A3		0.20 REF.		
D		10.00 BSC		
D1		9.75 BSC		
E		10.00 BSC		
E1		9.75 BSC		
θ			12°	
P	0.24	0.42	0.60	
R	0.13	0.17	0.23	12

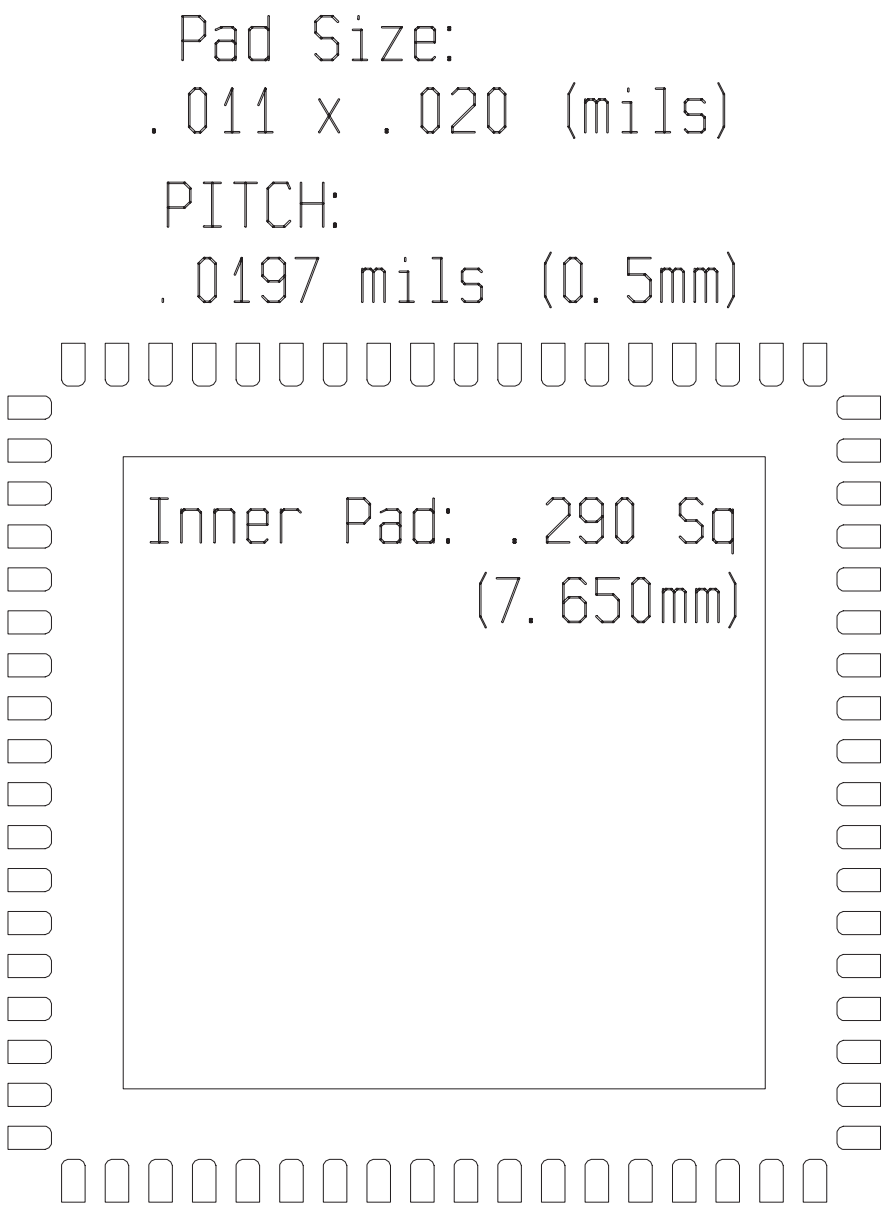
SYMBOLS		D2			E2			NOTE
		MIN	NOM	MAX	MIN	NOM	MAX	
EXPOSED PAD VARIATIONS	C	5.85	6.00	6.15	5.85	6.00	6.15	

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM(.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. - 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. PACKAGE WARPAGE MAX 0.08mm.
10. APPLIED FOR EXPOSED PAD AND TERMINALS.
    EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
11. APPLIED ONLY FOR TERMINALS.
12. Q AND R APPLIES ONLY FOR STRAGHT TIEBAR SHAPES.

The M21050 evaluation module (EVM) uses the PCB footprint shown in Figure 3-7.

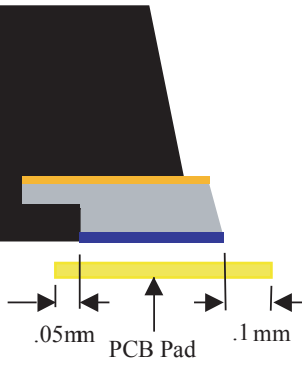
Figure 3-7. PCB Footprint for 72-Pin 10 mm MLF Package



Note: Pads placed on a .374 mils square (9.5 mm).
Add as many vias to ground in .290 square pad as possible.
Add .025 round clearances on soldermask in an even pattern to help solder ground pad.

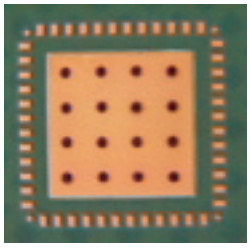
The pad length dimensions should account for component tolerances, PCB tolerances, and placement tolerances. At a minimum, the pad should extend at least 0.1 mm on the outside and 0.05 mm on the inside, as shown in Figure 3-8.

Figure 3-8. PCB Pad Extensions



To efficiently dissipate heat from the M21050, a thermal pad with thermal vias should be used on the PCB. An example of a thermal pad with a 4x4 via array is shown in Figure 3-9. The thermal vias provide a heat conduction path to inner and/or bottom layers of the PCB. The larger the via array, the lower the thermal resistance (θ_{ja}). It is recommended to use thermal vias with 1.0 to 1.2 mm pitch with 0.3 to 0.33 mm via diameter.

Figure 3-9. Recommended Via Array for Thermal Pad



For further details please refer to the relevant application note from package vendor Amkor. Much of the material in this section has been adopted from the Amkor SMT application note.

3.7 PCB High-Speed Design and Layout Guidelines

A single power plane for the ***AVdd_IO*** and ***AVdd_Core*** power supplies with bulk capacitors (typically 10 µF) distributed throughout the board will mitigate most power-rail related voltage transients. A bulk capacitor should also be placed where the power enters the board. It is recommended that decoupling capacitors only be routed directly to the power pin if they can be placed within 1/8 of an inch of the pin. Decoupling capacitors should be dispersed around the outside of the device on the top side and underneath the device on the bottom side of the board. It is recommended that 0.1 µF and 0.01 µF decoupling capacitors be used. All three values are not required on each pin, but values should be dispersed uniformly to filter different frequencies of noise.

A continuous ground plane is the best way to minimize ground impedance. Return currents and power supply transients produce most ground noise during switching. Reducing ground plane impedance minimizes this effect. There is a high frequency decoupling effect from the capacitive effect of power/ground planes and this can be used to help minimize the amount of high frequency decoupling capacitors.

High-speed PCML signals should be routed with 50Ω equal length traces for P and N signals within each differential pair. To route signals differentially, the signal pair (positive and negative) should have 50Ω impedance and surrounded by solid power/ground planes (buried stripline) or be coupled to a power/ground plane (microstrip). Buried strip line is recommended for internal layers while microstrip line is used for signals routed on surface layers. There should be no discontinuity in the planes during the path of the signal traces.

Impedance discontinuities occur when a signal passes through vias and travels between layers. It is recommended to minimize the number of vias and layers that the transmit/receive signals travel through in the design. The system PCB layout should be designed so that high-speed signals pass through a minimal number of vias and remain on a single internal high-speed routing layer.

When vias need to be used, the via design should match the transmission line impedance by observing the following:

- Avoid through-hole vias; they cause stubs by extending the full cross-section of the PCB despite the fact that the layer change requires only a small length via (as in the case of adjacent layers). Use short blind vias.
- Avoid layer changes in general as the characteristic impedance of the transmission line changes as a result.

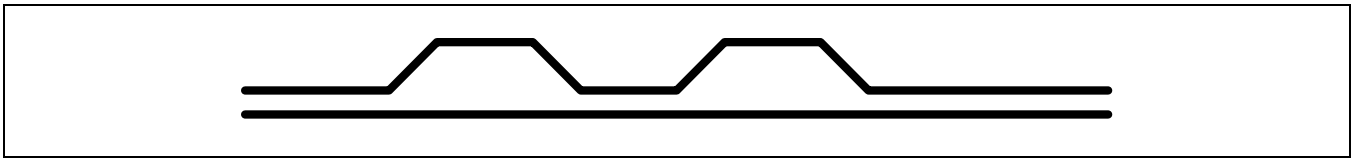
In general, some rules of thumb for PCB design at high data-rates are:

- PCB trace width for high-speed signals should closely match the SMT component width, so as to prevent stub effects from a sudden change in stripline width. A gradual increase in trace width is recommended as it meets the SMT pad.
- The PCB ground/power planes should be removed under the I/O components so as to reduce parasitic capacitance.
- High-speed traces should avoid sharp changes in direction. Using large radii will minimize impedance changes. Avoid bending traces by more than 45 degrees; otherwise, provide a circular bend so as to prevent the trace width from widening at the bend.
- Avoid trace stubs by minimizing components (resistors, capacitors) on the board. For instance, a termination resistor at the input of a receiver will inflict a stub effect at high frequency. Termination resistors integrated on device will eliminate the stub. Components designed to DC couple to one another avoid the need for coupling capacitors and the inherent stubs created from these.

For high-speed differential signals, the trace lengths of each side of the differential pair should be matched to each other as much as possible. The skew between the P and N signals in a differential pair should be tightly controlled in order for the differential receiver to detect a valid data transition. When matching trace lengths within a differential pair, care should be taken to avoid introducing large impedance discontinuities. The figures below show two methods of matching the trace lengths for a differential pair.

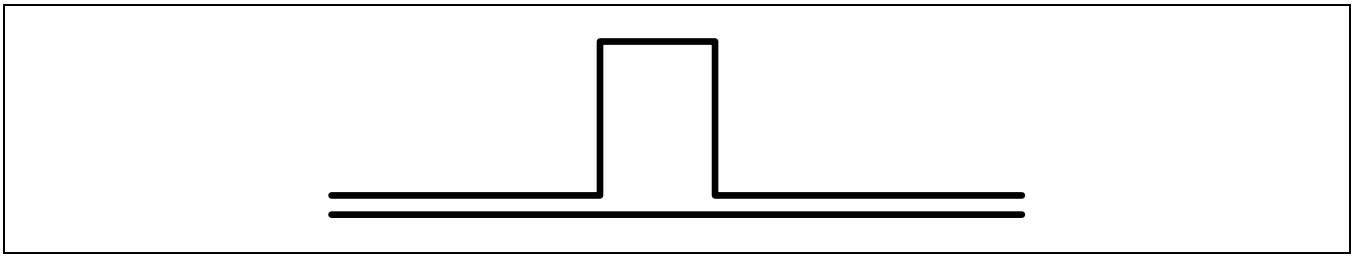
Typically, the preferred solution for trace length matching in differential pairs is to use a serpentine pattern for the shorter signal as shown in Figure 3-10. Using a serpentine pattern for length matching will minimize the differential impedance discontinuity while making both trace lengths equal.

Figure 3-10. Trace Length Matching Using Serpentine Pattern



The loop length matching method shown in Figure 3-11 will match the trace lengths of a differential pair, but will create a large impedance discontinuity in the transmission line, which could result in higher jitter on the signal and/or a greater sensitivity to noise for the differential pair.

Figure 3-11. Loop Length Matching for Differential Traces



When using capacitors to AC couple the input, care should be taken to minimize the pattern-dependant jitter (PD_J) associated with the low-frequency cutoff of the coupling network. When NRZ data containing long strings of 1s or 0s is applied to a high-pass filter, a voltage droop occurs. This voltage droop causes PD_J in much the same fashion as inter-symbol interference (ISI) is generated from dispersion effects of long lengths of backplane material.

If needed, use 0.1 μF capacitors to AC-couple the high-speed output signals, and the reference clock inputs. The high-speed data input signals must be AC-coupled.

On the Evaluation Module (EVM), we have tied ***DVdd_I/O*** and ***AVdd_I/O*** together to minimize the number of power supply jacks. They are kept separate on-device to give the flexibility to the system designers to supply a different voltage level for each. For instance, an FPGA can supply ***DVdd_I/O***, while a lower ***AVdd_I/O*** can be used to minimize power dissipation. On the EVM, we have also tied ***DVdd_Core*** and ***AVdd_Core*** together to minimize the number of power supply jacks. They are kept separate on-device to provide more isolation, however, if the system board plane is properly decoupled, they can be tied together.

No inductive filtering on the system board is necessary between different power supplies of the device. It is up to the system designer to determine if this needs to be considered for supplies that are coming from other parts of the system board (such as switching regulators or ASICs).

An inductor should not be used at the ***VddT*** pins. These pins were made available to create a low AC impedance, such that the 50Ω on-device termination impedances see a common AC ground. This assures both common-mode and differential termination. Note that a low AC impedance can also be created by tying the ***VddT*** pins to the ***AVdd_Core*** plane, thus saving on the number of external capacitors. ***VddT*** is not really a supply plane on-device, it is simply the point to which the 50Ω input impedances are tied.

Power planes should be decoupled to ground planes using thin dielectric layers, to increase capacitance (preferably 2-4 mils). Reference ground layers should be used on both sides of inner layer routing planes, with controlled impedance. The total board thickness should meet the standard drill holes to board thickness ratio of 1:12 or 1:14.

Use 1/2 ounce copper clad on all layers, which is approximately 0.7 mils. Avoid placing solder mask and silk-screen on top of transmission lines, solder mask will add 1 - 2Ω to the overall impedance of the transmission line. Dielectric core material should be used wherever possible, as it will maintain its thickness and geometry during processing, better than pliable prepreg.

The microwave ground should follow the transmission line from end to end, or from signal input to output. It is best to designate layers as dedicated microwave/circuit ground planes, and properly isolate them from other ground planes by providing adequate distance. All microwave ground planes should be tied together.

Uncoupled microstrip transmission lines should be placed at a distance from each other of at least three times the transmission line width. Coupled microstrip transmission lines, such as differential signal pairs, must be placed close to each other and maintain the same separation distance throughout the board (separation distance of at most twice the trace width). For buried stripline transmission lines, it is good design practice to maintain equal distance between the conductor and the ground plane on both sides.

During PCB manufacturing, over- and under-etching of traces used for transmission lines results in impedance discontinuities. Use of wide traces for transmission lines will reduce the impact of etching issues. Wide traces also help compensate for skin-effect losses in transmission lines. It should be noted, however, that the wider the traces in a differential pair, the thicker the underlying dielectric layer needs to be.

Surface mount connectors are preferred over through-mount connectors. Connectors should be selected that have controlled characteristic impedances that match the characteristic impedances of the transmission lines.

4.0 Appendices

4.1 Glossary of Terms/Acronyms

Table 4-1 contains a list of acronyms used in this data sheet.

Table 4-1. Acronyms

AIE	Adaptive Input Equalization
BER	Bit-Error Rate
BIST	Built-In Self Test
CDR	Clock and Data Recovery array
DRD	Data-Rate Divider
EVM	Evaluation Module
FLL	Frequency Lock Loop
FRA	Frequency Reference Acquisition
ISI	Inter-Symbol Interference
LOA	Loss of Activity
LOL	Loss of Lock
LOLCir	Loss of Lock Circuitry
MLF	MicroLeadFrame
NRW	Narrow Reference Window
PCB	Printed Circuit Board
PLL	Phase Lock Loop
RFD	Reference Frequency Divider
SONET	Synchronous Optical Network
VCD	VCO Comparison Divider
WRW	Wide Reference Window
XPTS	Crosspoint Switch

4.2 Reference Documents

4.2.1 External

The following external documents were referenced in this data sheet.

- The I^2C Bus Specification version 2.1
- InfiniBand Architecture Specification Volume 2 Release 1.1
- Fibre Channel - Methodologies for Jitter and Signal Quality Specification - MJSQ and FC-PI-2
- Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages
- Amkor Technology Thermal Test Report TT-00-06

4.2.2 Mindspeed

The following Mindspeed documents were referenced in this data sheet.

- M21050 Evaluation Module User Guide
- Jitter tolerance and generation of Mindspeed Technologies crosspoint switches and clock and data recovery arrays

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