M08048

SD, HD, and 3G Cable Driver

The M08048 is a high-speed, low-power, low-jitter cable driver. It is designed to drive serial digital video data through a 75 Ω coaxial cable typically used in video applications. The M08048 cable driver is optimized for performance from 143 Mbps up to 2970 Mbps. The M08048 has selectable slew rates for SD-SDI and HD-SDI applications.

The typical output rise/fall time of the M08048 is 100 ps for HD and 3G rates. The device has a typical set slew rate of 600 ps at SD rates. The M08048 supports a maximum single ended output swing of 1600 mV_{PP} when configured appropriately.

The device is packaged in a new high performance 3x3 mm QFN package to simplify the PCB and reduce package parasitics with resulting improvements in Output Return Loss (ORL). The device is available in an RoHS compliant package that is backward compatible with standard JEDEC SnPb processes.

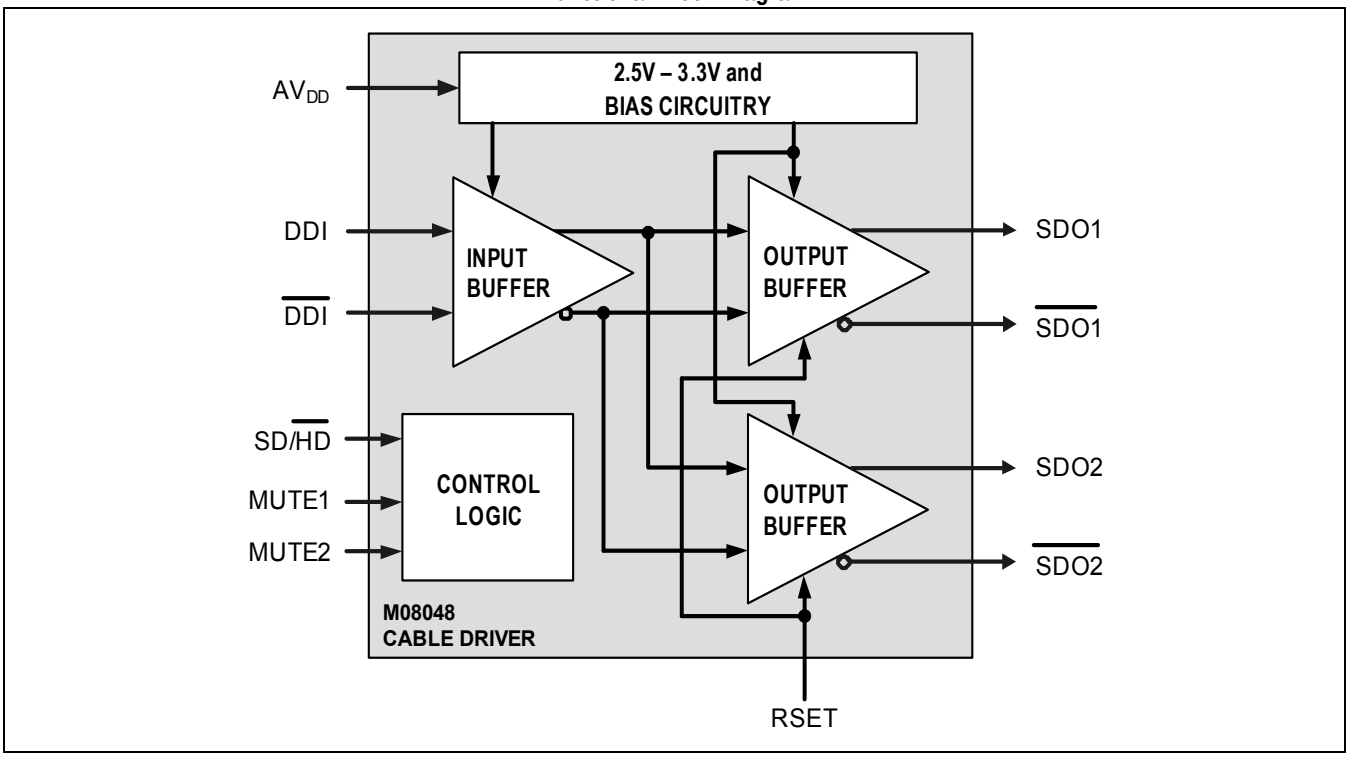
Applications

- Surveillance/CCTV Cameras
- Industrial and Professional Cameras
- Digital Video Recorders (DVR)
- Video Mixers and Switchers
- Digital Image Transmitter Devices
- Distribution Amplifiers
- Repeaters

Features

- 3G, HD and SD operation
- Dual Differential outputs, with individual mute control
- 800 mV_{PP} single ended output swing (typical)
- 1600 mV_{PP} maximum single ended output swing
- SD/HD slew rate control
- 2.5 V or 3.3 V supply
- Low P_{TOTAL} (122 mW @ 2.5 V, 144 mW @ 3.3 V)
- RoHS compliant
- Small form factor (3x3 mm, 16-pin QFN package)

Functional Block Diagram



Ordering Information

Part Number	Data Rates Supported	Package	Operating Temperature
M08048G-11*	143–2970 Mbps	3x3 mm QFN—16pins (RoHS compliant)	-10 °C to 85 °C

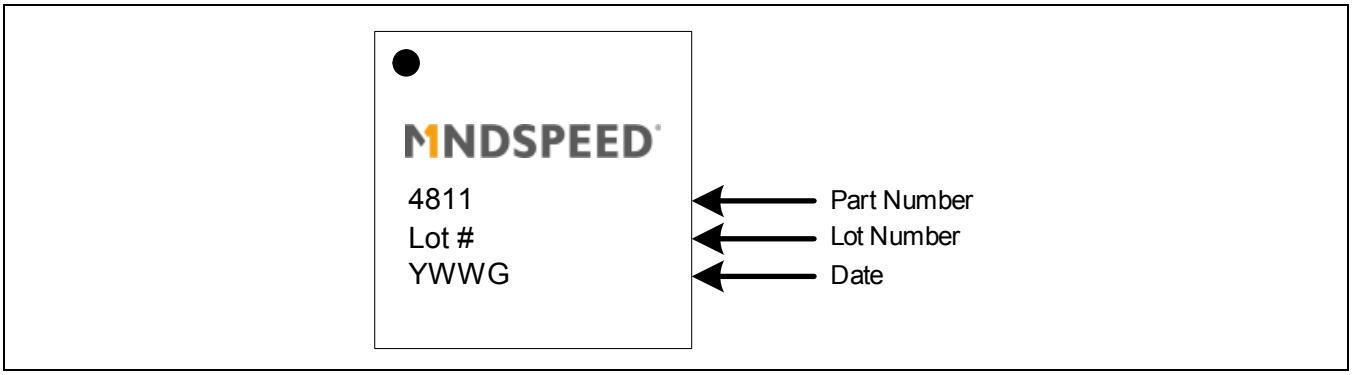
NOTES:

* The letter 'G' designator after the part number indicates a RoHS-compliant package. Refer to www.mindspeed.com for additional information.

Revision History

Revision	Level	Date	Description
B	Release	February 2012	Removed ASE packaging diagram.
A	Release	May 2011	Initial Release.

Marking Diagram



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1.0 Electrical Characteristics

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Units
V_{DD}	Power	AV_{SS} - 0.5	AV_{SS} + 3.47	V
$V_{MAX, IO}$	Maximum/minimum input/output voltage on any input/output pin	AV_{SS} - 0.5	AV_{DD} + 0.5	V
T_{STORE}	Storage Temperature	-65	+150	°C
$V_{ESD, HBM}$	Human Body Model	2000	—	V
$V_{ESD, CDM}$	Charge Device Model	500	—	V

NOTE:

1. No Damage.

Table 1-2. Recommended Operating Conditions

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
AV_{DD}	AV_{DD} Power	—	2.37	2.5/3.3	3.46	V
AV_{SS}	AV_{SS} Ground	—	—	0	—	V
T_A	Ambient Temperature	—	-10	—	+85	°C
θ_{JA}	Junction to ambient Thermal Resistance	1, 2	—	75	—	°C/W
AV_{TERM}	75 Ω Output Termination Voltage	See Table 3-1.				

NOTES:

1. Solder exposed underbody paddle with an array of thermal vias to optimize junction to ambient thermal resistance. Refer to Amkor Application Note (see Section A.2.1).
2. Mounted on a multi layer board (≥ 4 layers), airflow = 0.0 m/s.

Table 1-3. Power DC Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
I_{DD}	Supply Current (one output enabled)	1, 2	—	27	36	mA
I_{DD}	Supply Current (two outputs enabled)	1, 2	—	48	—	mA
I_{TERM}	Current in external termination resistors	1, 2, 3	—	22	—	mA
P_{TOTAL}	Power dissipation (AV_{DD} = 2.5 V, AV_{DDTERM} = 3.3 V)	1, 2, 4, 6	—	122	—	mW
P_{TOTAL}	Power dissipation (AV_{DD} = 2.5 V, AV_{DDTERM} = 3.3 V)	1, 2, 5, 6	—	156	—	mW
P_{TOTAL}	Power dissipation (AV_{DD} = 2.5 V, AV_{DDTERM} = 5.0 V)	1, 2, 4, 6	—	159	—	mW
P_{TOTAL}	Power dissipation (AV_{DD} = 2.5 V, AV_{DDTERM} = 5.0 V)	1, 2, 5, 6	—	194	—	mW
P_{TOTAL}	Power dissipation (AV_{DD} = 3.3 V, AV_{DDTERM} = 3.3 V)	1, 2, 4, 6	—	144	—	mW
P_{TOTAL}	Power dissipation (AV_{DD} = 3.3 V, AV_{DDTERM} = 3.3 V)	1, 2, 5, 6	—	195	—	mW
P_{TOTAL}	Power dissipation (AV_{DD} = 3.3 V, AV_{DDTERM} = 5.0 V)	1, 2, 4, 6	—	181	—	mW
P_{TOTAL}	Power dissipation (AV_{DD} = 3.3 V, AV_{DDTERM} = 5.0 V)	1, 2, 5, 6	—	232	—	mW

NOTES:

1. Recommended operating conditions — see Table 1-2.
2. 800 mV_{PP} standard swing, terminated as in Figure 3-3.
3. A portion of the power will be dissipated in the external 75OOhm termination ($P_{EXT} = V_{OD} \times I_{TERM}$).
4. One Output Enabled.
5. Two Outputs Enabled.
6. Does not include off-chip power dissipated by termination resistors.

Table 1-4. CMOS Input Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
V_{IH}	Input Logic High Voltage	1	0.75 x AV_{DD}	—	AV_{DD} + 0.3	V
V_{IL}	Input Logic Low Voltage	1	0	—	0.25 x AV_{DD}	V
I_{IH}	Input Current (logic High)	1	-100	—	100	µA
I_{IL}	Input Current (logic Low)	1	-100	—	100	µA

NOTE:

1. Specified at recommended operating conditions — see Table 1-2.

Table 1-5. High-Speed Input Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DR	Input Bit Rate (M08048)	1, 2	0	—	2970	Mbps
V_{IN}	Input Differential Voltage	1, 3, 4	100	—	2000	mV_{PPD}
V_{ICM}	Input Common-Mode Voltage	1	1200	—	AV_{DD}	mV
V_{IH}	Maximum Input High Voltage	1	—	—	AV_{DD} + 400	mV
V_{IL}	Minimum Input Low Voltage	1	1.2	—	—	V
R_{IN}	Single-ended input impedance	1	—	13.33	20	kΩ

NOTES:

1. Specified at recommended operation conditions — see Table 1-2.
2. Part is DC coupled at the input.
3. Example 1200 mV_{PPD} = 600 mV_{PP} for each single-ended terminal.
4. Minimum input level defined as BER ≤ 10^{-12}.

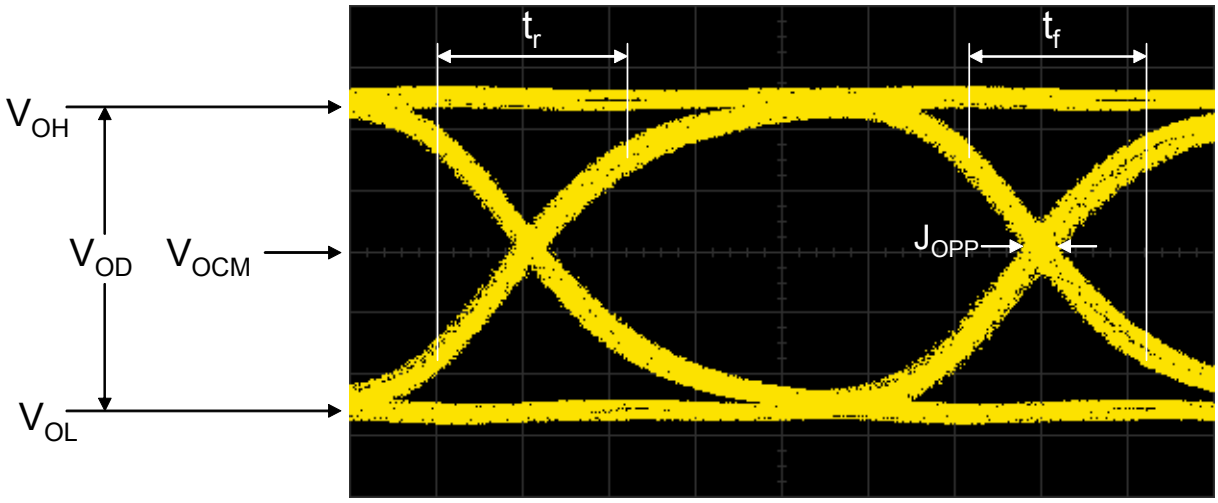
Table 1-6. Cable Driver Output Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DR	Output Bit Rates	1, 5	—	—	2970	Mbps
t_R/t_F	SD Rise/Fall Time (20–80%)	1, 3, 5	400	600	800	ps
	HD/3G Rise/Fall Time (20–80%)	1, 3, 5	—	100	135	ps
t_R/t_F Δ	Rise/fall mismatch (HD/3G Rate)	1, 2, 5	—	10	30	ps
	Rise/fall mismatch (SD Rate)	1, 2, 5	—	40	100	ps
$V_{OUT, SE}$	Single-ended voltage swing	1, 2, 4, 5	500	800	1600	mV_{PP}
$V_{PP, TOL}$	Swing Level output variation at 800 mV_{PP} [**RSET** = 750 Ω ±1%] (Single-Ended)	1, 2, 3, 5	-7	—	+7	%
$V_{OVER/UNDER}$	Overshoot/Undershoot	1, 2, 5	-10	—	+10	%
t_{JIT}	Additive Output Jitter (HD/3G rate)	1, 5, 8	—	20	30	ps
	Additive Output Jitter (SD rate)	1, 5, 8	—	40	60	ps
DCD_O	Duty Cycle Distortion (HD/3G Rate)	1, 2, 5, 6, 8	—	15	30	ps
	Duty Cycle Distortion (SD Rate)	1, 2, 5, 6, 8	—	20	70	ps
S_{22}	Output Return Loss (5 MHz to 1.5 GHz)	1, 2, 5, 7	15	—	—	dB
S_{22}	Output Return Loss (1.5 GHz to 3.0 GHz)	1, 2, 5, 7	10	—	—	dB

NOTES:

1. Entire table specified at recommended operating condition with 400 mV_{PPD} input — see Table 1-2.
2. Specification verified at 800 mV_{PP} output with 1 m cable on MSPD test board. System results may vary.
3. Rated at 800 mV_{PP} output swing (using a 750 Ω ± 1% resistor at RSET).
4. Output stage is an open collector differential pair, actual swing dependant on IC supply voltage and external termination voltage.
5. Into 75 Ω back termination and 75 Ω load and appropriate external termination voltage, see Table 3-1, Figure 3-3.
6. Duty Cycle Distortion (DCD) is defined as the difference in the intrinsic jitter at the 50% voltage level and the intrinsic jitter at the rising/falling edge crossing point. If the rising/falling edge crossing point is at the 50% voltage level, then DCD = 0.
7. Measured under DC conditions that simulate AC coupling, V_T = 3.3 V.
8. Measured using a “1010” data pattern.

Figure 1-1. Output Symbols Definition



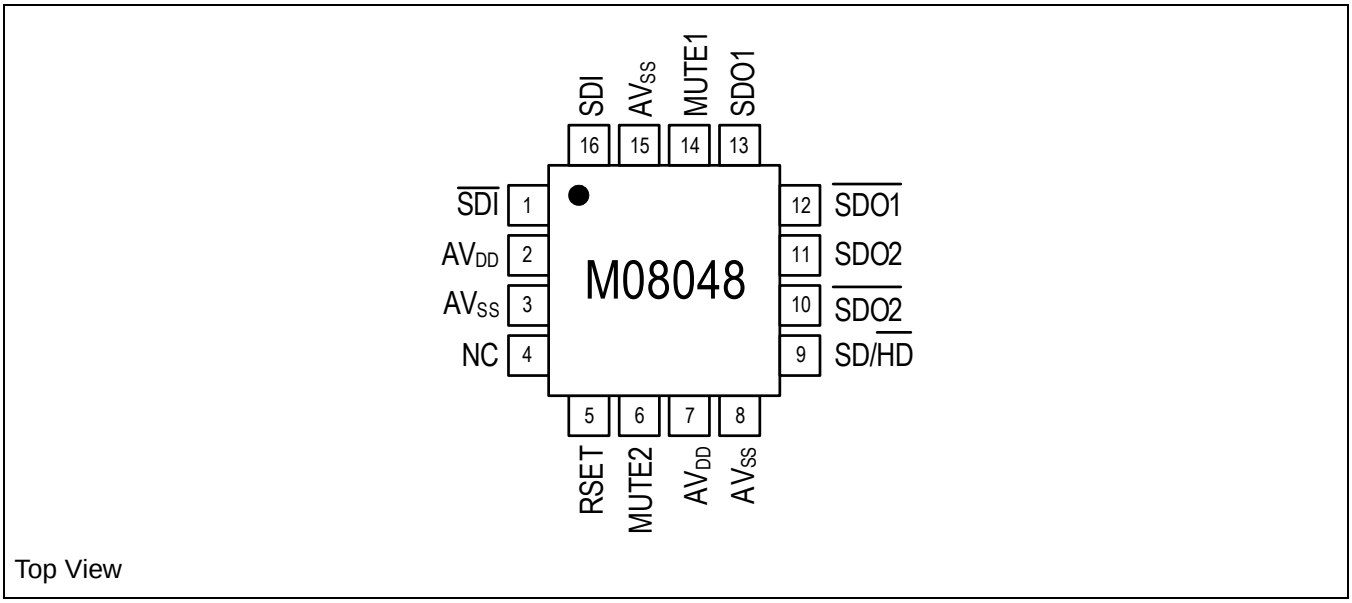
V_{OH}: Average voltage high level
V_{OL}: Average voltage low level
V_{OD}: (VOH) – (VOL)
V_{OCM}: Common Mode Voltage
J_{OPP}: Output Jitter Peak-Peak
t_r: 20-80% Rise Time
t_f: 80-20% Fall Time

NOTE: Waveform above is differential.

2.0 Pinout Diagram, Pin Descriptions, and Package Outline Drawing

The M08048 is available in a 16-pin, 3x3 mm QFN IC package. The pinout is shown in Figure 2-1.

Figure 2-1. M08048 Pin Out



Top View

2.1 Pin Descriptions

Table 2-1. Interface Pins

Pin Name	Pin #	Function	Default	Type
RSET	5	Input control signal for setting the single-ended output swing amplitude. Higher output swing levels or reduced variations with a ±1% tolerance external resistor. For 800 mV_{PP} single-ended, a 750 Ω ±1% resistor to AV_{DD} is recommended.	—	Analog Input

Table 2-2. Power Pins

Pin Name	Pin #	Function	Type
AV_{SS}	3, 8, 15	Ground	Power
AV_{DD}	2, 7	Positive Supply	Power
NC	4	Do not connect.	N/A

Table 2-3. High-speed Signal Pins

Pin Name	Pin #	Function	Default	Type
DDI/$\overline{\text{DDI}}$	16, 1	Non-inverting and Inverting serial externally terminated inputs.	—	CML input
SDO2/$\overline{\text{SDO2}}$	11, 10	Non-inverting and inverting serial unterminated data outputs to coaxial cable.	—	CML output
SDO1/$\overline{\text{SDO1}}$	13, 12	Non-inverting and inverting serial unterminated data outputs to coaxial cable.	—	CML output

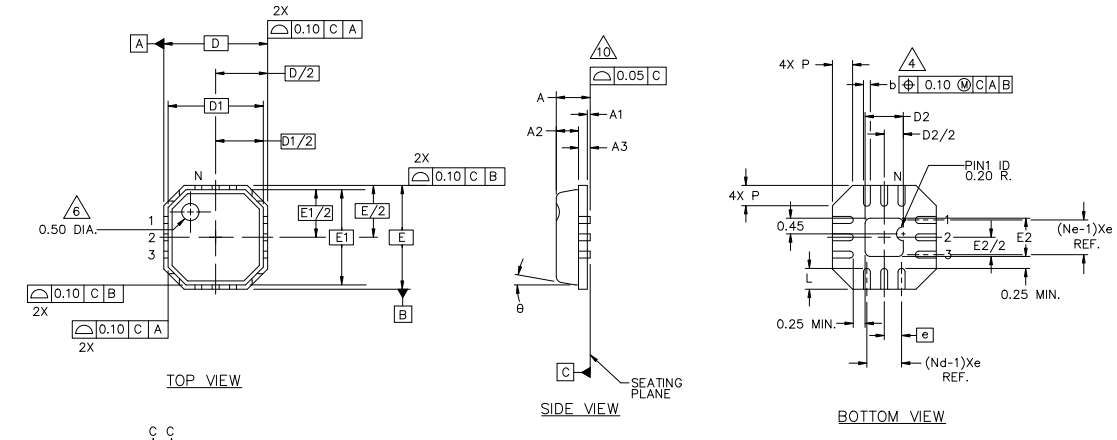
Table 2-4. Control Pins

Pin Name	Pin #	Function	Default	Type
MUTE2	6	A high mutes **SDO2/$\overline{\text{SDO2}}$** outputs, low enables SDO2/$\overline{\text{SDO2}}$.	Pull-up	CMOS input
MUTE1	14	A high mutes **SDO1/$\overline{\text{SDO1}}$** outputs, low enables SDO1, $\overline{\text{SDO1}}$.	Pull-down	CMOS input
SD/$\overline{\text{HD}}$	9	Input control signal to change the output slew rate. SD/$\overline{\text{HD}}$ = High: Slow output slew rate for SD-SDI rate (143–540 Mbps). SD/$\overline{\text{HD}}$ = Low: Fast output slew rate for HD and 3G-SDI rate.	Pull-up	CMOS input
NOTES: Internal pull-ups/pull-downs are 100 kΩ.				

2.2 Package Drawing

The package for the M08048 is illustrated in Figure 2-2 below.

Figure 2-2. M08048 Packaging Details—Amkor



Note: View is for a 12 pin package. All dimensions in the tables apply for the 16 pin package

SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		16		3
Nd		4		3
Ne		4		3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4
D2	1.35	1.50	1.65	
E2	1.35	1.50	1.65	

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	-	0.85	0.90	
A1	0.00	0.01	0.05	11
A2	-	0.65	0.70	
A3		0.20 REF.		
D		3.00 BSC		
D1		2.75 BSC		
E		3.00 BSC		
E1		2.75 BSC		
θ			12°	
P	0.24	0.42	0.60	

NOTES:

2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. - 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. PACKAGE WARPAGE MAX 0.05mm.
10. APPLIED FOR EXPOSED PAD AND TERMINALS.
    EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
11. APPLIED ONLY FOR TERMINALS.

Please see Amkor's Application Note for PCB footprint (referenced in Section 3.2.1).

2.3 Manufactureability

The values shown in this section may change; however, these are standard requirements.

2.3.1 Electrostatic Discharge

Tested per JESD22-A114. This device passes 2000 V of ESD Human Body Model (HBM) testing.

Tested per JESD22-C101. This device passes 500 V of ESD Charged Device Model (CDM) testing.

Tested per EIA/JESD78. This device passes 150 mA of trigger current at 85 °C during Latchup testing.

2.3.2 Peak Reflow Temperature

M08048G (RoHS compliant package): Peak reflow temperature is 260 °C per JEDEC standards.

3.0 Functional Description

3.1 Features

3.1.1 HD-SDI and SD-SDI Slew-rate Selection

The output slew rate of the M08048 is selectable to conform with the different SD-SDI and HD-SDI specifications. The slew rate will vary depending on the output matching network and connector used.

With **SD/$\overline{\textbf{HD}}$** = High, the rise/fall time is typically 600 ps. With SD/HD = Low, rise/fall time is typically 100 ps.

3.1.2 Output Amplitude Adjustment

An external 750 Ω ±1% resistor at **RSET** to $\mathbf{AV_{DD}}$ is recommended for a swing level of 800 mV_{PP} within a tolerance that is less than ±10%. The output amplitude can also be adjusted to range from 500 to 1600 mV_{PP} single ended using the following formula:

Output Swing = (600/**RSET**) [**RSET** in kΩ] (in mV_{PP}, Single Ended)

The actual swing is set as a function of the IC supply voltage, the external termination voltage and the limitations are shown in Table 3-1. In applications where lossy matching or splitting networks are used, the M08048 offers additional gain of up to 1600 mV_{PP} swings. When using swings in excess of 1200 mV_{PP}, there will be an increase in rise and fall times.

Table 3-1. Output Swing vs. Supply and Termination Voltage

AV_{DD} (V)	AV_{DDTERM} (V)	Maximum Swing (Single-ended mV_{PP})	Minimum Swing (Single-ended mV_{PP})
2.5–3.3	3.3	1200	500
2.5–3.3	5.0	1600	500

3.2 Pin Definitions

3.2.1 High-speed Inputs

The M08048 is designed to be operated with input signals as low as 100 mV_{PPD} or up to 2000 mV_{PPD}. The M08048 uses external 50 Ω input termination resistors to match 100 Ω differential impedance transmission lines for improved system level performance. The M08048 recommended input circuits are shown in Figure 3-1.

Note that AC coupling is not required when the M08048 is driven by Mindspeed digital video devices.

Figure 3-1. Typical Input Circuit—AC Coupled

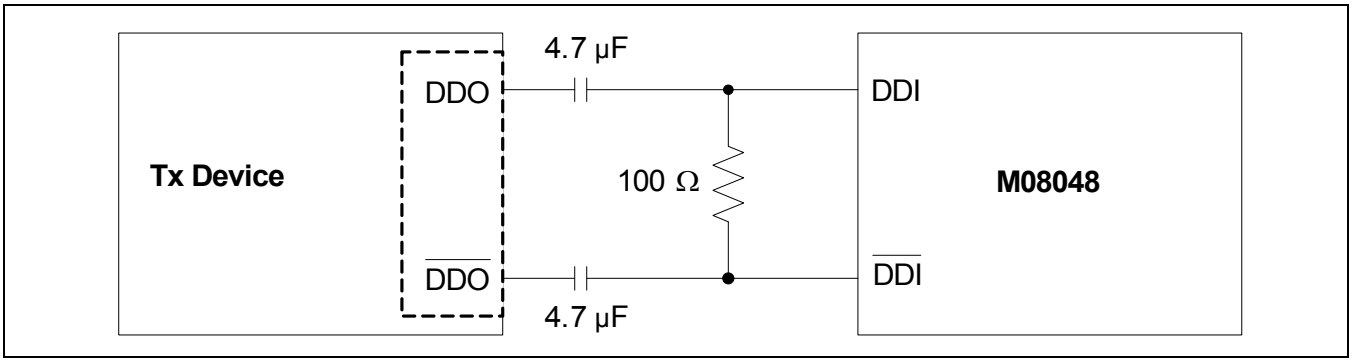
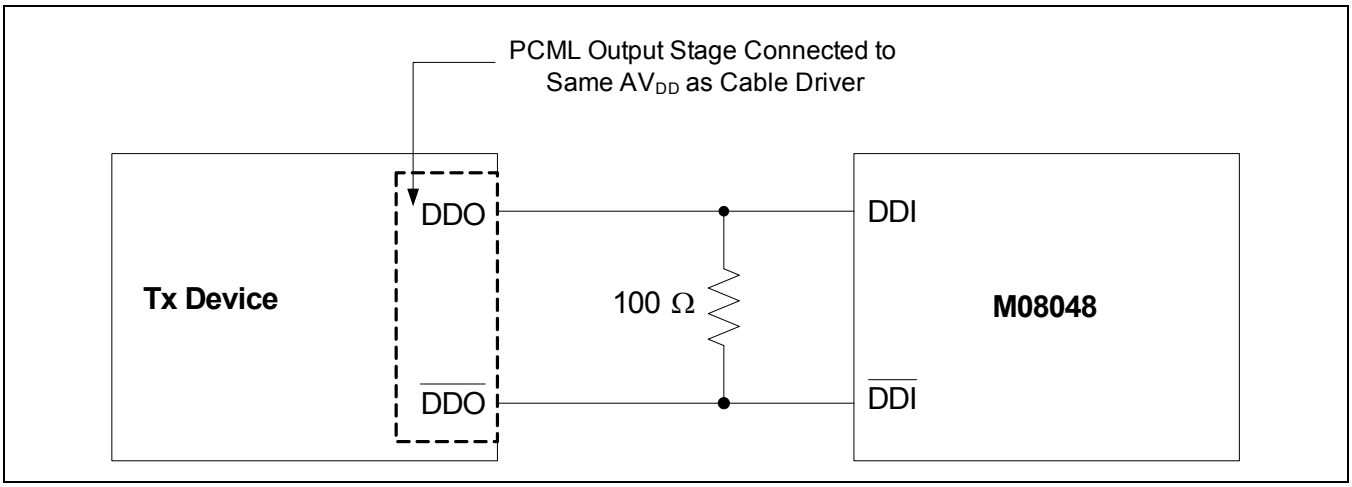


Figure 3-2. Typical Input Circuit—DC Coupled



3.2.2 High-speed Outputs

The M08048 output buffer is an open collector buffer that is designed for a return loss of 15 dB at SD and HD rates and 10 dB at 3G rates, using standard through-hole BNC connectors. A typical output matching circuit is shown in Figure 3-3. The Output Return Loss (ORL) is dependent on many factors such as the value and type of components used, PCB layout, PCB trace lengths, and type of PCB di-electric, therefore, the recommendations in the figure below should be used as starting guidelines only. Different output matching network topologies and different component values will result in different ORL performance.

The actual maximum output of the part depends on the applied IC voltage as well as the external termination voltage for the load termination. The limitations are discussed in Section 3.1.

Figure 3-3. Output Matching/Back-termination Circuit (Both Outputs Used)

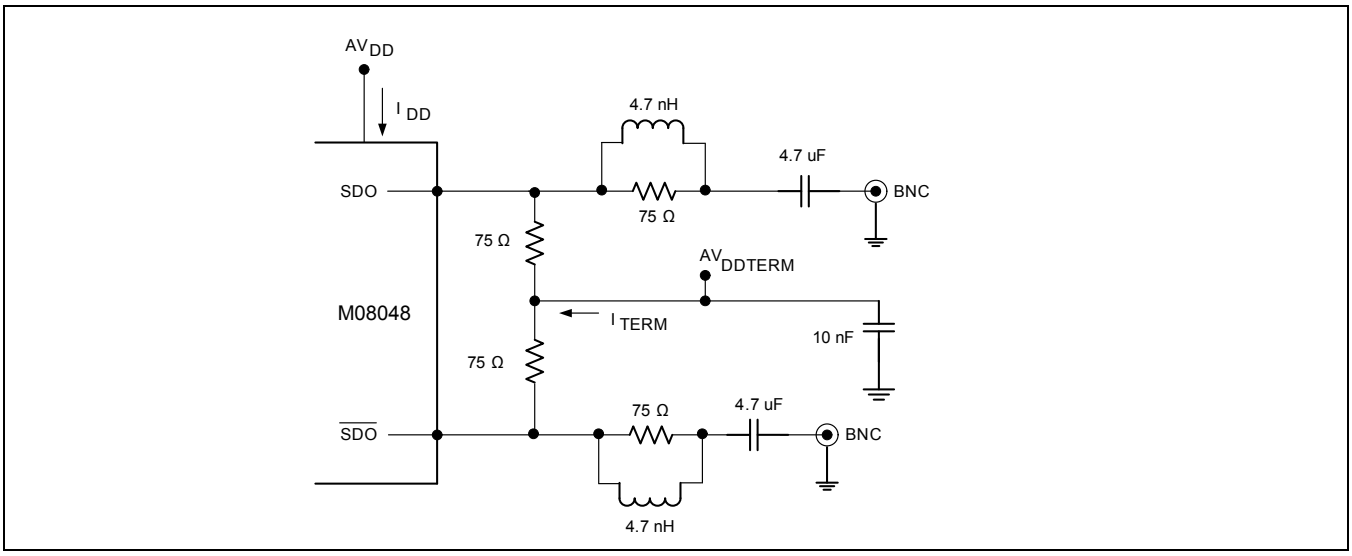
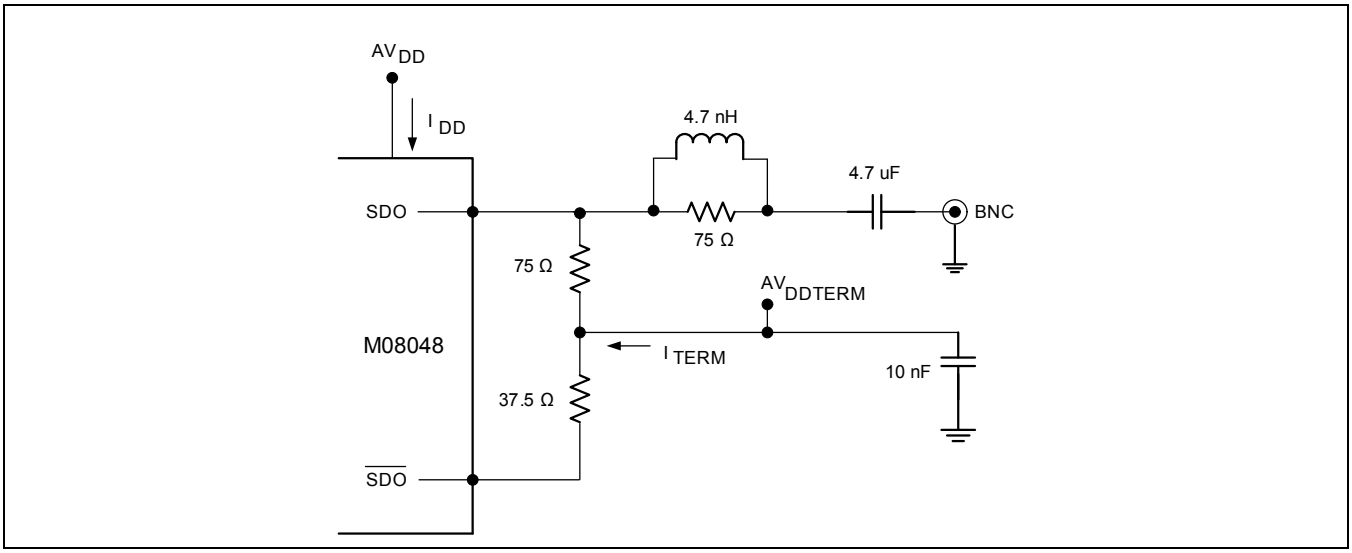


Figure 3-4. Output Matching/Back-termination Circuit (Only One Output Used)



Appendix

A.1 Glossary of Terms/Acronyms

BER	Bit Error Rate
CD	Cable Driver
CDA	Cable Distribution Amplifier
CML	Current Mode Logic
CMOS	Complementary Metal Oxide Semiconductor
DPLL	Digital Phase Locked Loop
EMI	Electro Magnetic Interference
EQ	Equalizer or Equalization
GREEN	Environmentally friendly
HD	High Definition
HW	Hardware
IC	Integrated Circuit
ID	Identifier
I/O	Input/Output
PCB	Printed Circuit Board
QFN	Quad Flat No Lead
ORL	Output Return Loss
RoHS	Restriction of Hazardous Substances
SD	Standard Definition
SDI	Serial Digital Input
SDO	Serial Digital Output
SE	Single Ended

A.2 Reference Documents

A.2.1 External

The following external documents were referenced in this data sheet.

- Application Notes for Surface Mount Assembly of Amkor's Packages
- Amkor Technology Thermal Test Report TT-00-06 (See http://www.amkor.com for detailed information)

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