M02014

CMOS Transimpedance Amplifier with AGC for Fiber Optic Networks up to 2.5 Gbps

The M02014 is a CMOS transimpedance amplifier with AGC. The AGC gives a wide dynamic range of 32 dB. The high transimpedance gain of 11 kΩ ensures good sensitivity.

For optimum system performance, the M02014 die should be mounted with a photodetector inside a lensed TO-Can or other optical sub-assembly.

The M02014 can either bias the PIN diode from the internal regulator or use an externally biased photodiode. A replica of the average photodiode current is available at the MON pad for photo-alignment.

Applications
- GPON
- PCI Express
- ATM/SONET
- Infiniband

Features
- Typical –26.6 dBm sensitivity, +6 dBm saturation at 2.5 Gbps when used with 0.9 A/W InGaAs PIN. (Cpd ≤ 0.5 pF, BER 10⁻¹⁰)
- Typical Differential Transimpedance: 11.1 kΩ
- Fabricated in standard CMOS
- Differential output
- Standard +3.3 Volt supply
- Available in die form only
- AGC provides dynamic range of 32 dB
- Can use internal or external bias for photodiode
- Usable with a PIN or APD photodiode
- Same pad layout and die size as M02011/13/15/16

Typical Applications Diagram
Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package</th>
<th>Operating Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>M02014-XX*</td>
<td>Waffle Pack</td>
<td>−40 °C to 95 °C</td>
</tr>
<tr>
<td>M02014-XX*</td>
<td>Expanded whole wafer on a ring</td>
<td>−40 °C to 95 °C</td>
</tr>
</tbody>
</table>

*For full ordering number please contact sales

Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>Level</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>Released</td>
<td>August 2007</td>
<td>Corrected PinA, AGC, and DOUT absolute maximum voltage in Table 1-1.</td>
</tr>
<tr>
<td>C</td>
<td>Released</td>
<td>May 2007</td>
<td>Production Release. Raised max operating temperature. Remove $V_{OL}$ and $V_{OH}$ from the DC specifications and updated $I_{CC}$ and $V_B$.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Update the following AC specifications: $R_{OUT}$ and $V_D$, and removed $I_{mon_off}$ and $I_{mon_lin}$. Update the gain and bandwidth in the Dynamic Specifications.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Added typical performance characteristics in the Specifications section. In the Functional Description section, the description for the monitor output now states it is intended for photo-alignment use only.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Added recommended assembly instructions.</td>
</tr>
<tr>
<td>B</td>
<td>Preliminary</td>
<td>August 2005</td>
<td>Revision B, Preliminary.</td>
</tr>
<tr>
<td>A</td>
<td>Advance</td>
<td>May 2005</td>
<td>Initial Release.</td>
</tr>
</tbody>
</table>

Typical Eye Diagram

Unfiltered Eye Diagram for 2.5 Gbps @ -26 dBm

Pad Configuration

Die size ≈ 1090 x 880 µm
1.0 Product Specification

1.1 Absolute Maximum Ratings

These are the absolute maximum ratings at or beyond which the IC can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

Table 1-1. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Rating</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>Power supply ($V_{CC} - \text{GND}$)</td>
<td>-0.4 to +4.0</td>
<td>V</td>
</tr>
<tr>
<td>$T_{STG}$</td>
<td>Storage temperature</td>
<td>-65 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>$I_{IN}$</td>
<td>PINA Input current</td>
<td>8.0 (1, 2) mApp</td>
<td></td>
</tr>
<tr>
<td>$V_{PINA}, V_{AGC}$</td>
<td>Maximum input voltage at PINA and AGC</td>
<td>-0.4 to +2.0 (2)</td>
<td>V</td>
</tr>
<tr>
<td>$I_{PINK}$</td>
<td>Maximum average current sourced out of PINK</td>
<td>10.0</td>
<td>mA</td>
</tr>
<tr>
<td>$V_{PINK}, V_{MON}$</td>
<td>Maximum input voltage at PINK and MON</td>
<td>-0.4 to Vcc +0.4</td>
<td>V</td>
</tr>
<tr>
<td>$I_{Dout}$</td>
<td>Maximum average current sourced out of Dout and DoutB</td>
<td>10.0 (3) mA</td>
<td></td>
</tr>
<tr>
<td>$V_{Dout}$</td>
<td>Maximum input voltage at Dout and DoutB</td>
<td>0.0 to +2.0 (3)</td>
<td>V</td>
</tr>
</tbody>
</table>

NOTES:
1. Equivalent to 4.9 mA average current.
2. Do not exceed either the $I_{IN}$ or $V_{PINA}$ rating. PINA damage will result in performance degradation which is difficult to detect.
3. Do not exceed either the $I_{Dout}$ or $V_{Dout}$ rating. Output device damage could occur.

1.2 Recommended Operating Conditions

Table 1-2. Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Rating</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>Power supply ($V_{CC} - \text{GND}$)</td>
<td>3.3 ± 10%</td>
<td>V</td>
</tr>
<tr>
<td>$C_{PD}$</td>
<td>Max. Photodiode capacitance ($V_{f} = 1.8\text{V}$, for 2.5 Gbps data rate)</td>
<td>0.5</td>
<td>pF</td>
</tr>
<tr>
<td>$T_{A}$</td>
<td>Operating ambient temperature</td>
<td>-40 to +95</td>
<td>°C</td>
</tr>
</tbody>
</table>
1.3 DC Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_B</td>
<td>Photodiode bias voltage (PINK – PINA)</td>
<td>1.7</td>
<td>2.0</td>
<td>2.2</td>
<td>V</td>
</tr>
<tr>
<td>V_CM</td>
<td>Common mode output voltage</td>
<td>0.7</td>
<td>1.0</td>
<td>1.3</td>
<td>V</td>
</tr>
<tr>
<td>I_CC</td>
<td>Supply current (no loads)</td>
<td>29</td>
<td>38</td>
<td>47</td>
<td>mA</td>
</tr>
<tr>
<td>R_LOAD</td>
<td>Recommended differential output loading</td>
<td>85</td>
<td>100(1)</td>
<td>—</td>
<td>Ω</td>
</tr>
</tbody>
</table>

NOTES:
1. 100Ω is the load presented by the limiting amplifier.

1.4 AC Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Minimum</th>
<th>Typical (1)</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_OUT</td>
<td>Output impedance (single ended)</td>
<td>—</td>
<td>30</td>
<td>50</td>
<td>70</td>
<td>Ω</td>
</tr>
<tr>
<td>L_FC</td>
<td>Low frequency cutoff (2)</td>
<td>—</td>
<td>—</td>
<td>35</td>
<td>50</td>
<td>kHz</td>
</tr>
<tr>
<td>V_D</td>
<td>Differential output voltage</td>
<td>100Ω differential load</td>
<td>—</td>
<td>225</td>
<td>400</td>
<td>mV</td>
</tr>
<tr>
<td>DCD</td>
<td>Duty cycle distortion</td>
<td>2.5 Gbps</td>
<td>—</td>
<td>—</td>
<td>50</td>
<td>ps</td>
</tr>
<tr>
<td>DJ</td>
<td>Deterministic jitter (includes DCD)</td>
<td>2.5 Gbps, 2^23 – 1 PRBS</td>
<td>—</td>
<td>—</td>
<td>60</td>
<td>psPP</td>
</tr>
<tr>
<td>PDJ</td>
<td>Pattern Dependant Jitter (at crossing point), with no DCD</td>
<td>2.5 Gbps, 2^23 – 1 PRBS</td>
<td>—</td>
<td>—</td>
<td>30</td>
<td>psPP</td>
</tr>
<tr>
<td>In, rms</td>
<td>Total input RMS noise</td>
<td>DC to 1.87 GHz (Bessel Filter), Cin = 0.5 pF</td>
<td>—</td>
<td>253</td>
<td>350</td>
<td>nA</td>
</tr>
<tr>
<td>PIN_mean_min</td>
<td>Optical Sensitivity (3)</td>
<td>—</td>
<td>26.6</td>
<td>—</td>
<td>dBm</td>
<td></td>
</tr>
</tbody>
</table>

NOTES:
1. Die designed to operate over an ambient temperature range (T_A) of –40 °C to +95 °C, and V_CC range from 3.0–3.6V. Typical values are tested at T_A = 25 °C and V_CC = 3.3V.
2. Input level below AGC threshold.
3. BER 10^-10, PD capacitance = 0.5 pF, Responsivity 0.9 A/W, Extinction Ratio = 10, Temp = 25 °C.
1.5 Dynamic Characteristics

Table 1-5. Dynamic Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>G</td>
<td>Differential Transimpedance (1)</td>
<td>6.9</td>
<td>11.15</td>
<td>15.5</td>
<td>kΩ</td>
</tr>
<tr>
<td>BW</td>
<td>Bandwidth to –3 dB point @ –26 dBm, 0.9 A/W, 0.5 pF PD</td>
<td>1400</td>
<td>2100</td>
<td>—</td>
<td>MHz</td>
</tr>
<tr>
<td>RC</td>
<td>AGC loop time constant</td>
<td>—</td>
<td>2</td>
<td>—</td>
<td>µs</td>
</tr>
<tr>
<td>I_{AGC}</td>
<td>AGC threshold</td>
<td>—</td>
<td>16</td>
<td>—</td>
<td>µA_P</td>
</tr>
<tr>
<td>I_{OVL}</td>
<td>Input overload current</td>
<td>3.3 (2)</td>
<td>—</td>
<td>—</td>
<td>mA_P</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power supply rejection, f &lt; 1 MHz</td>
<td>20</td>
<td>27</td>
<td>—</td>
<td>dB</td>
</tr>
</tbody>
</table>

NOTES:
2. Equivalent to +3dBm input optical power at Extinction Ratio = 10, Responsivity = 1.0 A/W.

1.6 Typical Performance

V_{CC} = 3.3V, Temperature = 25°C, L_{IN} = 1 nH, unless otherwise stated.

Figure 1-1. Typical Performance Diagrams 1 of 3
V_{CC} = 3.3V, Temperature = 25°C, L_{IN} = 1 nH, unless otherwise stated.

**Figure 1-2. Typical Performance Diagrams 2 of 3**

**Typical Differential Transimpedance vs. Average Input Power**
(Extinction Ratio = 13dB)

![Graph showing typical differential transimpedance vs. average input power]

**M02014 Jitter Characteristics vs. I_{IN}**
3.3V Typical, L_{IN} = 1 nH, C_{IN} = 0.5 pF, 2.5 Gbps
(note: DJ = PDJ + |DCD|)

![Graph showing jitter characteristics vs. input power]
$V_{CC} = 3.3V$, Temperature $= 25^\circ C$, $L_{IN} = 1$ nH, unless otherwise stated.

**Figure 1-3. Typical Performance Diagrams 3 of 3**

Note: Assumed TO Can thermal resistance of 100°C/W results in a typical die temperature rise of 15°C
2.0 Pin Definitions

Table 2-1. Pad Description

<table>
<thead>
<tr>
<th>Die Pad No</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>AGC</td>
<td>Monitor or force AGC voltage</td>
</tr>
<tr>
<td>2</td>
<td>$V_{CC}$</td>
<td>Power pin. Connect to most positive supply. (only one $V_{CC}$ pad needs to be connected)</td>
</tr>
<tr>
<td>3</td>
<td>PINK</td>
<td>Common PIN input. Connect a 470 pF capacitor to Gnd when using this pad to bias the photodiode cathode (^{(1)})</td>
</tr>
<tr>
<td>4</td>
<td>PINA</td>
<td>Active PIN input. Connect to photo diode anode</td>
</tr>
<tr>
<td>5</td>
<td>$V_{CC}$</td>
<td>Power pin. Connect to most positive supply (only one $V_{CC}$ pad needs to be connected)</td>
</tr>
<tr>
<td>6</td>
<td>MON</td>
<td>Analog current source output. Current matched to average photodiode current. Intended for photo-alignment use only</td>
</tr>
<tr>
<td>7</td>
<td>DOUT</td>
<td>Differential data output (goes low as light increases)</td>
</tr>
<tr>
<td>8</td>
<td>DOUTGND</td>
<td>Ground return for DOUT pad (^{(2)})</td>
</tr>
<tr>
<td>9</td>
<td>GND</td>
<td>Ground pin. Connect to the most negative supply (^{(2)})</td>
</tr>
<tr>
<td>10</td>
<td>GND</td>
<td>Ground pin. Connect to the most negative supply (^{(2)})</td>
</tr>
<tr>
<td>11</td>
<td>DOUTGND</td>
<td>Ground return for DOUT pad (^{(2)})</td>
</tr>
<tr>
<td>12</td>
<td>DOUT</td>
<td>Differential data output (goes high as light increases)</td>
</tr>
<tr>
<td>NA</td>
<td>Backside</td>
<td>Backside. Connect to the lowest potential, usually ground</td>
</tr>
</tbody>
</table>

NOTES:
1. Alternatively the photodiode cathode may be connected to a decoupled positive supply, e.g. $V_{CC}$.
2. All ground pads are common on the die. Only one ground pad needs to be connected to the TO-Can ground. However, connecting more than one ground pad to the TO-Can ground, particularly those across the die from each other can improve performance in noisy environments.

Figure 2-1. Bare Die Layout
3.0 Functional Description

3.1 Overview

The M02014 is a CMOS transimpedance amplifier with AGC. The AGC gives a wide dynamic range of 32 dB. The high transimpedance gain of 11 kΩ ensures good sensitivity.

For optimum system performance, the M02014 die should be mounted with a PIN photodetector inside a lensed TO-Can or other optical sub-assembly.

The M02014 can either bias the PIN diode from the internal regulator or use an externally biased photo diode.

A replica of the average photodiode current is available at the MON pad for photo-alignment.

Figure 3-1. M02014 Block Diagram
3.2 General Description

3.2.1 TIA (Transimpedance Amplifier)

The transimpedance amplifier consists of a high gain single-ended CMOS amplifier (TIA) with a feedback resistor. The feedback creates a virtual ground low impedance at the input and virtually all of the input current passes through the feedback resistor defining the voltage at the output. Advanced CMOS design techniques are employed to maintain the stability of this stage across all input conditions.

An on-chip low dropout linear regulator has been incorporated into the design to give excellent noise rejection up to several MHz. Higher frequency power supply noise is removed by the external 470 pF decoupling capacitor connected to PINK.

The circuit is designed for PIN photodiodes in the “grounded cathode” configuration, with the anode connected to the input of the TIA and the cathode connected to AC ground, such as the provided PINK terminal. Reverse DC bias is applied to reduce the photodiode capacitance. Avalanche photodiodes can be connected externally to a higher voltage.

3.2.2 AGC

The M02014 has been designed to operate over the input range of +6 dBm to –26.5 dBm. This represents a ratio of 1:1500 whereas the acceptable dynamic range of the output is only 1:30 which implies a compression of 50:1 in the transimpedance. The design uses a MOS transistor operating as a “voltage controlled resistor” to achieve the transimpedance variation.

Another feature of the AGC is that it only operates on signals greater than –20 dBm (@ 0.9 A/W). This knee in the gain response is important when setting “signal detect” functions in the following post amplifier. It also aids in active photodiode alignment.

The AGC pad allows the AGC to be forced externally through a low impedance, if desired. The AGC control voltage can be monitored during normal operation at this pad by a high impedance (>10 MΩ) circuit.

3.2.3 Output Stage

The signal from the TIA enters a phase splitter followed by a DC-shift stage and a pair of voltage follower outputs. These are designed to drive a differential (100Ω) load. They are stable for driving capacitive loads such as interstage filters. Since the M02014 exhibits rapid roll-off (3 pole), simple external filtering is sufficient.

3.2.4 Monitor O/P

High impedance output sources a replica average photodiode current for photo-alignment use. The accuracy of this signal does not meet the DDMI Receive Power Specification (SFP-8472) and it is not intended be used as such. Alternatives such as the M02015 TIA or the use of use of the Mindspeed M02040/50 limiting amplifiers’ RxAVGIN pin to bias the photodiode cathode are available to provide an SFP-8472 compliant monitoring function. Ensure that the voltage on VMON is in the range of 0 to 2V.
4.0 Applications Information

4.1 Recommended Pin Diode Connections

Figure 4-1. Suggested PIN Diode Connection Methods

Recommended Circuit:

Alternative Circuit: External PD/APD Bias
4.2 TO-Can Layout

Figure 4-2. Typical Layout Diagram with Photodiode Mounted on PINK Capacitor (5 pin TO-Can)

NOTES:
Typical application inside of a 5 lead TO-Can.
Only one of the $V_{CC}$ pads and one of the GND pads need to be connected (though in noisy environments two or more GND pads connected may improve performance). The backside must be connected to the lowest potential, usually ground, with conductive epoxy or a similar die attach material. If a monitor output is not required then a 4 lead TO-Can may be used.
4.3 Treatment of PINK

PINK requires bypassing to ground with a capacitor when powering a photo diode. If PINK is not used to bias the photo diode, then it is not necessary to bypass an unused PINK.

NOTES:
Typical application inside of a 5 lead TO-Can.
Only one of the Vcc pads and all of the GND pads need to be connected. The backside must be connected to the lowest potential, usually ground, with conductive epoxy or a similar die attach material. If a monitor output is not required then a 4 lead TO-Can may be used.
4.4 TO-Can Assembly Recommendations

Figure 4-4. TO-Can Assembly Diagram

**NOT Recommended Example**

```
This bond is unreliable
```

```
PIN Diode
This bond is too long and unreliable
```

```
M02014
```

```
Ceramic Shim Submount
```

```
TO Can Leads @4 or 5
```

**Recommended Example**

```
Metal Shim
```

```
PIN Diode
```

```
M02014
```

```
Ceramic Shim Submount
```

```
TO Can Leads @4 or 5
```

```
TO-CAN Header
```

```
TO-CAN Header
```

```
TO-CAN Header
```

```
TO-CAN Header
```

4.4.1 Assembly

The M02014 is designed to work with a wirebond inductance of 1 nH ± 0.25 nH. Many existing TO-Can configurations will not allow wirebond lengths that short, since the PIN diode submount and the TIA die are more than 1 mm away in the vertical direction, due to the need to have the PIN diode in the correct focal plane. This can be remedied by raising up the TIA die with a conductive metal shim. This will effectively reduce the bond wire length. Refer to Figure 4-4 above for details.

Mindspeed recommends ball bonding with a 1 mil (25.4 µm) gold wire. For performance reasons the PINA pad is smaller than the others and also has less via material connected to it. It therefore requires more care in setting of the bonding parameters. **For the same reason PINA has no ESD protection.**

In addition, please refer to the Mindspeed Product Bulletin (document number 0201X-PBD-002). Care must be taken when selecting chip capacitors, since they must have good low ESR characteristics up to 1.0 GHz. It is also important that the termination materials of the capacitor be compatible with the attach method used.

For example, Tin/Lead (Pb/Sn) solder finish capacitors are incompatible with silver-filled epoxies. Palladium/Silver (Pd/Ag) terminations are compatible with silver filled epoxies. Solder can be used only if the substrate thick-film inks are compatible with Pb/Sn solders.

4.4.2 Recommended Assembly Procedures

For ESD protection the following steps are recommended for TO-Can assembly:

a. Ensure good humidity control in the environment (to help minimize ESD).

b. Consider using additional ionization of the air (also helps minimize ESD).

c. It is best to ensure that the body of the TO-can header or the ground lead of the header is grounded through the wire-bonding fixture. The best solution will ensure that the $V_{CC}$ lead of the TO-Can is also grounded. When this is done and the procedure below is followed, the photodiode will help reduce the impact to PINA of any positive charge on the wire bonder when bonding to PINA, which is the very last bond placed. (Because the PD is already bonded to PINK and PINK has an internal ESD diode between itself and $V_{CC}$, if $V_{CC}$ is grounded, this will help protect PINA.)

d. The most reliable protection to prevent ESD damage on the die is to assure that the wirebonder (including the spool, clamp, etc.) is properly grounded.

1. Wire bond the ground pad(s) of the die first.
2. Then wire bond the VCC pad to the TO-Can lead.
3. Then wire bond any other pads going to the TO-Can leads (such as DOUT, DOUT and possibly MON)
4. Next wire bond any capacitors inside the TO-Can.
5. Inside the TO-can, wire bond PINK.
6. The final step is to wire bond PINA.
4.5 TIA Use with Externally Biased Detectors

In some applications, Mindspeed TIAs are used with detectors biased at a voltage greater than available from TIA PIN cathode supply. This works well if some basic cautions are observed. When turned off, the input to the TIA exhibits the following I/V characteristic:

Figure 4-5. TIA Use with Externally Biased Detectors, Powered Off

In the positive direction the impedance of the input is relatively high.
After the TIA is turned on, the DC servo and AGC circuits attempt to null any input currents (up to the absolute maximum stated in Table 1-1) as shown by the I/V curve in Figure 4-6.

*Figure 4-6. TIA Use with Externally Biased Detectors, Powered On*

It can be seen that any negative voltage below 200 mV is nulled and that any positive going voltage above the PINA standing voltage is nulled by the DC servo. The DC servo upper bandwidth varies from part to part, but is generally at least 50 kHz.

When externally biasing a detector such as an APD where the supply voltage of the APD exceeds that for PINA, care should be taken to power up the TIA first and to keep the TIA powered up until after the power supply voltage of the APD is removed. Failure to do this with the TIA unpowered may result in damage to the input FET gate at PINA. In some cases the damage may be very subtle, in that nearly normal operation may be experienced with the damage causing slight reductions in bandwidth and corresponding reductions in input sensitivity.
5.0 Die Specification

Figure 5-1. Bare Die Layout

NOTES:
Process technology: CMOS, Silicon Nitride passivation
Die thickness: 300 µm
Pad metallization: Aluminium
Die size: 880 µm x 1090
Pad openings (except PinA): 86 µm across flats
PinA pad: 70 µm across flats (70 µm x 70 µm)
Pad Centers in µm referenced to center of device

<table>
<thead>
<tr>
<th>Pad Number</th>
<th>Pad</th>
<th>X</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>AGC</td>
<td>-329</td>
<td>-76</td>
</tr>
<tr>
<td>2 (1)</td>
<td>VCC</td>
<td>-329</td>
<td>-228</td>
</tr>
<tr>
<td>3</td>
<td>PINK</td>
<td>-124</td>
<td>-434</td>
</tr>
<tr>
<td>4</td>
<td>PINA</td>
<td>124</td>
<td>-434</td>
</tr>
<tr>
<td>5 (1)</td>
<td>VCC</td>
<td>329</td>
<td>-228</td>
</tr>
<tr>
<td>6</td>
<td>MON</td>
<td>329</td>
<td>-76</td>
</tr>
<tr>
<td>7</td>
<td>DOUT</td>
<td>329</td>
<td>76</td>
</tr>
<tr>
<td>8 (1)</td>
<td>DOUTGND</td>
<td>329</td>
<td>228</td>
</tr>
<tr>
<td>9c (1, 2)</td>
<td>GND</td>
<td>329</td>
<td>360</td>
</tr>
<tr>
<td>9b (1, 2)</td>
<td>GND</td>
<td>255</td>
<td>434</td>
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<tr>
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<td>GND</td>
<td>124</td>
<td>434</td>
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<tr>
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<tr>
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<tr>
<td>12</td>
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<td>-329</td>
<td>76</td>
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</tbody>
</table>

NOTES:
1. It is only necessary to bond one VCC pad and one GND pad. However, bonding one of each pad (if available) on each side of the die is encouraged for improved performance in noisy environments.
2. Each location is an acceptable bonding location.
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