Programming Guide, Integer N PLL Synthesizer 100 - 2800 MHz

Rev. V2

Introduction

M/A-COM's surface mount frequency synthesizers integrate a low-noise buffered VCO, phase locked loop circuit and low-pass loop filter. The VCO output is coupled into the PLL circuit where the VCO frequency is divided down in a dual-modulus prescaler and 18-bit N Counter or feedback divider (5-bit swallow counter and 13-bit programmable divider) to the phase comparison frequency or step size of the PLL. This is usually in the range of 10 kHz to 5 MHz for most applications. The prescaler modulus is 32/33. The external reference oscillator is also divided down in the 14-bit programmable R Counter or reference divider to the same phase comparison frequency.

The divided VCO and divided reference signals are then fed into the phase comparator, which produces an error signal whose magnitude is proportional to the phase difference between the two signals. The error signal is then passed through a loop filter to produce the desired performance characteristics and the result is a voltage, which is applied to the tuning input of the VCO. The frequency of the VCO is then steered to the desired frequency, at which point the phase difference in the phase comparator will be zero. The phases of the divided VCO and the divided reference signals are then said to be 'locked' to one another, hence the term phase locked loop.

Any subsequent phase or frequency perturbation on the VCO output results in an error signal at the output of the phase comparator. This error signal in turn produces a modification of the tuning voltage to maintain the phase locked condition. A typical synthesizer block diagram is shown below.

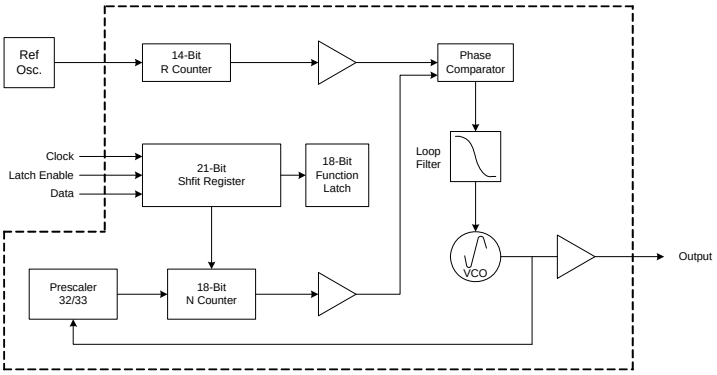
Programming Overview

The programmable dividers and counters are serially programmed using a standard 3-wire CMOS or TTL interface. The programming data is input using the Clock, Data and Load Enable input pins. The Clock input latches one bit on the Data input into the PLL shift register on the rising edge of each clock pulse (MSB first). When the Load Enable input is HIGH the stored data is transferred into the latches. The last two bits are the control bits. The data is transferred into the counters as shown below.

Control		Data location
C2	C1	
0	0	R Counter
0	1	N Counter
1	0	Function Latch
1	1	Initialization

Programming the Reference Word (R Counter)

If the control bits are (C2, C1) = (0, 0), data is transferred from the 21-bit shift register into a latch that sets the 14-bit R Counter. Bits R1 – R14 hold the reference division ratio. Bits R15 – R18 are for test modes, and should be set to 0 for normal use. Bit R19 specifies lock detect (LD) precision and is used in the digital lock detect mode, as described in the Function Latch section. Serial data format is shown on the next page, together with the programming table for the R Counter.



Typical Block Diagram

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MSB LSB

R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	C	C
19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	2	1

14-bit programmable R Counter

Division Ratio (R)	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Notes: Division ratios less than 3 are prohibited.
Division ratios from 3 to 16383 are allowed.

The maximum step size or phase comparison frequency allowable for a given output frequency is given by:

$\triangle F \leq F_{MIN} / P (P - 1)$

Where, $\triangle F$ = phase comparison frequency or step size, F_{MIN} = minimum synthesizer output frequency and P = prescaler modulus. For example, the maximum step size allowable to programme F_{MIN} = 1810 MHz using the modulus 32 prescaler would be $\triangle F \leq$ 1810 MHz / (32 x 31) = $\leq$ 1.82 MHz.

Example

The reference division ratio for the programmable R Counter is calculated using:
$R = F_{REF} / \triangle F$

Where, R = R Counter division ratio, F_{REF} = reference oscillator frequency and $\triangle F$ = phase comparison frequency or step size. Note that the reference frequency used must be an exact multiple of the required phase comparison frequency.

For example, programme the synthesizer to use a phase comparison frequency / step size of 50 kHz using a reference frequency of 10 MHz.

This would require an R Counter division ratio of
R = 10 MHz / 50 kHz = 200 = 11001000 in binary.

Selecting the reference word would require
(C1, C2) = (0, 0).

The complete 21-bit binary reference word to be programmed would then be as below.

MSB LSB

X	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0

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Programming the Frequency Word (N Counter)

If the control bits are (C2, C1) = (0, 1), data is transferred from the 21-bit shift register into a 5-bit latch which sets the swallow (A) counter and a 13-bit latch which sets the programmable (B) counter. The GO bit, N19, sets the charge pump output current. If N19 = 0, I_{CP} = 250µA If N19 = 1, I_{CP} = 1mA. Please refer to individual M/A-COM Component Product Specifications for the charge pump current required in each case. The serial data format and the programming tables for the N Counter are shown below.

Example

The feedback division ratio for the programmable N Counter is calculated using: $N = F_{OUT} / \triangle F$

Where, N = N Counter division ratio, F_{OUT} = synthesizer output frequency and $\triangle F$ = phase comparison frequency or step size. Note that the output frequency must be an exact multiple of the phase comparison frequency. The step size is usually determined by system specifications or the required channel frequency resolution.

In order to programme the A and B Counters the following mathematical relationship is used:
N = (P x B) + A

Where, P = modulus of the prescaler (32), B = B Counter division ratio determined by the integer of N/P, and A = A Counter division ratio determined by the remainder of N/P.

For example, programme the synthesizer to an output frequency of 1810 MHz using a phase comparison frequency or step size of 50 kHz.

Then N Counter division ratio
N = 1810 MHz / 50 kHz = 36200 = (P x B) + A.

B Counter division ratio
B = integer of N / P = 36200 / 32 = 1131 = 10001101011 in binary.

A Counter division ratio
A = remainder of N / P = 36200 – (32 x 1131) = 8 = 1000 in binary.

Selecting the frequency word would require
(C2, C1) = (0, 1).

MSB LSB

GO	Division Ratio of the B Counter													Division Ratio of the A Counter					Control	
N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	C	C
19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	2	1

13-bit Programmable B Counter

Division Ratio (R)	N18	N17	N16	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6
3	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•
8191	1	1	1	1	1	1	1	1	1	1	1	1	1

Notes: B division ratios less than 3 are prohibited.
B division ratios from 3 to 8191 are allowed.
B ≥ A
Control bits (C2, C1) set to (0, 1) to load A and B Counters.
Data is shifted MSB first.

5-bit Swallow A Counter

Division Ratio (R)	N5	N4	N3	N2	N1
3	0	0	0	0	0
4	0	0	0	0	0
•	•	•	•	•	•
8191	1	1	1	1	1

Notes: A division ratios from 0 to 31 are allowed.
B ≥ A

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The complete 21-bit binary frequency word to be programmed would then be as below.

Function and Initialisation Latches

Both the 18-bit Function and Initialisation Latches write to the same registers. For the Function Latch, (C2, C1) = (1, 0).

For the Initialisation Latch, (C2, C1) = (1, 1). Loading the Function Latch with (C2, C1) = (1, 1) immediately followed by an R Counter load, then an N Counter load, efficiently programmes the control register. Setting (C2, C1) = (1, 1) programmes the same Function Latch as a load with (C2, C1) = (1, 0), and additionally provides an internal reset pulse. This programme sequence ensures that the counters are at load point when the N Counter data is latched in and the part will begin counting in close phase alignment.

MSB LSB

X	0	0	1	0	0	0	1	1	0	1	0	1	1	0	1	0	0	0	0	1

Programming the Function Latch

The serial data format is shown below, together with the programming table for the Function Latch.

MSB LSB

F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	C	C
18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	4	3	2	1	2	1

F18	F17-15	F14-11	F10	F9	F8	F7	F6	F5-3	F2	F1	C2	C1
Power down mode	Test modes	Timeout counter value	Timeout counter enable	FastLock control	FastLock enable	CP tri-state	PD polarity	Fo/LD control	Power down	Counter reset	1	0

Bit function description

F1: The counter reset bit, when activated, allows the reset of both N and R Counters. In normal operation this is set to 0.

F2, F18: The powerdown bits provide programmable powerdown modes. In normal operation these are both set to 0.

F3-5: These bits control the function of the Fo/LD output of the PLL IC. On M/A-COM synthesizers, bits (F5, F4, F3) should be set to (0, 0, 1) for digital lock detect or (1, 0, 1) for analog open-drain lock detect.

In digital mode, the Lock Detect output (pin 9 of the synthesizer) goes HIGH when the absolute phase error is <15ns for 3 consecutive phase comparator cycles if bit R19 is LOW, or 5 consecutive phase comparator cycles if bit R19 is HIGH. If the absolute phase error >30ns for a single phase comparator cycle, Lock Detect will go LOW.

In analog mode, when the loop is locked, Lock Detect is HIGH with narrow LOW pulses at the phase comparison frequency. When the loop is out of lock, Lock Detect alternates between HIGH and LOW, at a rate dependent on the frequency error. An external filter is needed, to turn these conditions into stable HIGH or LOW states. See Application Note AN3003 for notes on filter design.

F6: The phase detector polarity bit should be set to 1.

F7: The charge pump tri-state bit should be set to 0 for normal operation.

F8: M/A-COM synthesizers are not designed to use FastLock modes, so F8 should be set to 0.

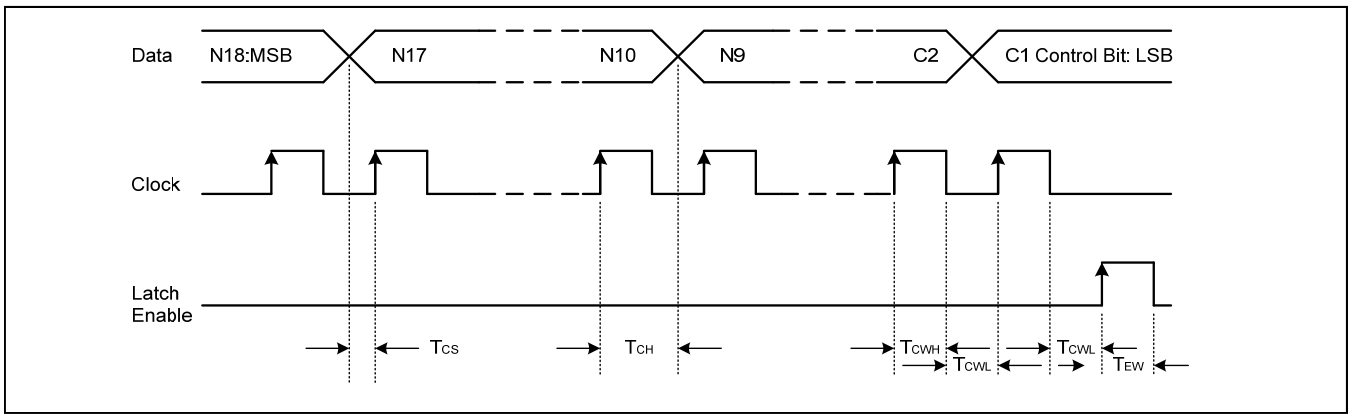
F9-14: The FastLock and timeout counter control bits should be set to 0 on M/A-COM synthesizers.

F15-17: These are for test modes, and should be set to 0 for normal operation.

For more detailed information on the operation of the PLL IC, please refer to the National Semiconductor LMX2326 data sheet.

Serial Data Input Timing Diagram

Data in parenthesis indicates reference word data.
Data shifted into register on rising edge of clock pulses, MSB first.



Electrical Characteristics

Vcc = 5.0V -40°C <T_A < 85°C except as specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VIH	High-Level Input Voltage (3.3V logic)		2.7			V
V_{IL}	Low-Level Input Voltage (3.3V logic)				0.6	V
V_{IH}	High-Level Input Voltage (5V logic)		4.0			V
V_{IL}	Low-Level Input Voltage (5V logic)				1.0	V
I_{IH}	High-Level Input current (Clock, Data)	$V_{IH} = V_{CC} = 5.5V$	-1.0		1.0	mA
I_{IL}	Low-Level Input current (Clock, Data)	$V_{IL} = 0V$ $V_{CC} = 5.5V$	-1.0		1.0	mA
I_{IH}	High-Level Input current (LE, FC)	$V_{IH} = 3.3V$ $V_{CC} = 5.5V$	-1.0		1.0	mA
I_{IL}	Low-Level Input current (LE, FC)	$V_{IL} = 0V$ $V_{CC} = 5.5V$	-1.0		1.0	mA
t_{CS}	Data to Clock Set Up Time	See Data Input Timing	50			ns
t_{CH}	Data to Clock Hold Time	See Data Input Timing	10			ns
t_{CWH}	Clock Pulse Width High	See Data Input Timing	50			ns
t_{CWL}	Clock Pulse Width Low	See Data Input Timing	50			ns
t_{ES}	Clock to Enable Set Up Time	See Data Input Timing	50			ns
t_{EW}	Load Enable Pulse Width	See Data Input Timing	50			ns