Mounting Methods for High Power RF Ceramic Packaged Devices

Introduction

The purpose of this application note is to provide customers with a guide for mounting ceramic packaged high power RF devices to a circuit board. Adherence to the methods described in this document will enable the product to achieve desired RF performance and reliable operation throughout its life.

Using this guide customers should be able to develop mounting procedures that are compatible with their product design and manufacturing processes. These processes will produce a part with good thermal grounding for heat dissipation, good electrical grounding for stable RF performance, and reliable lead connections.

Background

High power ceramic packaged devices have a unique construction, see Figure 1. In the high power package the die is attached to a flange that is attached to the ceramic body. The die is connected internally to leads that protrude from the package body on a different plane than the bottom flange.

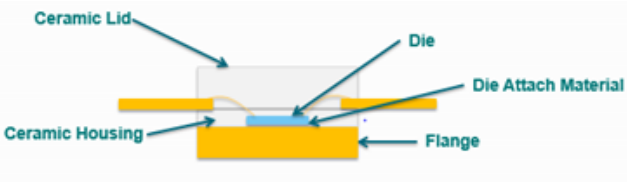


Figure 1: Cross-section diagram of high power ceramic packaged part.

This design enables the package to be mounted in a customer's board so that the package flange can be in direct contact with a metal carrier while the leads can be in contact with the printed circuit board (PCB). This package construction and the high power nature of the device lead to some challenges that need to be considered. These challenges include:

- Maintaining good contact between the flange and carrier for thermal transfer and electrical grounding.
- Attention to cavity height, stack-up of material and process tolerances.
- Attaching leads to PCB without overstressing

There are several ways to mount high power ceramic packages and each has its advantages and disadvantages. It is important to understand these so that the customer can make the best decision considering cost, performance, manufacturability, and reliability.

Application Note

Ceramic Package Attach – Solder-Down Method

The first consideration in mounting the high power ceramic package is the heat slug attach. There are two ways this can be accomplished, the solder-down method or bolt-down method. The best way to mount the flange portion of the package is the solder -down method. When done correctly, it provides a consistent bond between the package flange and the carrier of the board ensuring good thermal contact and electrical grounding for the life of the device.

The carrier is typically made of metal, usually copper or aluminum, and has a solderable surface. A copper carrier is usually plated with Ni followed by a thin layer of Au to prevent the Ni from oxidizing. An aluminum carrier is typically plated by a zincation process, followed by Ni and a thin Au layer.

The solder can be introduced as either preform or paste. Solder preform, which is a pre-cut solder foil usually coated with flux, is the preferred material. This typically produces less voiding than solder paste, resulting in better thermal transfer from the device to the carrier or heat sink. For designs that have more than a 2 or 3 mil between the base of the package and the heat-sink a meshed preform can be used. Meshed preforms typically have copper meshes that form pockets in the preform and prevent the solder from flowing out during reflow maintaining a consistent volume of solder under the device. There are many Pb-based and Pb-free solders available, along with recommended solder reflow profiles, from the solder material suppliers. No-clean flux is recommended as this does not require an aqueous cleaning step after solder reflow. Some suppliers offer different flux formulations even for no-clean. Some are advertised to result in less overall voiding after reflow. The flange of the package can be soldered to the carrier as a separate process step or be done at the same time as the other components and the leads of the package are soldered to the PCB. Refer to Table 1 and Figure 7 for standard Sn-Pb and PB-free reflow profiles. In general to minimize solder voiding the soak time should be extended to drive off flux and the peak temp should be below 240°C.

Ceramic Package Attach – Bolt-Down Method

Even though soldering the flange provides the best interface, there are still customers that prefer to bolt down the part. With the bolt-down method, it is even more important to use the correct hardware, surface finish, cavity height, etc. because there is no solder to compensate for variations between the flange of the package and the carrier. For bolt-down mounting the carrier is typically machined or die cast using an aluminum alloy. The surface flatness of the carrier should not exceed 0.4 mils / inch (0.4 micron / mm) and the average surface roughness (Ra) of the carrier should not exceed 32 micro-inches (0.8 microns). These values can typically be achieved by conventional machining without needing to add process steps such as lapping or polishing. Casting can not usually achieve the appropriate flatness and roughness without an additional machining step in the area where the part is mounted to the carrier.

Using the bolt-down method it is important for the center of the flange to be in direct contact with the carrier, so that there is a good thermal path directly beneath the semiconductor device. See Figure 2 for how the package should be attached to the mating assembly.

Application Note

Ceramic Package Attach – Bolt-Down Method Continued

The part is bolted down using a M2.5, M3, or #4-40 screw along with a matching flat washer and lock washer, see Figure 2. A good bolting technique should be used, recommendation as follows:

1. Tighten each screw on a single part to what is commonly referred to as “finger tightening”.
2. Use a torque wrench to partially tighten each screw.
3. Use a torque wrench set to 5 in.-lbs. to completely tighten each screw.

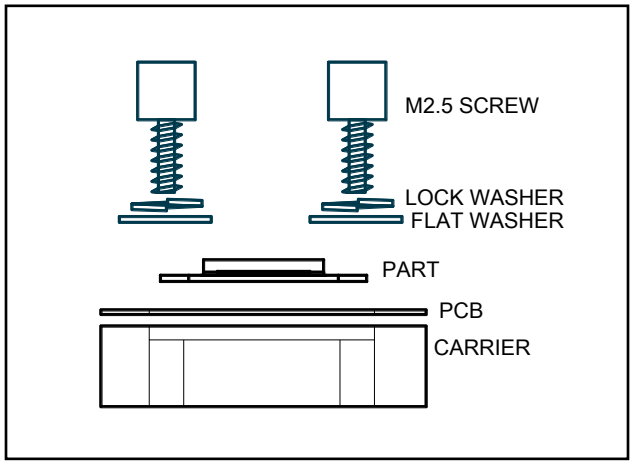


Figure 2: Part mounted with clamp, M2.5 screw, flat washer, and lock washer.

The part can also benefit from the use of an interface material placed between the carrier and the bottom of the package. The interface material should have the same footprint as the part and be made of a material that is electrically and thermally conductive. Examples of materials are: thermal grease, T-GON, PGS, copper foil, and indium foil. These materials must be selected carefully considering the customer’s application to ensure they meet requirements for cost, thermal conductivity, RF stability, corrosion resistance, changing properties over time, manufacturability, etc.

Lead Attach

In combination with both mounting methods, solder-down and bolt-down, the leads are soldered to the PCB. MACOM recommends that the leads be soldered after the flange is attached to the carrier, to minimize stress on the leads and to reduce the chance of voiding on the lead attach interface. Leads can be hand soldered or attached with solder paste in a reflow process.

In the case of hand soldering the tip temperature should be no more than 350°C for Pb-based solder or no more than 400°C for Pb-free solder. Soldering time should not exceed 10s per lead. The solder tip should not touch the ceramic body of the part and leads should be deflected near the lead tips, not near the base. The lead deflection should not exceed 0.010 inches.

In the case of solder paste, the paste can be screen printed on the surface of the PCB. The leads are aligned to the PCB while the flange is aligned to the carrier and then the entire board is sent through a solder reflow process. In combination with the flange solder-down method, the leads and the flange can be attached during the same reflow step or during different steps. Figure 4 shows the recommended land pads that should be used to mount the various ceramic package styles. Figure 5 shows the recommended stencil patterns that should be used to mount the various ceramic package styles. As described previously there are many different Pb-based and Pb-free solder options that are suitable to attach the leads. A typical lead-free solder profile can be seen in Figure 7.

Application Note

Cavity Height

The distance between the top surface of the carrier and the top surface of the PCB (or solder on PCB) is referred to as cavity height. This distance is critical to ensure the flange of the part is making good contact for thermal and electrical grounding while the leads are attached properly without being overstressed for good RF connectivity.

There can be many layers and tolerances that affect the cavity height, see Figure 3. Some layers in the material stack-up, such as the package seating plane and interface material, bring the leads of the package away from the board. Other layers, such as PCB, PCB attach material, and solder (under leads), bring the leads closer to the board. A pedestal or channel usually needs to be added to the carrier so that the part fits properly into the board.

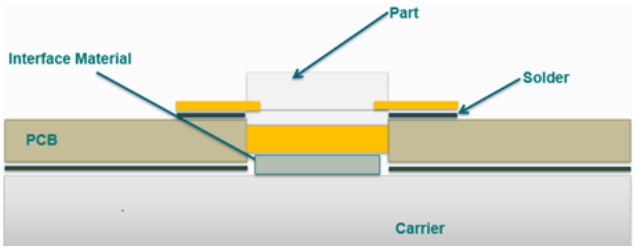


Figure 3 – Material stack-up to determine cavity height.

Each of these layers also has a tolerance that needs to be considered when determining the optimum cavity height. The best method for understanding the total variation of the assembly stack-up and to determine the correct nominal cavity height is the Root Sum of Squares (RSS) method. To do this the customer first needs to determine the standard deviation of each of the materials in the stack-up. If these are not known, they can be derived by assuming a Cpk of 1.0 (±3σ process) and calculating the standard deviation by taking the one-sided tolerance and dividing it by 3. The total standard deviation is then calculated by adding the squares of the individual standard deviations and then taking the square root of this sum.

The following example will help illustrate this method.

Assume the customer is using a package with a seating plane of 0.050”±0.002”, a PCB with thickness 0.032”±0.002”, an epoxy preform under the PCB with thickness 0.003”±0.001”, solder under leads with thickness 0.002”±0.001”, and solder preform (under package) with thickness 0.002”±0.0005”. The machining tolerance of the cavity or pedestal in the carrier, which can typically be held to ±0.001”, should also be considered. The nominal protrusion of the package would be:

Nominal Protrusion = Seating plane + solder preform - PCB - epoxy preform - solder

Nominal Protrusion = 0.050” + 0.002” - 0.032” - 0.003” - 0.002” = 0.015”

The total standard deviation would be:

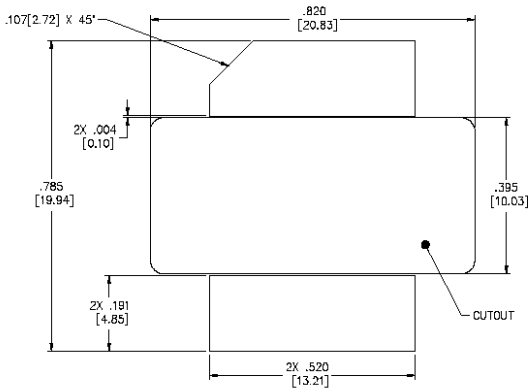
$$\sigma_{total} = \sqrt{\sigma_{seating\ plane}^2 + \sigma_{PCB}^2 + \sigma_{epoxy\ preform}^2 + \sigma_{solder}^2 + \sigma_{solder\ preform}^2 + \sigma_{machining}^2}$$

$$\sigma_{total} = \sqrt{(0.002/3)^2 + (0.002/3)^2 + (0.001/3)^2 + (0.001/3)^2 + (0.0005/3)^2 + (0.001/3)^2} = 0.001”$$

Assuming again a process Cpk of 1.0, the total variation will be ±0.003” (3 X 0.001”). This indicates that the package (and preform in this case) will protrude 0.015”±0.003”. A channel will need to be added to the carrier to accommodate this protrusion. If this number were negative a pedestal would need to be added to the carrier. In this case the nominal channel depth should be 0.013”. It is usually better to make the channel depth smaller than the nominal protrusion to ensure the heat slug of the package is well grounded, and compensate with solder under the leads or bending the leads down slightly to the PCB. In contrast, if the channel depth is too deep the leads prevent the heat slug from making contact with the carrier and applying additional force to bend the leads near the package body can damage the package.

Application Note

Figure 4: Land Pad Layouts



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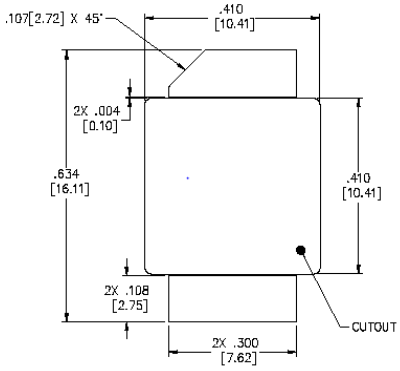
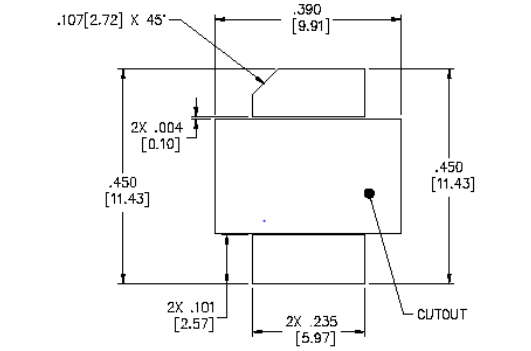
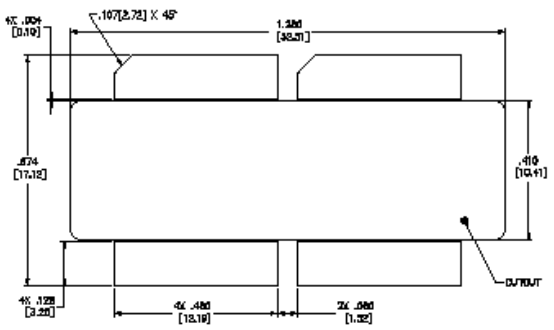


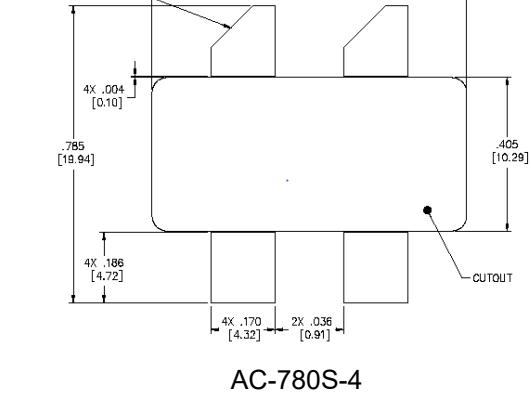
AC-400S-2



AC-360S-2



AC-1230S-4



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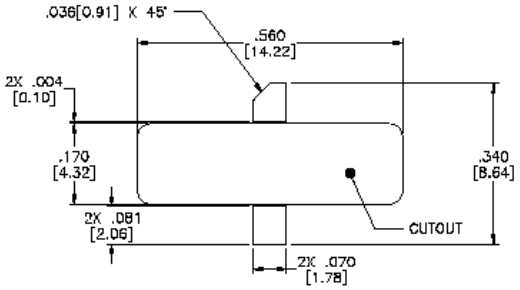
Application Note

Figure 4: Land Pad Layouts



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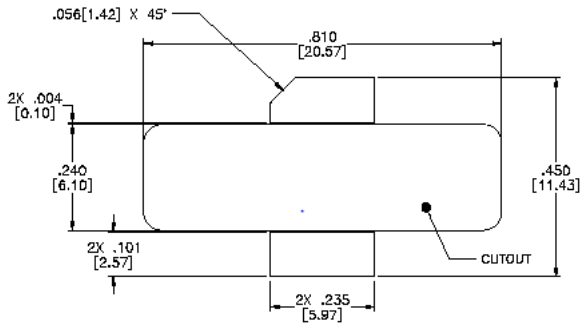
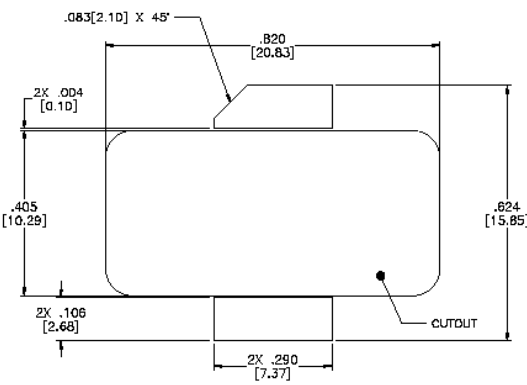
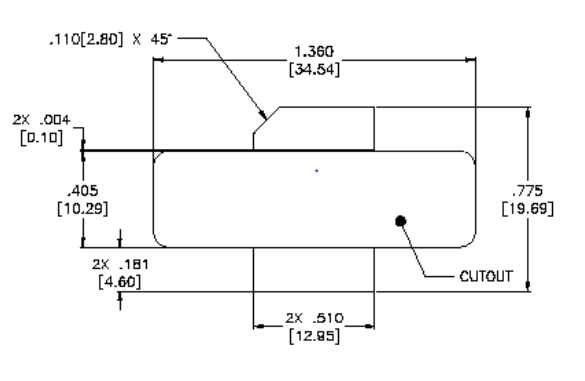


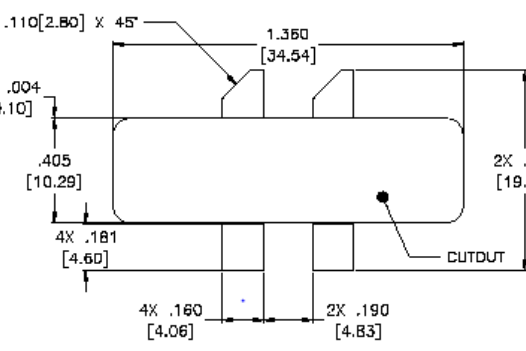
AC-360B-2



AC-400B-2



AC-780B-2



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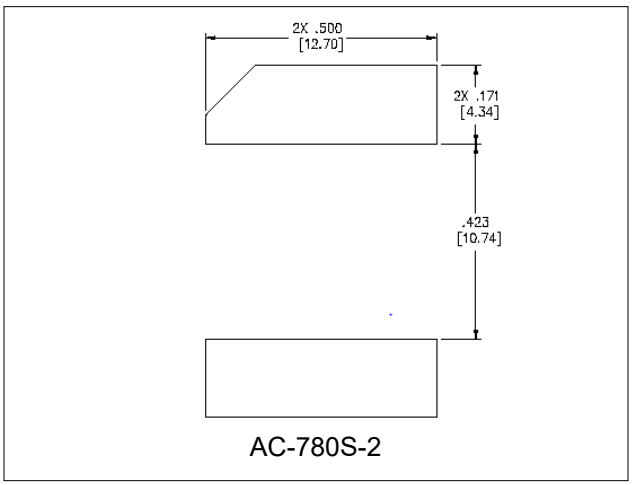
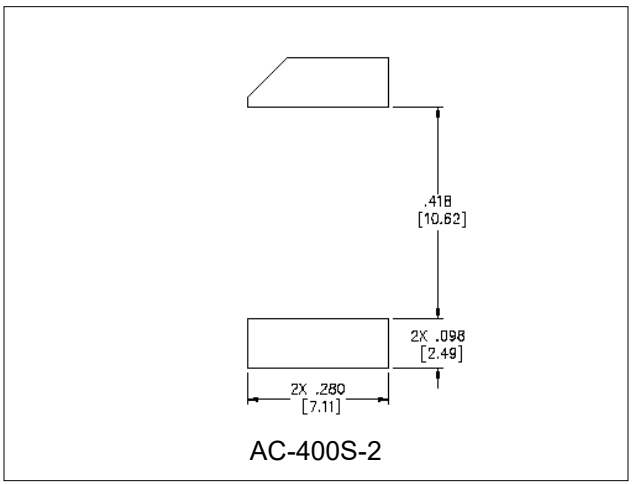
Application Note

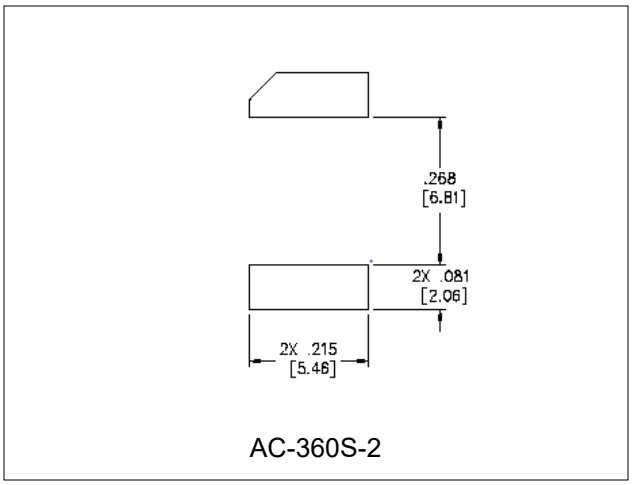
Figure 5: Stencil Layouts



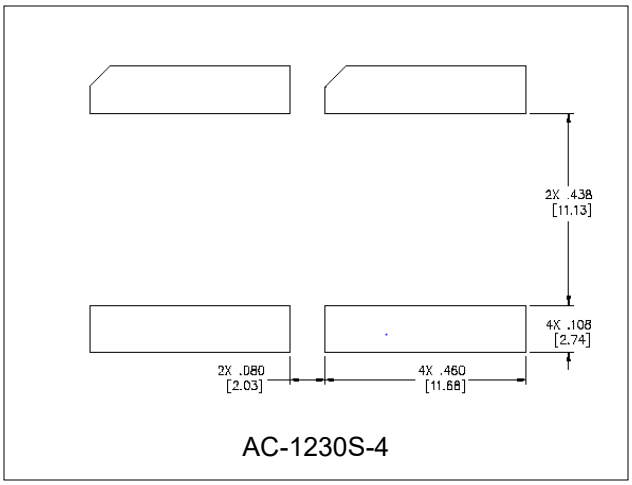
AC-780S-2



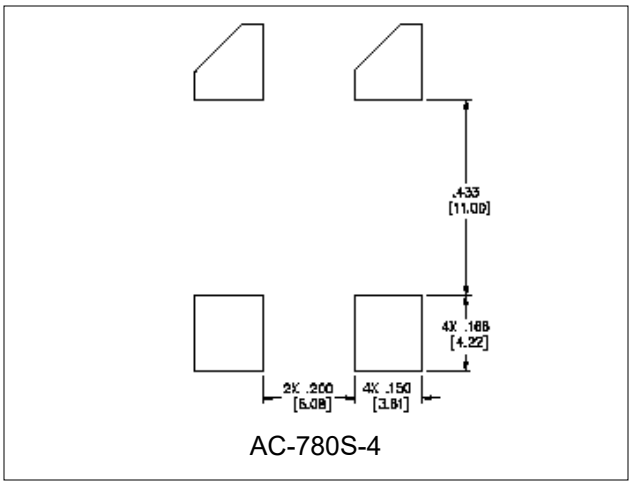
AC-400S-2



AC-360S-2



AC-1230S-4



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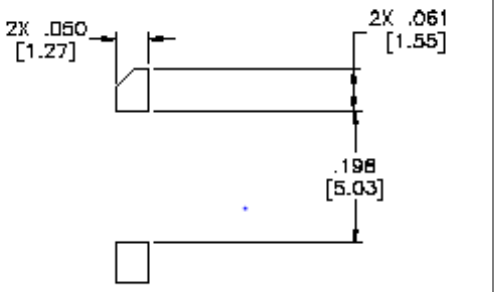
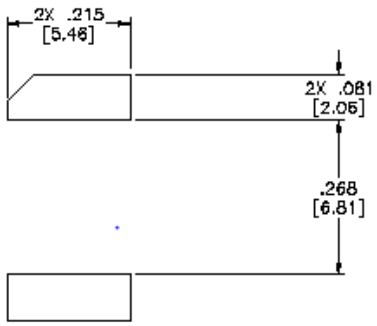
Application Note

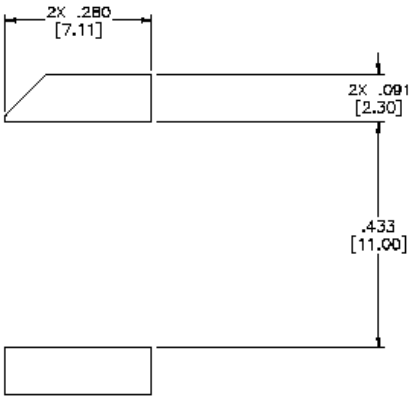
Figure 5: Stencil Layouts



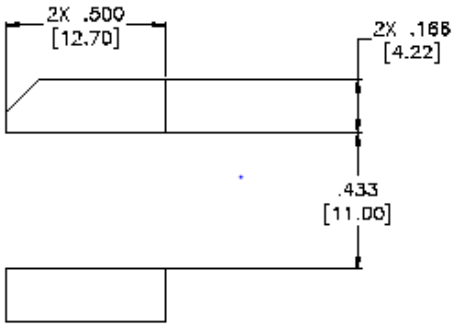
AC-200B-2



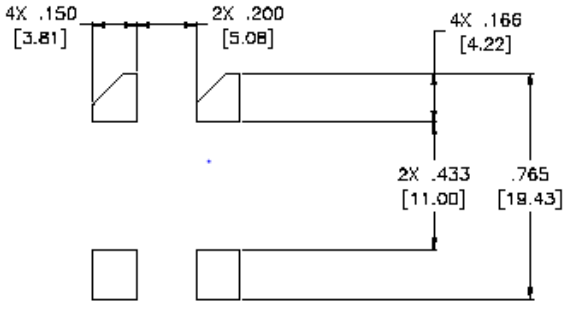
AC-360B-2



AC-400B-2



AC-780B-2



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Application Note

Reflow Profile

The most common solder reflow method is accomplished in a belt furnace using convection heat transfer. Tables 1 thru 3 along with Figure 7 show a typical convection reflow profile of temperature versus time. The profile reflects the three distinct heating stages, or zones (preheat, reflow, and cooling) recommended in automated reflow processes to ensure reliable, finished solder joints. The profile will vary among soldering systems and is intended as an example to use as a starting point. Other factors that can affect the profile include the density and types of components on the board, type of solder used and type of board or substrate material being used.

Thermocouples should be securely attached to the top surface of a representative component to insure the temperature exposure is met. Profile should be recorded by data acquisition for future reference.

General Soldering Precautions

The melting temperature of solder generally exceeds the recommended maximum operating temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, always observe the following instructions to minimize the thermal stress to the devices.

- Always preheat the device (failure to do so can cause excessive thermal shock and stress that can result in damage to the device).
- Limit the temperature in the reflow stage to peak temperature indicated in Tables 1 thru 3.
- After completing the soldering process, allow the devices to cool naturally for at least 3 minutes. Gradual cooling should be used, as the use of forced cooling will increase the temperature gradient and may result in latent failure due to mechanical stress.
- Avoid any mechanical stress or shock to the solder joints and devices during cooling.

Application Note

Table 1. Reflow Conditions

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature Min (Ts_{min}) Temperature Max (Ts_{max}) Time (t_s) from (Ts_{min} to Ts_{max})	 100°C 150°C 60 - 120 seconds	 150°C 200°C 60 - 120 seconds
Ramp-Up Rate (T_L to Tp)	3°C/second max.	3°C/second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	183°C 60 - 150 seconds	217°C 60 - 150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the Classification temperature in Table 4 For suppliers Tp must not exceed the Classification temperature in Table 4	For users Tp must not exceed the Classification temperature in Table 5 For suppliers Tp must not exceed the Classification temperature in Table 5
Time (tp)* within 5 °C of the specified Classification temperature (T_C), see re-flow profile	20* seconds	30* seconds
Ramp-Down Rate (Tp to T_L)	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum		

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), T_p **shall** be within ± 2 °C of the live-bug T_p and still meet the T_c requirements, otherwise, the profile **shall** be adjusted to achieve the latter. To accurately measure actual peak package body temperatures refer to JEP140 for recommended thermocouple use.
Note 2: Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table 3
For example, if T_c is 260 °C and time t_p is 30 seconds, this means the following for the supplier and the user.
For a supplier: The peak temperature must be at least 260 °C. The time above 255 °C must be at least 30 seconds.
For a user: The peak temperature must not exceed 260 °C. The time above 255 °C must not exceed 30 seconds.
Note 3: All components in the test load **shall** meet the classification profile requirements.
Note 4: SMD packages classified to a given moisture sensitivity level by using Procedures or Criteria defined within any previous version of J-STD-020, JESD22-A112 (rescinded), IPC-SM-786 (rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification temperature is desired.

Table 2. SnPb Eutectic Process - Classification Temperature (T_C)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235°C	220°C
≥2.5 mm	220°C	220°C

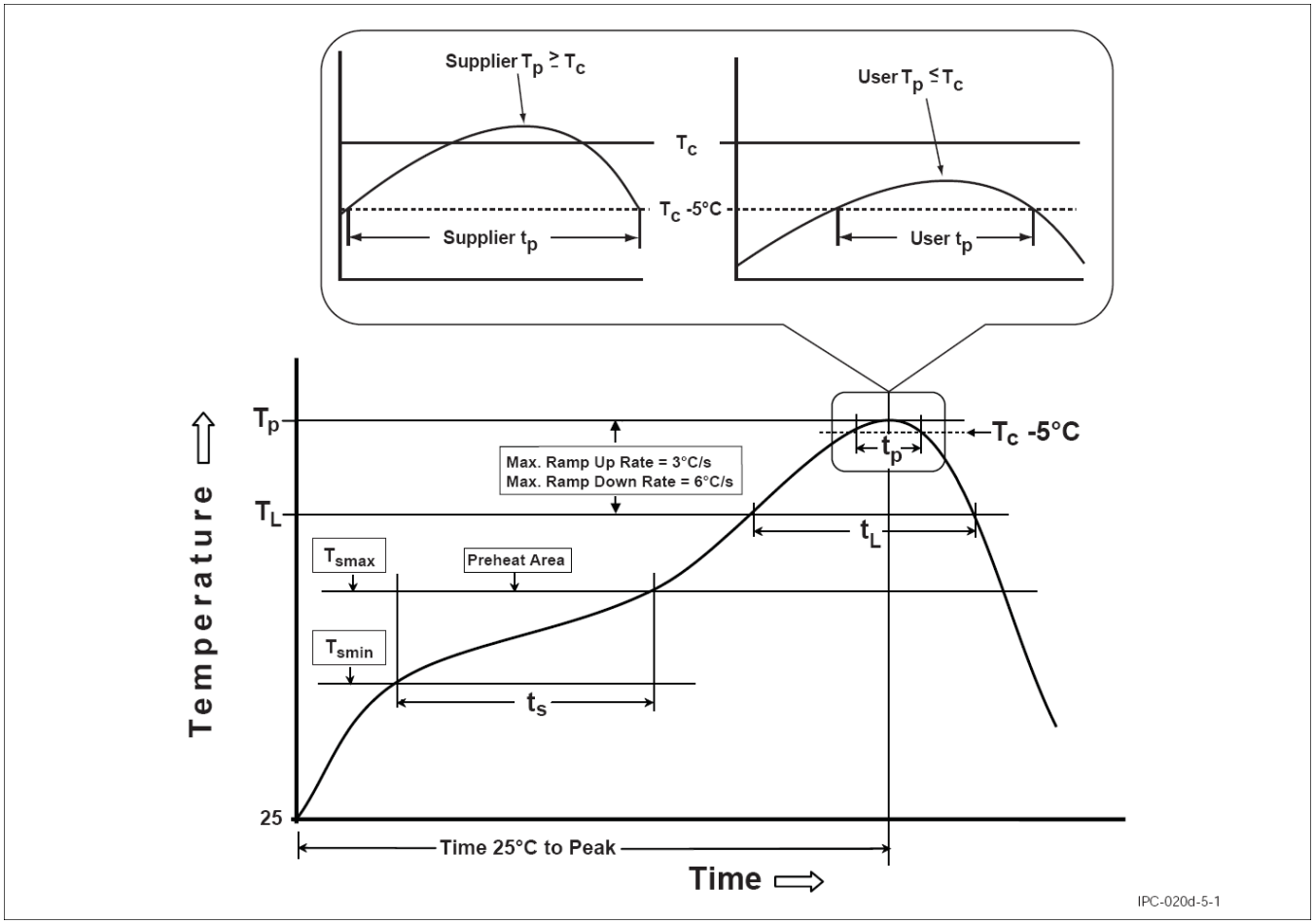
Application Note

Table 3. Pb-Free Process - Classification Temperature (T_C)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm - 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Note 1: At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (T_p) can exceed the values specified in Tables 4 or 5. The use of a higher T_p does not change the classification temperature (T_c).
Note 2: Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.
Note 3: The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.
Note 4: Moisture sensitivity levels of components intended for use in a Pb-free assembly process **shall** be evaluated using the Pb-free classification temperatures and profiles defined in Tables 3 and 5, whether or not Pb-free.
Note 5: SMD packages classified to a given moisture sensitivity level by using Procedures or Criteria defined within any previous version of J-STD-020, JESD22-A112 (rescinded), IPC-SM-786 (rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification temperature is desired

Figure 7: Reflow Profile



Application Note

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