AN-0004357

Low Cost Active Bias Circuit for GaAs FET Amplifiers

Due to variations in semiconductor processes, particularly those inherent to Enhancement Mode (E-mode) FET devices, there is potential for the drain current to vary between amplifiers set at a fixed gate voltage. This effect is seen to a greater extend in E-mode devices than Depletion mode (D-mode) devices. As key RF parameters such as P1dB and OIP3 are highly dependent on the drain current, some applications may require a tighter control of drain current than that which can be realized by biasing the gate at a fixed voltage. The most effective way to achieve this is through the use of an active bias circuit, which monitors the current on the drain supply and actively adjusts the gate voltage to set it to a predetermined value. This Application Note will introduce such a circuit.

There are several possible implementations of this type of circuit all of which involve the use of a small 'current sensing' series resistor in the drain supply. The voltage drop across the sensing resistor is used to determine the current flowing on the drain line. A comparator circuit, implemented using an operational amplifier or, for greater design flexibility, a BJT circuit is then used to close the loop and provide a voltage to the gate of the amplifier thus adjusting the drain current to a desired level. If required, additional functionality can be added to the circuit to enable sequencing of the gate and drain voltages to ensure safe startup. D-mode pHEMT amplifiers typically require proper sequencing

The bias network discussed here can be used for both E-mode (E-pHEMT) and D-mode (pHEMT) amplifiers. Figure 1 below shows the schematic for the D-mode (pHEMT) amplifier since it includes the sequencer M1, R7 and R8 along with a negative supply voltage V2. For E-mode (E-pHEMT) amplifiers, no sequencer is required; therefore, M1, R7 and R8 can be removed, V2 is grounded (set to zero) and V1 is connected to the Vdd node.

The circuit provides set points for voltage at two locations (Vdrain and Vg1) as well as the ability to control the drain current of an amplifier. Referring to figure 1, it starts with a basic template and then allows for adjustment of a few resistors to get the operation bias points you need. Resistors R3, R4 and R6 are used for biasing, while R7 and R8 are used in the sequencer. R1, R2, and R5 are chosen as reasonable values for components, but are not set in stone. Changing these component values will affect the rest of the design, but the operation of the bias network does not hinge on a particular value in the same way it does with the other components.
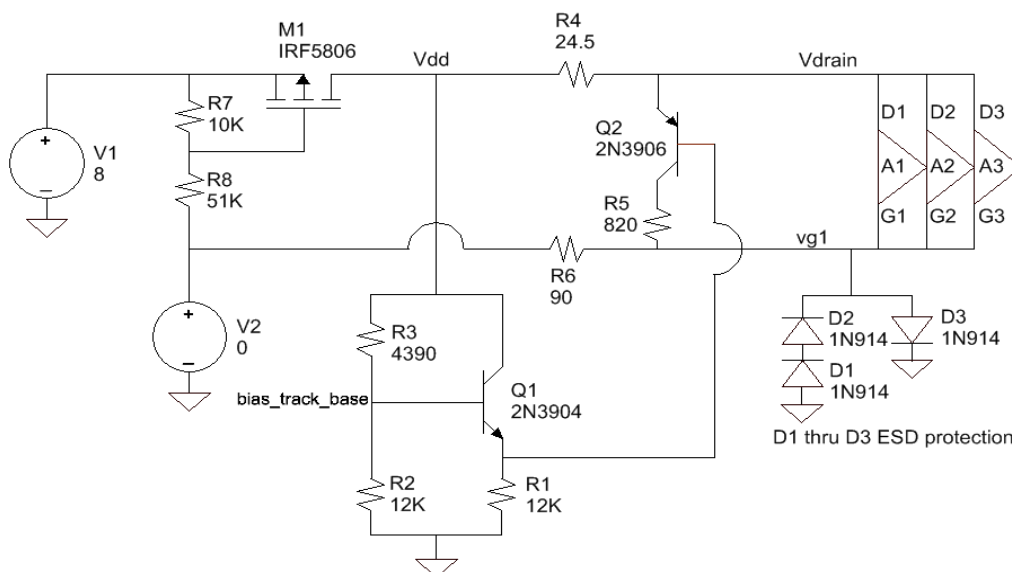

Figure 1 Active bias circuit for D-mode pHEMT amplifiers (A1, A2, A3) with sequencing. For E-pHEMT amplifiers; no sequencer components M1, R7 and R8 are required; V2 is equal to zero (grounded) and V1 is connected directly to the Vdd node.

For further information and support please visit:
https://www.macom.com/support

Low Cost Active Bias Circuit for GaAs FET Amplifiers

V1

The first step to determine the values in the BJT bias network is to calculate Q2 V_{CEsat}. This can be done using the formula shown below[1]:

$$V_{CEsat} = Vt * \ln((1 + (\beta_{FORCED} + 1) / \beta_R) / (1 - \beta_{FORCED} / \beta_F)) \quad (1)$$

Once this value is known, the next step is to determine the current flowing through R6. To do this, we start by subtracting V_{CEsat} from our desired drain voltage to give the voltage at the collector of Q2. This gives the voltage at one side of R5. Since R5 is known and the other side is at the desired gate voltage, the current through R5 is:

$$I_{R5} = (V_{COLLECTOR} - V_{GATE}) / R5 \quad (2)$$

Now, the current flowing through R6 is the current flowing through R5 as well as the typical gate current leakage of the device. Since this circuit is intended to be used for low noise amplifiers, typical gate current is assumed to be 1 mA. This gives:

$$R6 = (V_{SS} - V_{GATE}) / (I_{R5} + I_{GATE}) \quad (3)$$

With the current and voltage known through R6, it is now possible to get an optimal value for R6. The next step is to calculate R4. Since the current through R4 needs to equal the current flowing through the BJT and through the device drains, it is now simple to calculate the optimal value for R4. R4 is going to need to be able to dissipate a relatively low voltage with a high current, so it will be a low resistance that needs to be able to handle high power without overheating or other problems.

$$R4 = (V_{DD} - V_{DRAIN}) / (I_{R5} + I_{DRAIN}) \quad (4)$$

Now that BJT Q2 has established points for the collector and emitter, the next task is to set the point for the base of Q2 to allow it to operate in the proper way. Since the emitter shares the same voltage as the drains, the drop between emitter and base is just the V_{BE}sat of the BJT. Since that base is connected to the emitter of transistor Q1, the base of Q1 is simply:

$$V_B = V_E + V_{BEsat} \quad (5)$$

With the proper voltage on the emitter and the base and the collector connected to V_{DD}, now we can calculate the current through R1. The base current through Q1 can be calculated as well because the ratio is the value for Beta on the transistor:

$$I_B = I_C / \beta \quad (6)$$

Using the current through the base, we can calculate the nominal value for R3.

$$R3 = (V_{DD} - V_B) / (I_B + (V_B / R2)) \quad (7)$$

2

Low Cost Active Bias Circuit for GaAs FET Amplifiers

Once R3 is calculated, the final step is to determine how you want the sequencer to operate.

The sequencer in this case is a p-channel MOS device. The larger MOS switching devices usually have a protection diode in parallel with the drain-source path. It's important to pay attention to this diode. If the device is inserted backwards, the diode will always conduct, irrespective of the gate voltage! In this case, it is important to understand if the system V_2 supply will be -5 V when operating and 0 V when not operating. If it could be other potentials or an open this needs to be considered.

The idea of the sequencer is to turn the gate voltage on before applying the drain voltage to the FET amplifier. In the case shown in figure 1 and to turn on the p-channel MOS FET, a simple resistor divider network (R7 & R8) is used. To get the MOS FET to snap on faster, the output of a logic gate or op amp circuit could be used instead.

Now, an example for the MAAL-011141 E-pHEMT amplifier (no negative bias or sequencer required).

Given:
Q1 Beta	200
Q1 VBEsat	0.75 V
Q2 Beta	200
Q2 VBEsat	-0.9 V
V_{DD}	8 V
V_2	0 V (Enhancement mode FET. No negative supply required.)

Requirements:
V_{GATE} typ	0.5 V
I_{GATE} typ	0.001 A
V_{DRAIN} typ	6 V
I_{DRAIN} typ	0.075 A

Baseline Component Values:
R1	1200
R2	1200
R5	820

PNP V_{CEsat}:
βF	50
βforced	15
βR	0.1
Vt	0.025 V

Calculations:

$V_{CEsat} = Vt * \ln((1 + (\beta_{FORCED} + 1) / \beta_R) / (1 - \beta_{FORCED} / \beta F))$
$= 0.136$

$V_{COLLECTOR} = V_{DRAIN} - V_{CEsat}$
$= 5.864$

$IR5 = (V_{COLLECTOR} - V_{GATE}) / R5$
$= 0.00654$

For further information and support please visit:
https://www.macom.com/support

Low Cost Active Bias Circuit for GaAs FET Amplifiers

V1

$R6 = (V_2 - V_{GATE}) / (I_{R5} + I_{GATE})$
= 90.2

$R4 = (V_{DD} - V_{DRAIN}) / (I_{R5} + I_{DRAIN})$
= 25.5

$V_{B2} = V_{DRAIN} - V_{BEsat2}$
= 5.1

$V_{B1} = V_{E1} + V_{BEsat1}$
= 5.85

$I_{R1} = V_{E1} / R1$
= 0.000425

$I_{B1} = I_{C1} / \beta1$
= 0.000002125

$R3 = (V_{DD} - V_{B1}) / (I_{B1} + (V_{B1}/R2))$
= 4391

Next, an example for the MAAM-011109 amplifier which uses depletion mode pHEMT technology and will require a sequencer.

Given:
Q1 Beta	200
Q1 VBEsat	0.75 V
Q2 Beta	200
Q2 VBEsat	-0.9 V
V_{DD}	6 V
V_2	-5 V

Requirements:
V_{GATE} typ	-0.5 V
I_{GATE} typ	0.001 A
V_{DRAIN} typ	5 V
I_{DRAIN} typ	0.170 A

Baseline Component Values:
R1	1200
R2	1200
R5	820

PNP V_{CEsat}:
βF	50
βforced	15
βR	0.1
Vt	0.025 V

4

Low Cost Active Bias Circuit for GaAs FET Amplifiers

Calculations:

$V_{CEsat} = Vt * \ln((1 + (\beta_{FORCED} + 1) / \beta_R) / (1 - \beta_{FORCED} / \beta F))$
$= 0.136$

$V_{COLLECTOR} = V_{DRAIN} - V_{CEsat}$
$= 4.864$

$IR5 = (V_{COLLECTOR} - V_{GATE}) / R5$
$= 0.00654$

$R6 = (V_2 - V_{GATE}) / (I_{R5} + I_{GATE})$
$= 812$

$R4 = (V_{DD} - V_{DRAIN}) / (I_{R5} + I_{DRAIN})$
$= 5.7$

$V_{B2} = V_{DRAIN} - V_{BEsat2}$
$= 4.1$

$V_{B1} = V_{E1} + V_{BEsat1}$
$= 4.85$

$I_{R1} = V_{E1} / R1$
$= 0.000342$

$I_{B1} = I_{C1} / \beta1$
$= 0.000001708$

$R3 = (V_{DD} - V_{B1}) / (I_{B1} + (V_{B1} / R2))$
$= 2833$

Finally, R7 (10 KOhm) and R8 (51 KOhm) sequencer resistor values are chosen such that the voltage divider network across R7 exceeds the 1.2 V threshold voltage (Vth) of the P-channel MOSFET IRF5806.

Voltage across R7,

$V_{R7} = (V_{DD} + V_2) * R7 / (R7 + R8)$
$= 1.8 V$

To help with the calculations above, an Excel spreadsheet (AN-0004357) can be downloaded from MACOM's website. This calculator tool has all of the equations programmed in it and available for making the active bias circuit's calculations. It is only intended to be used as a starting point. Actual component values will need to be verified and fine-tuned on the bench.

References

[1] Sedra & Smith:*Microelectronic Circuits 3rd Edition*; Saunders College Publishing, 1991; (page 994)

For further information and support please visit:
https://www.macom.com/support

Low Cost Active Bias Circuit for GaAs FET Amplifiers