Quality and Reliability Report

Product Qualification
MASW-007921
2mm 8-Lead Plastic Package

QTR-0148

M/A-COM Technology Solutions Inc.
100 Chelmsford Street
Lowell, MA 01851
Tel: (978) 656-2500
Fax: (978) 656-2900
1. Summary

This document describes the product qualification results for the MASW-007921, a High Power GaAs SPDT Switch housed in a 2mm 8-lead PDFN package.

The MASW-007921 meets M/A-COM Technology Solutions’ (MACOM) reliability requirements and is released for production with a JEDEC J-STD-020 MSL 1 moisture sensitivity level classification.

2. Scope

The qualification was performed to validate the reliability of the pHEMT process and the 2mm 8-lead PDFN package assembly. The results of this report are not limited to the specific product described herein; they apply to a family of products designed at MACOM which use the same wafer fabrication process and/or package assembly.

3. Reference Documents


3.2. JESD22-A104 “Temperature Cycling”

3.3. JESD22-A108 “Temperature, Bias, and Operating Life”

3.4. JESD22-A110 “Highly-Accelerated Temperature and Humidity Stress Test”

3.5. JESD22-A113 “Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing”


3.7. JESD22-B100 “Physical Dimensions”

3.8. JESD22-B102 “Solderability”

3.9. JESD-B108 “External Visual”

3.10. JESD47 “Stress-Test-Driven Qualification of Integrated Circuits”

4. Product Description and Information

The MASW-007921, is a High Power GaAs SPDT Switch housed in a 2mm 8-lead PDFN package.

Each device is 100% RF tested to ensure performance compliance. The part is fabricated using a pHEMT process.

4.1 Die Information

- **Die Size:** 0.725 x 1.115 mm
- **Die Thickness:** 6 mil
- **Fabrication Process:** 0.5 µm pHEMT
- **Mask ID:** 1589

4.2 Assembly and Package Information

- **Package Style:** PDFN
- **Assembly Manufacturer:** Unisem (Malaysia)
- **Package Body Dimensions:** 2.0 x 2.0 x 0.9 mm
- **Lead Count:** 8
- **Leadframe Material:** 194 Cu
- **D/A Pad Size:** 1.0 x 1.6 mm
- **D/A Plating:** Full Spot Ag
- **Lead Pitch:** 0.50 mm
- **Lead Finish:** Matte Tin
- **Die Attach:** Abletherm 2600AT
- **Wirebond:** 1.0 mil Gold Wire
- **Package Material:** Sumitomo EME-G770HCD
- **Marking Method:** Laser

5. Product Qualification Requirements

Qualification testing has been performed to validate the reliable operation of MACOM products manufactured using a GaAs MMIC process. Tests are included to specifically address failure mechanisms related to elevated temperature, temperature cycling, humidity, and applied electrical bias.
5.1 General Information

Qualification Vehicle: MASW-007921  
Lot Numbers/Date Codes: 101, 201/07R, 07U

<table>
<thead>
<tr>
<th>Qualification Tests</th>
<th>Conditions</th>
<th>Endpoints</th>
<th>Fails/SS</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>High Temperature Operating Life (HTOL) (JESD22-A108)</td>
<td>150°C Junction Temperature</td>
<td>1000 Hours</td>
<td>0/192</td>
<td>PASS</td>
</tr>
<tr>
<td>Preconditioning (JESD22-A113) (J-STD-020)</td>
<td>MSL1: 85°C, 85% RH</td>
<td>Bake 125°C 24Hrs Moisture Soak 168 Hrs 3x Reflow</td>
<td>0/78</td>
<td>PASS</td>
</tr>
<tr>
<td>Temperature Cycling (JESD22-A104)</td>
<td>Preconditioned Condition H -55°C to +150°C</td>
<td>200 Cycles</td>
<td>0/40</td>
<td>PASS</td>
</tr>
<tr>
<td>HAST (JESD22-A110)</td>
<td>Preconditioned 130°C, 85% RH, 15psig</td>
<td>96 Hours</td>
<td>0/37</td>
<td>PASS</td>
</tr>
<tr>
<td>Solderability (JESD22-B102)</td>
<td>Method 1</td>
<td>N/A</td>
<td>0/5</td>
<td>PASS</td>
</tr>
<tr>
<td>Physical Dimensions (JESD22-B100)</td>
<td>Coplanarity, 4 mils</td>
<td>N/A</td>
<td>0/20</td>
<td>PASS</td>
</tr>
<tr>
<td>Destructive Physical Analysis (DPA) (MIL-STD-883)</td>
<td>X-ray, C-SAM, Visual inspection, Bond pull</td>
<td>N/A</td>
<td>0/5</td>
<td>PASS</td>
</tr>
<tr>
<td>ESD (HBM) (JESD22-A114)</td>
<td>1 positive discharge and 1 negative discharge per pin for each pin combination</td>
<td>3 devices/level</td>
<td>0/30</td>
<td>150V Class 0B</td>
</tr>
</tbody>
</table>

1. Not all parts subjected to Preconditioning were used for subsequent qualification testing.
Analysis of Results

6.1 High Temperature Operating Life (HTOL)

Description  This stress is used to identify any failure mechanisms accelerated by DC bias and elevated temperature that could occur during the lifetime of the product under test. Typical failure mechanisms that may occur include gate oxide breakdown, ionic contamination, and electromigration for silicon (Si) technologies, or gate sinking, ohmic contact degradation, and trap generation for gallium arsenide (GaAs) technologies. Process and/or assembly defects may be detected by this test in either technology. Devices are biased and operated at junction temperatures between 125°C and 160°C. Once failure mechanisms are identified, device lifetime at normal operating temperatures may be predicted. Devices are stressed for 1000 hours followed by electrical test. JESD22-A108 is used as a guideline.

Results  No evidence of wearout failure was found during this test. The HTOL test boards are optimized for stable use at elevated temperature. Since the boards are designed to withstand temperature extremes and not for optimal performance, the devices may not meet datasheet limits. Therefore, failure criteria is based on pre and post stress deltas. The results indicate that the devices are stable and reliable.

6.2 Preconditioning/Moisture Sensitivity Level (MSL) Classification

Description  Preconditioning is performed to simulate the effects of board assembly on moisturized packages, prior to reliability testing. During preconditioning, test samples are subjected to temperature dry bake, moisture soaking, solder reflow simulation, and electrical test before reliability testing. Preconditioning is performed before Temperature Cycling and Temperature Humidity Bias stressing. MSL stressing is performed to identify the classification level of nonhermetic surface mounted devices that may be sensitive to moisture-induced stress so that they can be properly packaged, stored, and handled to avoid damage during assembly solder reflow attachment and/or repair operations. JESD22-A113 is used as a guideline.

Results  No failures were observed either visually or electrically. This indicates that the devices may be safely handled, stored, assembled, and reworked per the tested MSL conditions.
6.3 Temperature Cycling

**Description**  Unbiased devices are exposed to sudden extreme temperature changes. This accelerated stress test simulates equipment that is operated intermittently at low temperatures. Devices are exposed to a high temperature for a time long enough to assure a stable temperature is reached by all the samples (typically 10 to 15 minutes) and then immediately transferred to a low temperature (transfer time ~10 seconds) and held for the same length of time. After 200 cycles, the devices are electrically tested and visually checked for any mechanical damage. JESD22-A104 is used as a guideline.

**Results**  No failures were observed either visually or electrically. This indicates that the mechanical assembly of the integrated circuits can withstand sudden extreme temperature changes with no degradation in performance or construction. It also indicates that no problems exist due to the internal mechanical stresses between the mold compound, leadframe, and die.

6.4 Highly Accelerated Stress Test (HAST)

**Description**  This stress is performed for the purpose of evaluating the reliability of non-hermetic packaged solid-state devices in humid environments. It employs severe conditions of temperature, humidity, and bias which accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it. This stress usually activates the same failure mechanisms as the “Steady-State Humidity Life Test (THB 85°C/85%RH described in JEDEC JESD22-A101) in an accelerated manner. Common types of failures include bond pad corrosion and electrolytic conduction. Devices are biased so that the device is in a low current state to minimize package drying. Devices are stressed for 96 hours with electrical testing performed after. JEDEC Standard JESD22-A110 is used as a guideline.

**Results**  The results indicate that the passivation layer, die-edge termination, and plastic packaging provide excellent resistance to moisture ingress.
6.5 Physical Integrity

**Description**  Coplanarity, marking permanency, and solderability were performed to verify the legibility and permanence of marking and to determine the ability of the device to be properly soldered to a printed circuit board. The appropriate test methods specified by MIL-STD-883 were used as guidelines for these tests.

**Results**  All markings were legible and showed no signs of degradation after the cleaning steps. Coplanarity was within spec and devices were properly wetted and exhibited a continuous solder coating free from defects for a minimum of 95% of the critical surface area of any individual termination.

6.6 Destructive Physical Analysis (DPA)

**Description**  X-ray, CSAM, and visual inspection of devices are performed to verify the physical integrity of the assembled integrated circuit. For this product bond pull testing was also performed. The appropriate test methods specified by MIL-STD-883 were used as guidelines for these tests.

**Results**  All physical dimensions and workmanship were within specification and showed no significant variation. This data indicates that the process is uniform and is in statistical control.

6.7 Electrostatic Discharge Sensitivity (ESD) Classification

**Description**  This stress is performed to evaluate the device’s susceptibility to damage or degradation by electrostatic discharge that may be encountered during the routine handling and assembly of the device. Human Body Model (HBM) testing was performed per JESD22-A114.

**Results**  The level of ESD that the device can safely tolerate was determined and recorded in the Qualification Tests table.
7. Predicted Failure Rates

Most integrated circuit failure mechanisms are based on physical or chemical reactions. These reactions are accelerated by temperature and can be modeled using the Arrhenius equation. The acceleration factor (AF) between any two temperatures may be calculated as follows:

\[
AF = e^{\frac{E_a}{k}(\frac{1}{T_1} - \frac{1}{T_2})}
\]

Where:
- \(AF\) = acceleration factor
- \(e\) = natural log
- \(E_a\) = activation energy in electron volts
- \(k\) = Boltzman's constant (8.62 x 10^{-5} eV/K)
- \(T_1\) = derated temperature (K)
- \(T_2\) = stress temperature (K)

The following assumptions have been made in M/A-COM Technology Solutions determination of failure rates:

- Activation energy for the 0.5 µm pHEMT (IS) process = 1.88 eV
- Junction temperature during HTOL = 150°C

Next, a Chi square approximation of the mature life failure rate can be made using the following information:

\[
\text{Failure rate} (X^2) = \frac{X^2}{(2f + 2, \alpha)}
\]

Where:
- \(f\) = number of failures
- \(\alpha\) = 1 – confidence level
- \(n\) = quantity tested
- \(T\) = test duration (hours)
- \(AF\) = acceleration factor

Therefore, for the MASW-007921 built using the 0.5 µm pHEMT process, the predicted failure rates are as follows:

<table>
<thead>
<tr>
<th>Confidence Level</th>
<th>Use Temperature</th>
<th>X² Value</th>
<th>AF</th>
<th>Equivalent Device Hours</th>
<th>Failure Rate (FITS)</th>
<th>MTBF (Hours)</th>
</tr>
</thead>
<tbody>
<tr>
<td>60%</td>
<td>85°C</td>
<td>1.83</td>
<td>11668.56</td>
<td>2.24E+09</td>
<td>0</td>
<td>2.45E+09</td>
</tr>
<tr>
<td>60%</td>
<td>55°C</td>
<td>1.83</td>
<td>3074469.92</td>
<td>5.90E+11</td>
<td>0</td>
<td>6.44E+11</td>
</tr>
<tr>
<td>90%</td>
<td>85°C</td>
<td>4.61</td>
<td>11668.56</td>
<td>2.24E+09</td>
<td>1</td>
<td>9.73E+08</td>
</tr>
<tr>
<td>90%</td>
<td>55°C</td>
<td>4.61</td>
<td>3074469.92</td>
<td>5.90E+11</td>
<td>0</td>
<td>2.56E+11</td>
</tr>
</tbody>
</table>
Parts Qualified by Similarity (QBS) per JESD47

<table>
<thead>
<tr>
<th>Device</th>
<th>QBS For</th>
<th>ESD (HBM)</th>
<th>ESD (CDM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MASW-009276</td>
<td>Process</td>
<td>550V</td>
<td>N/A</td>
</tr>
<tr>
<td>MASW-009590</td>
<td>Process</td>
<td>350V</td>
<td>N/A</td>
</tr>
</tbody>
</table>

Revision History

Rev - released September 30, 2014 (original qual date June 5, 2008) Loren Reifsteck

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