ATM OC-3 Service SAR Plus with xBR Traffic Management

Mindspeed's CN8236 Service Segmentation and Reassembly (ServiceSAR) controller integrates ATM terminal functions, PCI bus master and slave controllers, and a UTOPIA 1 or 2 interface with service-specific functions in a single package for AAL0, AAL3/4, and AAL5 operations. The ServiceSAR controller generates and terminates ATM traffic (TM.4.1) and automatically schedules cells for transmission with patented xBR traffic management. The CN8236 is targeted at 155 Mbps throughput systems where the number of VCCs is relatively large, or the performance of the overall system is critical. Examples of such networking equipment include routers, Ethernet switches, ATM edge switches, or frame relay switches.

Service-Specific Performance Accelerators

The CN8236 incorporates numerous service-specific features designed to accelerate and enhance system performance. For example, the CN8236 implements echo suppression of LAN traffic via LECID filtering, and supports frame relay DE to CLP interworking.

Advanced xBR Traffic Management

The xBR traffic manager in the CN8236 supports multiple ATM service categories. These include CBR, VBR (both single and dual leaky bucket), UBR, GFR (guaranteed frame rate), and ABR (explicit rate, relative rate and EFCI marking). The CN8236 manages each VCC independently.

**KEY FEATURES**

- AAL0, AAL3/4, AAL5, inter-working function for AAL1/2 scheduling (cell-on-demand scheduling)
- ATM TM 4.1 service categories: ABR, CBR, GFR, VBR-rt, VBR-nrt, GFR
- Service-specific performance accelerators – LECID filtering and echo suppression, CLP0+1, Frame Relay DE interworking
- Dynamic per-VCC scheduling
- Flexible tunneling with mixed service categories (16 priorities)
- Multi-peer architecture with up to 32 peers
- Head-of-line blocking protection for multi-PHY operation
- 64 K VCC, 155 Mbps full duplex with 2-cell PDU
- UTOPIA Level 2, 8/16 bit @ 50 MHz
- 33 MHz (up to 40 MHz), PCI 2.1
- 388 BGA, low-power dissipation

It dynamically schedules segmentation traffic to comply with up to 16+CBR user-configured scheduling priorities for the various traffic classes. Scheduling is controlled by a schedule table configured by the user and based on a user-specified time reference. ABR channels are managed in hardware according to user-programmable ABR templates. These templates tune the performance of the CN8236's ABR algorithms to a specific system's or network's requirements.
Multi-Queue Segmentation Processing

The CN8236's segmentation coprocessor generates ATM cells for up to 64 K VCCs. The segmentation coprocessor formats cells on each channel according to segmentation VCC tables, utilizing up to 32 independent transmit queues and reporting segmentation status on a parallel set of up to 32 segmentation status queues. The segmentation coprocessor fetches client data from the host, formats ATM cells while generating and appending protocol overhead, and forwards these to the UTOPIA port. The segmentation coprocessor operates as a slave to the xBR traffic manager which schedules VCCs for transmission.

Multi-Queue Reassembly Processing

The CN8236's reassembly coprocessor stores the payload data from the cell stream received by the UTOPIA port into host data buffers. Using a dynamic lookup method which supports NNI or UNI addressing, the reassembly coprocessor processes up to 64K VCCs simultaneously. The host supplies free buffers on up to 32 independent free buffer queues. The reassembly coprocessor performs all CPCS protocol checks and reports the results of these checks and other status data on one of 32 independent reassembly status queues.

High-Performance Host Architecture with Buffer Isolation

The CN8236 host interface architecture maximizes performance and system flexibility. The device's control and status queues enable host/SAR communication via write operations alone. This "write-only architecture" lowers latency and PCI bus occupancy. Flexibility is achieved by supporting a scalable peer-to-peer architecture. Multiple host clients can be addressed by the segmentation and reassembly (SAR) as separate physical or logical PCI peers. Segmentation and reassembly data buffers on the host system are identified by buffer descriptors in SAR-shared (or host) memory, which contain pointers to buffers. The use of buffer descriptors in this way allows for isolation of data buffers from the mechanisms that handle buffer allocation and linking. This provides a layer of indirection in buffer assignment and management that maximizes system architecture flexibility.
Designer Toolkit
Mindspeed provides an evaluation environment for the CN8236 which provides a working reference design and facilities for generating and terminating all service categories of ATM traffic. This system accelerates ATM system development by providing a rapid prototyping environment.

What is ATM?
Asynchronous transfer mode (ATM) has emerged as the primary networking technology for next-generation, multiservice communication networks. ATM-enabled services benefit the Internet as well as emerging applications in science, telemedicine, and distance learning. Just as the Internet revolutionized worldwide communications, ATM brings new meaning to high-speed networking.

ATM, which uses a fixed size packet, or cell, is a transport protocol capable of providing a homogeneous network for all traffic types, regardless of whether the application is to carry conventional telephony, entertainment video, or data traffic over LANs, MANs, or WANs.

The ITU-T and ANSI selected ATM for Broadband-ISDN. SONET/SDH, as specified by the ITU, is intended as the primary transport mechanism for ATM cells in WAN applications. ATM also plays a key role in next-generation consumer applications for high-speed Internet access and wireless access. The ADSL Forum and the Universal ADSL Working Group chose ATM as the network layer protocol for G.lite and G.DMT ADSL.

ATM physical layer (ATM-PHY) IC devices adapt ATM cells to and from a broad range of transmission rates ranging from 1.544 Mbps to 2.4 Gbps via a standard system interface called UTOPIA.
Product Features

Service-Specific Performance Accelerators
- LEIDC filtering and echo suppression
- Dual leaky bucket based on CLP (frame relay)
- Frame relay DE interworking
- Internal SNMP MIB counters
- IP over ATM, supports both CLP0+1 and ABR shaping

Flexible Architectures
- Multi-peer host
- Direct switch attachment via reverse UTPIDAC
- ATM terminal
  - Host control
  - Local bus control
- Optional local processor

New Features
- 3.3 V, 38B BGA lowers power and eases PCB assembly (0.75 W max)
- AAL3/4 CPCS generation and checking
- PCI 2.1, including support for serial EEPROM
- Enhancements to XBR Traffic Manager
  - Fewer ABR templates
  - Improved CBR tunneling
- Reduced memory size for VCC lookup tables
- Increased addressing flexibility
- Additional byte lane swappers for increased system flexibility
- UTPIDAC Level 2, 8/16 bit 50 MHz
- Programmable size routing tags for up to 64 byte cells
- Selectable single/separate UTPIDAC clocks
- Interworking function for all AAL1/2 scheduling
  - Cell-on-demand scheduling
  - Updated PM-OAM processing per i.810
  - SECBC calculated per GR-1248
- Paging function in order to gluelessly control RS8228 cell delineator
- Robust EEPROM operation (SAR provides power)
- Compact PCI Hot Swap capabilities
- Master PCI write over read arbitration control
- Increase incoming DMA FIFO buffer from 2 KB to 8 KB
- Prepended VCC index on RSM BOM cells
- Optional reference clock drive scheduler
- Head of line blocking protection for multi-PHY operation

xBR Traffic Management
- TM4.1 Service Classes
  - CBR
  - VBR (single, dual and CLP-based leaky buckets)
  - Real-time VBR
  - ABR (explicit rate, relative rate and EFCI marking)
  - UBR
  - GFC (controlled and uncontrolled flows)
- Guaranteed Frame Rate (GFR)
  - Guaranteed MCR on UBR VCCs
  - 16 levels of priorities (16 + CBR)
- Dynamic per-VCC scheduling
- Multiple programmable ABR templates (supplied by Mindspeed or user)
  - Scheduler driven by selectable clock
  - Local system clock
  - External reference clock
- Internal RM OAM cell feedback path
- Virtual FIFO buffer rate matching (Source Rate Matching)
  - Per-VCC MCR and ICR
  - Tunneling
    - VP tunnels (VCI interleaving on PDU boundaries)
    - CBR tunnels (cells interleaved as UBR, VBR or ABR with an aggregate CBR limit)
- 155 Mbps full-duplex (2-cell PDUs)

Multi-Queue Segmentation Processing
- 32 transmit queues with optional priority levels
- 64 K VCCs maximum
- AAL5 and AAL3/4 CPCS generation
- AAL0 Null CPCS (optional use of PTI for PDU demarcation)
- ATM cell header generation
- Raw cell mode (52 octet)
- 200 Mbps half-duplex
- 155 Mbps full-duplex (with 2-cell PDUs)
- Distributed host or SAR-shared memory reassembly
  - 8 Programmable reassembly hardware time outs (per-VCC assignable)
- Global max PDU length for AAL5
- Per-VCC buffer firewall (memory usage limit)
- Simultaneous reassembly and segmentation
- Idle cell filtering

High-Performance Host Architecture with Buffer Isolation
- Write-only control and status
- Read multiple command for data transfer
- Up to 32 host clients control and status queues
  - Physical or logical clients
    - Enables peer-to-peer architecture
    - Descriptor-based buffer chaining
    - Scatter/gather DMA
  - Endian neutral (allows data word and control word byte swapping, for both big and little endian systems)
  - Non-word (byte) aligned host buffer addresses
  - Automatically detects presence of Tx data or Rx free buffers
  - Virtual FIFO buffers (PCI bursts treated as a single address)
  - Hardware indication of BOM
  - Allows isolation of system resources
  - Status queue interrupt delay

Designer Toolkit
- Evaluation hardware
- Reference schematics
- Generous Implementation of OAM-PM Protocols
- Detection of all F4/F6 OAM flows
- Internal PM monitoring and generation for up to 128 VCCs
- Optional global OAM Rx/Tx queues
- In-line OAM insertion and generation

Standards-Based I/O
- 33 MHz PCI 2.1 (to 40 MHz)
- Serial EEPROM to store PCI configuration information
- PHY interfaces
  - UTPIDAC master (Level 1)
  - UTPIDAC slave (Level 1)
  - UTPIDAC master (Level 2)
  - UTPIDAC slave (Level 2)
- Flexible SAR-shared memory architecture
- Optional local control interface
- Boundary scan for board-level testing
- Source loopback, for diagnostics
- Glueless connection to Mindspeed’s ATM physical layer device, the CX28250 and CN8223

Standards Compliance
- UNI/NNI 3.1
- TM 4.0 / TM 4.1 compliant
- Bellcore GR-1248
- ATM Forum B-ICI V2.0

Ordering Information
Model number: CN8236E8BB
Manufacturing part number: 82836-12P
Product revision: B
Package: 388-pin BGA
Operating temperature: -40°C to 85°C